

TRANSISTOR DATA



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POWER MOSFET TRANSISTOR DATA

After several years of development, Motorola introduced its first power MOSFETs in 1980. Several technologies were evaluated and the final choice was the double diffused (DMOS) process which Motorola has acronymed TMOS. This process is highly manufacturable and is capable of producing devices with the best characteristics for product needed for power control. Most suppliers of power MOSFETs use the basic DMOS process.

The key to success of power MOSFETs is the control of vertical current flow, which enables suppliers to reduce chip sizes comparable to bipolar transistors. This development opens a new

dimension for designers of power control systems.

This manual is intended to give the users of power MOSFETs the basic information on the product, application ideas of power MOSFETs and data sheets of the broadest line of power MOSFETs with a variety of package configurations. The product offering is far from complete. New products will be introduced and old products will be improved, offering designers an even better selection of products for their designs.

Motorola has a long history of supplying high quality power transistors in large volume to the military, automotive, consumer, industrial and computer markets. Being the leading supplier of power transistors in the world, we strive to serve our customers' needs to maintain our leadership

position.

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Chapter 1: Introduction to Power MOSFETs

Symbols, Terms and Definitions

The following are the most commonly used letter symbols, terms and definitions associated with Power MOSFETs.

Symbol	The inemial resistance (steady-state) from the ductor junction(s) to the ambient.	Definition
Cds	drain-source capacitance	The capacitance between the drain and source terminals with the gate terminal connected to the guard terminal of a three-terminal bridge.
C _{dq}	drain-gate capacitance	The same as C _{rss} — See C _{rss} .
Cgs ns ni ,s	gate-source capacitance	The capacitance between the gate and source terminals with the drain terminal connected to the guard terminal of a three-terminal bridge.
C _{iss}	short-circuit input capacitance,	The capacitance between the input terminals (gate and source) with the drain short-circuited to the source for alternating current. (Ref. IEEE No. 255)
C _{OSS}	short-circuit output capacitance, common-source	The capacitance between the output terminals (drain and source) with the gate short-circuited to the source for alternating current. (Ref. IEEE No. 255)
C _{rss}	short-circuit reverse transfer capacitance, common-source	The capacitance between the drain and gate terminals with the source connected to the guard terminal of a three- terminal bridge.
9FS	common-source large-signal transconductance	The ratio of the change in drain current due to a change in gate-to-source voltage
ID .*(1 elel	drain current, dc	The direct current into the drain terminal.
ID(on)	on-state drain current	The direct current into the drain terminal with a specified forward gate-source voltage applied to bias the device to the on-state.
IDSS -riotiwa ei ta pnitoubnoor	zero-gate-voltage drain current left sooige ift solog lugni as doubly ganub levisine emit ent non s of gate-ubroo s most observed ent gate as sources.	The direct current into the drain terminal when the gate- source voltage is zero. This is an on-state current in a depletion-type device, an off-state in an enhancement-type device.
	gate current, dc	The direct current into the gate terminal.
IGSS	reverse gate current, drain short-circuited to source	The direct current into the gate terminal of a junction-gate field-effect transistor when the gate terminal is reverse biased with respect to the source terminal and the drain terminal is short-circuited to the source terminal.

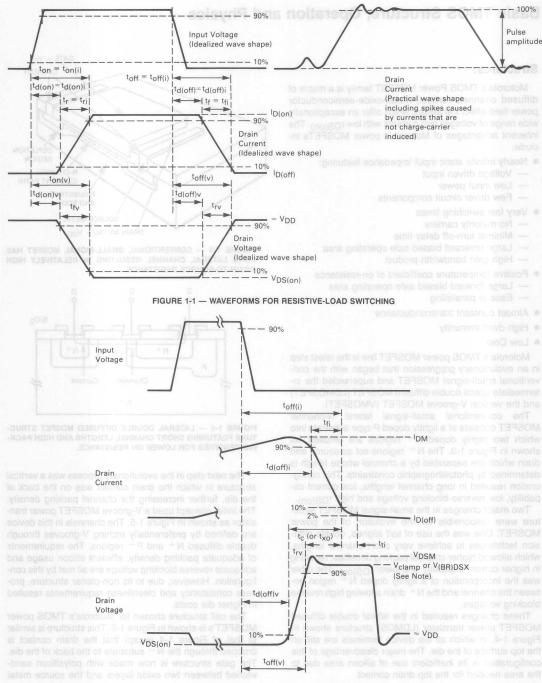
Symbol	Term	Definition
lgssf	forward gate current, drain short-circuited to source	The direct current into the gate terminal of an insulated- gate field-effect transistor with a forward gate-source volt- age applied and the drain terminal short-circuited to the source terminal.
IGSSR	reverse gate current, drain short-circuited to source	The direct current into the gate terminal of an insulated- gate field-effect transistor with a reverse gate-source volt- age applied and the drain terminal short-circuited to the source terminal.
Is	source current, dc	The direct current into the source terminal.
P _T , P _D	total nonreactive power input to all terminals	The sum of the products of the dc input currents and voltages.
Q_g	total gate charge	The total gate charge required to charge the MOSFETs input capacitance to $V_{GS(on)}$.
rDS(on)	static drain-source on-state resistance	The dc resistance between the drain and source terminals with a specified gate-source voltage applied to bias the device to the on state.
$R_{\theta}CA$	thermal resistance, case-to-ambient	The thermal resistance (steady-state) from the device case to the ambient.
R_{θ} JA	thermal resistance, junction-to-ambient	The thermal resistance (steady-state) from the semiconductor junction(s) to the ambient.
R _θ JC	thermal resistance, junction-to-case	The thermal resistance (steady-state) from the semiconductor junction(s) to a stated location on the case.
$R_{ hetaJM}$	thermal resistance, junction-to-mounting surface	The thermal resistance (steady-state) from the semiconductor junction(s) to a stated location on the mounting surface.
TA inimel sour	ambient temperature or free-air temperature	The air temperature measured below a device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.
ne source of	case temperature	The temperature measured at a specified location on the case of a device.
	turn-off crossover time and some sources with the source alternating oursent. (Ret IEEE No. 255) The department between the drain and gate	The time interval during which drain voltage rises from 10% of its peak off-state value and drain current falls to 10% of its peak on-state value, in both cases ignoring spikes that are not charge-carrier induced.
al of a threeT	channel temperature	The temperature of the channel of a field-effect transistor.
T _{stg}	storage temperature	The temperature at which the device, without any power applied, may be stored.
td(off)	turn-off delay time	Synonym for current turn-off delay time (see Note 1)*.
td(off)i	Current turn-off delay time The direct current voltage applied to biase the on-state. The direct current into the drain terminal w	The interval during which an input pulse that is switching the transistor from a conducting to a nonconducting state falls from 90% of its peak amplitude and the drain current waveform falls to 90% of its on-state amplitude, ignoring spikes that are not charge-carrier induced.
	voltage turn-off delay time payt-noteleeb eoveb	The time interval during which an input pulse that is switching the transistor from a conducting to a nonconducting state falls from 90% of its peak amplitude and the drain voltage waveform rises to 10% of its off-state amplitude, ignoring spikes that are not charge-carrier induced.
	turn-on delay time was a same to site blait	Synonym for current turn-on delay time (see Note 1)*.

ased with respect to the source terminal and the drain ter-

Symbol	Term	Definition	Definition	mieT	Symbol
point on fine the control of the wayer with respect	Officurrent turn-on delay time solutions of the control of the con		The time interval during whing the transistor from a state rises from 10% of its current waveform rises to ignoring spikes that are no	nonconducting to a s peak amplitude ar 10% of its on-state	conducting nd the drain amplitude,
^t d(on)v	voltage turn-on delay time		The time interval during whing the transistor from a state rises from 10% of its voltage waveform falls to ignoring spikes that are no	nonconducting to a s peak amplitude at 90% of its off-state	conducting nd the drain amplitude,
t _f betsoibni	fall time wolled as nexted tonce		Synonym for current fall tir	me (See Note 1)*.	
tfilloeqs s	current fall time		The time interval during w from 90% to 10% of its pea that are not charge-carrier	k off-state value, ign	-
t _{fv}	voltage fall time		The time interval during w from 90% to 10% of its pea that are not charge-carrier	k off-state value, ign	-
toff sqa s r	ipuoturn-off time soupe and of be		Synonym for current turn-	off time (see Note 1	Vegras.v(
toff(i)	current turn-off time		The sum of current turn-off i.e., td(off)i + tfi.	f delay time and curr	
toff(v)	voltage turn-off time		The sum of voltage turn-time, i.e., td(off)v + trv-	off delay time and	
ton me beild	turn-on time		Synonym for current turn-	on time (See Note 1	V(8R)G\$*(
ton(i)	of a current turn-on time had a la		The sum of current turn-on	delay time and curre	ent rise time,
ton(v)	voltage turn-on time illme age		The sum of voltage turn-on i.e., td(on)v + tfv.	n delay time and volta	age fall time,
d by the sqt	of the relevantion merela and the polarity a property and the polarity and the first subscript).		The time interval between edge of a pulse waveforn trailing edge of the same	m and a reference	
			Note: The two reference points a plitude of the waveform existing respect to the steady-state ampli the reference points are 50% p pulse duration should be used.	after the leading edge, itude existing before the	measured with leading edge. If
t _r	rise time		Synonym for current rise t	ime (See Note 1)*.	
e field-efford ow value.	the dollar course time to the total course time time time time time time time tim		The time interval during w from 10% to 90% of its pea that are not charge-carrier	ak on-state value, ign	_
^t rv	voltage rise time admission of the second of		The time interval during w from 10% to 90% of its pea that are not charge-carrier	ak off-state value, igr	
	to a stated location on the case, current tail time "" and "has time" always refer to the characteristic state to the characteristic state to the characteristic state of the considered agual tail time may be considered agual to the characteristic state of the characteristic state		induced. Pebodico bas laures	from 10% to 2% of kes that are not ch	during which its peak on- narge-carrier

Symbol	Term notified	Definition meT lodmy2
e conducting and the drain tate amplitude induced. e that is switch	The time interval noiserub sellud epareval ing the translator from a nonconducting to state rises from 10% of its peak amplitude ourself wavefrom rises to 10% of its one ignoring spikes that are not charge-carrier. The time interval during which an input puls ing the translator from a nonconducting the	The time interval between a reference point on the leading edge of a pulse waveform and a reference point on the trailing edge of the same waveform, with both reference points being 50% of the steady-state amplitude of the waveform existing after the leading edge, measured with respect to the steady-state amplitude existing before the leading edge.
		Note: If the reference points are not 50% points, the symbol $\rm t_p$ and term pulse duration should be used.
V(BR)DSR	drain-source breakdown voltage with (resistance between gate and source)	The breakdown voltage between the drain terminal and the source terminal when the gate terminal is (as indicated by the last subscript letter) as follows:
		R = returned to the source terminal through a specified resistance.
V(BR)DSS	gate short-circuited to source	S = short-circuited to the source terminal.
V _(BR) DSV	voltage between gate and source	V = returned to the source terminal through a specified voltage.
V _{(BR)DSX}	circuit between gate and source months are source months and source months and source months are source monthing are source months are source months are source months are sou	X = returned to the source terminal through a specified circuit.
V _(BR) GSSF	forward gate-source breakdown voltage	The breakdown voltage between the gate and source terminals with a forward gate-source voltage applied and the drain terminal short-circuited to the source terminal.
V(BR)GSSR	reverse gate-source breakdown voltage	The breakdown voltage between the gate and source terminals with a reverse gate-source voltage applied and the drain terminal short-circuited to the source terminal.
V _{DD} , V _{GG} V _{SS}	voltago	The dc supply voltage applied to a circuit or connected to the reference terminal in no-mul applies (v) applies
VDG VDS VGD VGS VSD VSG	drain-to-gate drain-to-source gate-to-drain gate-to-source source-to-drain source-to-gate	The dc voltage between the terminal indicated by the firs subscript and the reference terminal indicated by the sec ond subscript (stated in terms of the polarity at the termina indicated by the first subscript).
V _{DS} (on)	drain-source on-state voltage	The voltage between the drain and source terminals with a specified forward gate-source voltage applied to bias the device to the on state.
VGS(th)	gate-source threshold voltage	The forward gate-source voltage at which the magnitude of the drain current of an enhancement-type field-effectransistor has been increased to a specified low value.
$Z_{\theta JA(t)}$	transient thermal impedance, junction-to-ambient	The transient thermal impedance from the semiconducto junction(s) to the ambient.
$Z_{\theta JC(t)}$	transient thermal impedance, junction-to-case	The transient thermal impedance from the semiconductor junction(s) to a stated location on the case.

Note 1: As names of time intervals for characterizing switching transistors, the terms "fall time" and "rise time" always refer to the change that is taking place in the magnitude of the output current even though measurements may be made using voltage waveforms. In a purely resistive circuit, the (current) rise time may be considered equal and coincident to the voltage fall time and the (current) fall time may be considered equal and coincident to the voltage rise time. The delay times for current and voltage will be equal and coincident. When significant amounts of inductance are present in a circuit, these equalities and coincidences no longer exist, and use of the unmodified terms delay time, fall time, and rise time must be avoided.



NOTE: V_{clamp} (in a clamped inductive-load switching circuit) or V_{(BR)DSX} (in an unclamped circuit) is the peak off-state voltage excluding spikes.

FIGURE 1-2 — WAVEFORMS FOR INDUCTIVE LOAD SWITCHING, TURN-OFF

Basic TMOS Structure, Operation and Physics

Structures:

Motorola's TMOS Power MOSFET family is a matrix of diffused channel, vertical, metal-oxide-semiconductor power field-effect transistors which offer an exceptionally wide range of voltages and currents with low rDS(on). The inherent advantages of Motorola's power MOSFETs include:

- Nearly infinite static input impedance featuring:
 - Voltage driven input
 - Low input power
 - Few driver circuit components
- Very fast switching times
 - No minority carriers
 - Minimal turn-off delay time
 - Large reversed biased safe operating area
 - High gain bandwidth product
- Positive temperature coefficient of on-resistance
- Large forward biased safe operating area
- Ease in paralleling
- Almost constant transconductance
- · High dv/dt immunity
- Low Cost

Motorola's TMOS power MOSFET line is the latest step in an evolutionary progression that began with the conventional small-signal MOSFET and superseded the intermediate lateral double diffused MOSFET (LDMOSFET) and the vertical V-groove MOSFET (VMOSFET).

The conventional small-signal lateral N-channel MOSFET consists of a lightly doped P-type substrate into which two highly doped N+ regions are diffused, as shown in Figure 1-3. The N+ regions act as source and drain which are separated by a channel whose length is determined by photolithographic constraints. This configuration resulted in long channel lengths, low current capability, low reverse blocking voltage and high rpS(on).

Two major changes in the small-signal MOSFET structure were responsible for the evolution of the power MOSFET. One was the use of self aligned, double diffusion techniques to achieve very short channel lengths, which allowed higher channel packing densities, resulting in higher current capability and lower $r_{\mbox{DS}(\mbox{on})}$. The other was the incorporation of a lightly doped N $^+$ region between the channel and the N $^+$ drain allowing high reverse blocking voltages.

These changes resulted in the lateral double diffused MOSFET power transistor (LDMOS) structure shown in Figure 1-4, in which all the device terminals are still on the top surface of the die. The major disadvantage of this configuration is its inefficient use of silicon area due to the area needed for the top drain contact.

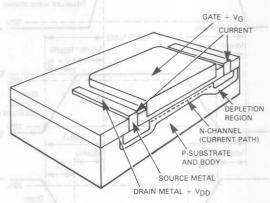


FIGURE 1-3 — CONVENTIONAL SMALL-SIGNAL MOSFET HAS LONG LATERAL CHANNEL RESULTING IN RELATIVELY HIGH DRAIN-TO-SOURCE RESISTANCE.

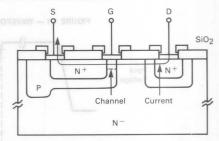


FIGURE 1-4 — LATERAL DOUBLE DIFFUSED MOSFET STRUCTURE FEATURING SHORT CHANNEL LENGTHS AND HIGH PACKING DENSITIES FOR LOWER ON RESISTANCE.

The next step in the evolutionary process was a vertical structure in which the drain contact was on the back of the die, further increasing the channel packing density. The initial concept used a V-groove MOSFET power transistor as shown in Figure 1-5. The channels in this device are defined by preferentially etching V-grooves through double diffused N + and P - regions. The requirements of adequate packing density, efficient silicon usage and adequate reverse blocking voltage are all met by this configuration. However, due to its non-planar structure, process consistency and cleanliness requirements resulted in higher die costs.

The cell structure chosen for Motorola's TMOS power MOSFET's is shown in Figure 1-6. This structure is similar to that of Figure 1-4 except that the drain contact is dropped through the N - substrate to the back of the die. The gate structure is now made with polysilicon sandwiched between two oxide layers and the source metal

applied continuously over the entire active area. This two layer electrical contact gives the optimum in packing density and maintains the processing advantages of planar LDMOS. This results in a highly manufacturable process which yields low $r_{DS(0n)}$ and high voltage product.

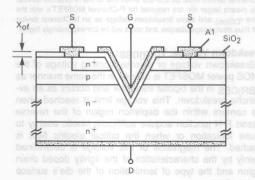


FIGURE 1-5 — V-GROOVE MOSFET STRUCTURE HAS SHORT VERTICAL CHANNELS WITH LOW DRAIN-TO-SOURCE RESISTANCE.

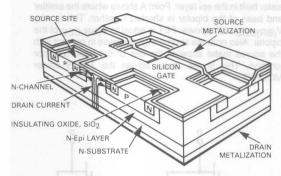


FIGURE 1-6 — TMOS POWER MOSFET STRUCTURE OFFERS VERTICAL CURRENT FLOW, LOW RESISTANCE PATHS AND PERMITS COMPACT METALIZATION ON TOP AND BOTTOM SURFACES TO REDUCE CHIP SIZE.

Operation:

Transistor action and the primary electrical parameters of Motorola's TMOS power MOSFET can be defined as follows:

Drain Current, In:

When a gate voltage of appropriate polarity and magnitude is applied to the gate terminal, the polysilicon gate induces an inversion layer at the surface of the diffused channel region represented by rCH in Figure 1-7 (page A-8). This inversion layer or channel connects the source to the lightly doped region of the drain and current begins to flow. For small values of applied drain-to-source voltage, VDS, drain current increases linearly and can be represented by Equation (1).

(1)
$$I_D \approx \frac{Z}{I} \mu Co [V_{GS} - V_{GS(th)}] V_{DS}$$

As the drain voltage is increased, the drain current saturates and becomes proportional to the square of the applied gate-to-source voltage, V_{GS} , as indicated in Equation (2).

(2) ID
$$\approx \frac{Z}{2L} \, \mu \text{Co} \, [\text{V}_{GS} - \text{V}_{GS(th)}]^2$$

Where $\mu = \text{Carrier Mobility}$

Co = Gate Oxide Capacitance per unit area

Z = Channel Width

L = Channel Length

These values are selected by the device design engineer to meet design requirements and may be used in modeling and circuit simulations. They explain the shape of the output characteristics discussed in Chapter 2.

Transconductance, ges:

The transconductance or gain of the TMOS power MOSFET is defined as the ratio of the change in drain current and an accompanying small change in applied gate-to-source voltage and is represented by Equation (3).

(3)
$$g_{FS} = \frac{\Delta ID(sat)}{\Delta V_{GS}} = \frac{Z}{L} \mu Co [V_{GS}-V_{GS}(th)]$$

The parameters are the same as above and demonstrate that drain current and transconductance are directly related and are a function of the die design. Note that transconductance is a linear function of the gate voltage, an important feature in amplifier design.

Threshold Voltage, VGS(th)

Threshold voltage is the gate-to-source voltage required to achieve surface inversion of the diffused channel region, (r_{CH} in Figure 1-7 page A-8) and as a result, conduction in the channel.

As the gate voltage increases the more the channel is "enhanced," or the lower its resistance (r_{CH}) is made, the more current will flow. Threshold voltage is measured at a specified value of current to maintain measurement correlations. A value of 1.0 mA is common throughout the industry. This value is primarily a function of the gate oxide thickness and channel doping level which are chosen during the die design to give a high enough value to keep the device off with no bias on the gate at high temperatures. A minimum value of 1.5 volts at room temperature will guarantee the transistor remains an enhancement mode device at junction temperatures up to 150°C.

On-Resistance, rps(on):

On-resistance is defined as the total resistance encountered by the drain current as it flows from the drain terminal to the source terminal. Referring to Figure 1-7, rDS(on) is composed primarily of four resistive components associated with:

The Inversion channel, r_{CH} ; the Gate-Drain Accumulation Region, r_{ACC} ; the junction FET Pinch region, r_{JFET} ; and the lightly doped Drain Region, r_{D} , as indicated in Equation (4).

(4)
$$rDS(on) = rCH + rACC + rJFET + rD$$

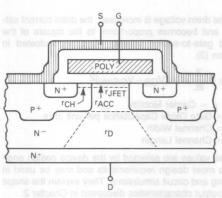


FIGURE 1-7 — TMOS DEVICE ON-RESISTANCE

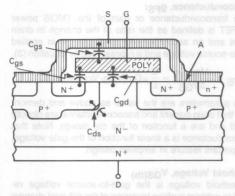


FIGURE 1-8 — TMOS DEVICE PARASITIC CAPACITANCES

Whereas the channel resistance increases with channel length, the accumulation resistance increases with poly width and the JFET pinch resistance increases with epi resistivity and all three are inversely proportional to the channel width and gate-to-source voltage. The drain resistance is proportional to the epi resistivity, poly width and inversely proportional to channel width. This says that the on-resistance of TMOS power FETs with the thick and high resistivity epi required for high voltage parts will be dominated by rp.

Low voltage devices have thin, low resistivity epi and r_{CH} will be a large portion of the total on-resistance. This is why high voltage devices are "full on" with moderate voltages on the gate, whereas with low voltage devices

the on-resistance continues to decrease as VGS is increased toward the maximum rating of the device.

Note: rDS(on) is inversely proportional to the carrier mobility. This means that the rDS(on) of the P-Channel MOSFET is approximately 2.5 to 3.0 times that of a similar N-Channel MOSFET. Therefore, in order to have matched complementary on characteristics, the Z/L ratio of the P-Channel device must be 2.5–3.0 times that of the N-Channel device. This means larger die are required for P-Channel MOSFET's with the same rDS(on) and same breakdown voltage as an N-Channel device and thus device capacitances and costs will be correspondingly higher.

Breakdown Voltage, V(BR)DSS:

Breakdown voltage or reverse blocking voltage of the TMOS power MOSFET is defined in the same manner as V(BR)CES in the bipolar transistor and occurs as an avalanche breakdown. This voltage limit is reached when the carriers within the depletion region of the reverse biased P-N junction acquire sufficient kinetic energy to cause ionization or when the critical electric field is reached. The magnitude of this voltage is determined mainly by the characteristics of the lightly doped drain region and the type of termination of the die's surface electric field.

Figure 1-9 shows a schematic representation of the cross-section in Figure 1-8 and depicts the bipolar transistor built in the epi layer. Point A shows where the emitter and base of the bipolar is shorted together. This is why V(BR)DSS of the power FET is equal to V(BR)CES of the bipolar. Also note the short brings the base in contact with the source metal allowing the use of the base-collector junction. This is the diode across the TMOS power MOSFET.

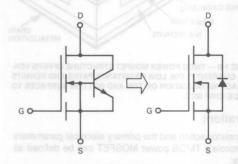


FIGURE 1-9 — SCHEMATIC DIAGRAM OF ALL THE COMPONENTS OF THE CROSS SECTION OF FIGURE 1-7.

TMOS Power MOSFET Capacitances:

Two types of intrinsic capacitances occur in the TMOS power MOSFET — those associated with the MOS structure and those associated with the P-N junction.

The two MOS capacitances associated with the MOS-FET cell are:

Gate-Source Capacitance, C_{gS} Gate-Drain Capacitance, C_{qd}

The magnitude of each is determined by the die geometry and the oxides associated with the silicon gate.

The P-N junction formed during fabrication of the power MOSFET results in the drain-to-source capacitance, C_{ds} . This capacitance is defined the same as any other planar junction capacitance and is a direct function of the channel drain area and the width of the reverse biased junction depletion region.

The dielectric insulator of C_{gs} and C_{gd} is basically a glass. Thus these are very stable capacitors and will not vary with voltage or temperature. If excessive voltage is placed on the gate, breakdown will occur through the

glass, creating a resistive path and destroying MOSFET operation.

Optimizing TMOS Geometry:

The geometry and packing density of Motorola's MOSFETs vary according to the magnitude of the reverse blocking voltage.

The geometry of the source site, as well as the spacing between source sites, represents important factors in efficient power MOSFET design. Both parameters determine the channel packing density, i.e.: ratio of channel width per cell to cell area.

For low voltage devices, channel width is crucial for minimizing $r_{DS(on)}$, since the major contributing component of $r_{DS(on)}$ is r_{CH} . However, at high voltages, the major contributing component of resistance is r_{D} and thus minimizing $r_{DS(on)}$ is dependent on maximizing the ratio of active drain area per cell to cell area. These two conditions for minimizing $r_{DS(on)}$ cannot be met by a single geometry pattern for both low and high voltage devices.

Distinct Advantages of Power MOSFETs

Power MOSFETs offer unique characteristics and capabilities that are not available with bipolar power transistors. By taking advantage of these differences, overall systems cost savings can result without sacrificing reliability.

Speed

Power MOSFETs are majority carrier devices, therefore their switching speeds are inherently faster. Without the minority carrier stored base charge common in bipolar transistors, storage time is eliminated. The high switching speeds allow efficient switching at higher frequencies which reduces the cost, size and weight of reactive components

MOSFET switching speeds are primarily dependent on charging and discharging the device capacitances and are essentially independent of operating temperature.

Input Characteristics

The gate of a power MOSFET is electrically isolated from the source by an oxide layer that represents a do resistance greater than 40 megohms. The devices are fully biased-on with a gate voltage of 10 volts. This significantly simplifies the drive circuits and in many instances the gate may be driven directly from logic integrated circuits such as CMOS and TTL to control high power circuits directly.

Since the gate is isolated from the source, the drive requirements are nearly independent of the load current. This reduces the complexity of the drive circuit and results in overall system cost reduction.

Safe Operating Area

Power MOSFETs, unlike bipolars, do not require de-

rating of power handling capability as a function of applied voltage. The phenomena of second breakdown does not occur within the ratings of the device. Depending on the application, snubber circuits may be eliminated or a smaller capacitance value may be used in the snubber circuit. The safe operating boundaries are limited by the peak current ratings, breakdown voltages and the power capabilities of the devices.

On-Voltage

The minimum on-voltage of a power MOSFET is determined by the device on-resistance rDS(on). For low voltage devices the value of rDS(on) is extremely low, but with high voltage devices the value increases. rDS(on) has a positive temperature coefficient which aids in paralleling devices.

Examples of Advantages Offered by MOSFETs

High Voltage Flyback Converter business augus MW9 ed

An obvious way of showing the advantages of power MOSFETs over bipolars is to compare the two devices in the same system. Since the drive requirements are not the same, it is not a question of simply replacing the bipolar with the FET, but one of designing the respective drive circuits to produce an equivalent output, as described in Figures 1-10 and 1-11.

For this application, a peak output voltage of about 700 V driving a 30 k Ω load $(P_{O(pk)} \approx$ 16 W) was required. With the component values and timing shown, the inductor/device current required to generate this flyback voltage would have to ramp up to about 3.0 A.

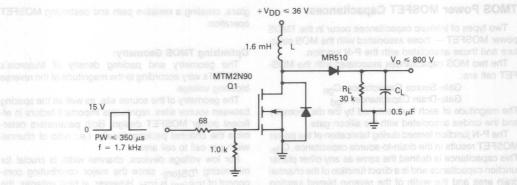


FIGURE 1-10 — TMOS OUTPUT STAGE

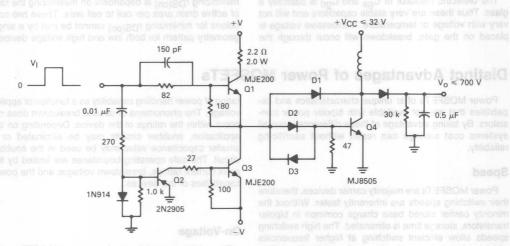


FIGURE 1-11 — BIPOLAR DRIVER AND OUTPUT STAGE

FIGURES 1-10 AND 1-11 — CIRCUIT CONFIGURATIONS FOR A TMOS AND
BIPOLAR OUTPUT STAGE OF A HIGH VOLTAGE FLYBACK CONVERTER
BIPOLAR OUTPUT STAGE OF A HIGH VOLTAGE FLYBACK CONVERTER

Figure 1-10 shows the TMOS version. Because of its high input impedance, the FET, an MTM2N90, can be directly driven from the pulse width modulator. However, the PWM output should be about 15 volts in amplitude and for relatively fast FET switching be capable of sourcing and sinking 100 mA. Thus, all that is required to drive the FET is a resistor or two. The peak drain current of 3.2 A is within the MTM2N90 pulsed current rating of 7.0 A (2.0 A continuous), and the turn-off load line of 3.2 A, 700 V is well within the Switching SOA (7.0 A, 900 V) of the device. Thus, the circuit demonstrates the advantages of TMOS:

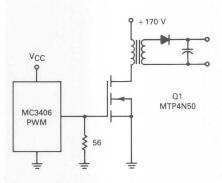
- High input impedance
- Fast Switching
- No Second breakdown junds of gu grass of even blue

Compare this circuit with the bipolar version of Figure 1-11.

To achieve the output voltage, using a high voltage Switchmode MJ8505 power transistor, requires a rather complex drive circuit for generating the proper I_{B1} and I_{B2}. This circuit uses three additional transistors (two of which are power transistors), three Baker clamp diodes, eleven passive components and a negative power supply for generating an off-bias voltage. Also, the RBSOA capability of this device is only 3.0 A at 900 V and 4.7 A at 800 V, values below the 7.0 A, 900 V rating of the MOSFET. A detailed description of these circuits is shown in Chapter 7, TMOS applications.

20 kHz Switcher

An example of TMOS advantage over bipolar that il-



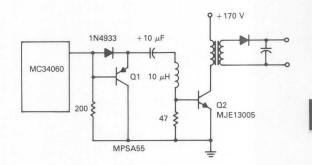


FIGURE 1-12 — TMOS VERSION

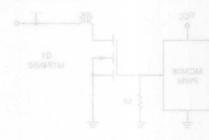
FIGURE 1-13 — BIPOLAR VERSION

FIGURES 1-12 AND 1-13 — COMPARISON OF TMOS versus BIPOLAR IN THE POWER OUTPUT STAGE OF A 20 kHz SWITCHER

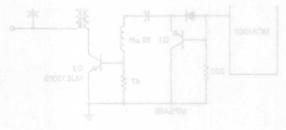
lustrates its superior switching speed is shown in the power output section of Figures 1-12 and 1-13. In addition to the drive simplicity and reduced component count, the faster switching speed offers better circuit efficiency. For this 35 W switching regulator, using the same small heatink for either device, a case temperature rise of only 18°C was measured for the MTP4N50 power MOSFET compared to a 46°C rise for the MJE13005 bipolar transistor.

Although the saturation losses were greater for the TMOS, its lower switching losses predominated, resulting in a more efficient switching device. A more detailed description of this Switcher is shown in Chapter 9.

In general, at low switching frequencies, where static losses predominate, bipolars are more efficient. At higher frequencies, above 30 kHz to 100 kHz, the power MOS-FETs are more efficient.



PICHER 1.12 ... THOS VERSION



IQUINE 1-13 - BIPOLAR VERSION

FIGURES 1-12 AND 1-13 — COMPARISON OF TMOS VERSUS BIPOLAR IN THE POWER OUTPUT STAGE OF A 20 MHz SWITCHER

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Chapter 2: Basic Characteristics of Power MOSFETs

Output Characteristics

Perhaps the most direct way to become familiar with the basic operation of a device is to study its output characteristics. In this case, a comparison of the MOSFET characteristics with those of a bipolar transistor with similar ratings is in order, since the curves of a bipolar device are almost universally familiar to power circuit design engineers.

As indicated in Figures 2-1 and 2-2, the output characteristics of the power MOSFET and the bipolar transistor can be divided similarly into two basic regions. The figures also show the numerous and often confusing terms assigned to those regions. To avoid possible confusion, this section will refer to the MOSFET regions as the "on" (or "ohmic") and "active" regions and bipolar regions as the "saturation" and "active" regions.

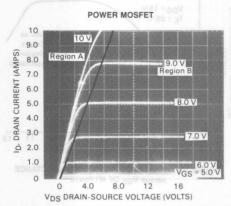


FIGURE 2-1 — ID-VDS TRANSFER CHARACTERISTICS OF MTP8N15. REGION A IS CALLED THE OHMIC, ON, CONSTANT RESISTANCE OR LINEAR REGION. REGION B IS CALLED THE ACTIVE, CONSTANT CURRENT, OR SATURATION REGION.

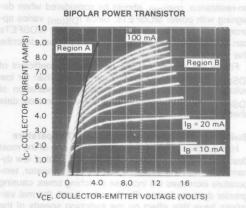


FIGURE 2-2 — I_C-V_{CE} TRANSFER CHARACTERISTICS OF MJE15030 (NPN, I_C CONTINUOUS = 8.0 A, V_{CEO} = 150 V) REGION A IS THE SATURATION REGION. REGION B IS THE LINEAR OR ACTIVE REGION.

One of the three obvious differences between Figures 2-1 and 2-2 is the family of curves for the power MOSFET is generated by changes in gate voltage and not by base current variations. A second difference is the slope of the curve in the bipolar saturation region is steeper than the slope in the ohmic region of the power MOSFET indicating that the on-resistance of the MOSFET is higher than the effective on-resistance of the bipolar.

The third major difference between the output characteristics is that in the active regions the slope of the bipolar curve is steeper than the slope of the TMOS curve, making the MOSFET a better constant current source. The limiting of ID is due to pinch-off occurring in the MOSFET channel.

Basic MOSFET Parameters

On-Resistance

The on-resistance, or rDS(on), of a power MOSFET is an important figure of merit because it determines the amount of current the device can handle without excessive power dissipation. When switching the MOSFET from off to on, the drain-source resistance falls from a very high value to rDS(on), which is a relatively low value. To minimize rDS(on) the gate voltage should be large enough for a given drain current to maintain operation in the ohmic region. Data sheets usually include a graph, such as Figure 2-3, which relates this information. As Figure 2-4 indicates, increasing the gate voltage above 12 volts has a diminishing effect on lowering on-resistance (especially in high voltage devices) and increases the possibility of spurious gate-source voltage spikes exceeding the maximum gate voltage rating of 20 volts. Somewhat like driving a bipolar transistor deep into saturation, unnecessarily high gate voltages will increase turn-off time because of the excess charge stored in the input capacitance. All Motorola TMOS FETs will conduct the rated continuous drain current with a gate voltage of 10 volts.

As the drain current rises, especially above the continuous rating, the on-resistance also increases. Another important relationship, which is addressed later with the other temperature dependent parameters, is the effect that temperature has on the on-resistance. Increasing T_J and I_D both effect an increase in $r_{DS(on)}$ as shown in Figure 2-5.

Transconductance of huoms lisms believed a doirly is

Since the transconductance, or gFS, denotes the gain of the MOSFET, much like beta represents the gain of the bipolar transistor, it is an important parameter when the device is operated in the active, or constant current, region. Defined as the ratio of the change in drain current corresponding to a change in gate voltage (gFS = dIp/dVGS), the transconductance varies with operating conditions as seen in Figure 2-6. The value of gFS is determined from the active portion of the VpS-Ip transfer characteristics where a change in VpS no longer significantly influences gFS. Typically the transconductance rating is specified at half the rated continuous drain current and at a VpS of 15 V.

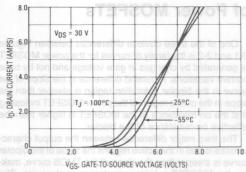


FIGURE 2-3 — TRANSFER CHARACTERISTICS OF MTP4N50

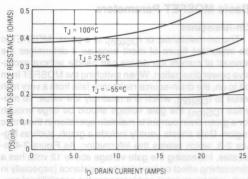


FIGURE 2-5 — VARIATION OF rDS(on) WITH DRAIN CURRENT AND TEMPERATURE FOR MTM15N45

For designers interested only in switching the power MOSFET between the on and off states, the transconductance is often an unused parameter. Obviously when the device is switched fully on, the transistor will be operating in its ohmic region where the gate voltage will be high. In that region, a change in an already high gate voltage will do little to increase the drain current; therefore, gFS is almost zero.

Threshold Voltage

Threshold Voltage, VGS(th), is the lowest gate voltage at which a specified small amount of drain current begins to flow. Motorola normally specifies VGS(th) at an ID of one milliampere. Device designers can control the value of the threshold voltage and target VGS(th) to optimize device performance and practicality. A low threshold voltage is desired so the TMOS FET can be controlled by low voltage chips such as CMOS and TTL. A low value also speeds switching because less current needs to be transferred to charge the parasitic input capacitances. But the threshold voltage can be too low if noise can trigger the device. Also, a positive-going voltage transient on the drain can be coupled to the gate by the gate-to-drain parasitic capacitance and can cause spurious turn-on of a device with a low VGS(th).

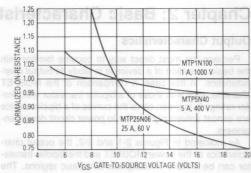


FIGURE 2-4 — THE EFFECT OF GATE-TO-SOURCE
VOLTAGE ON ON-RESISTANCE VARIES WITH A DEVICE'S
VOLTAGE RATING

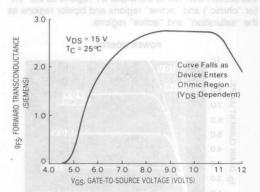


FIGURE 2-6 — SMALL-SIGNAL TRANSCONDUCTANCE versus V_{GS} OF MTP8N10

Temperature Dependent Characteristics ^rDS(on)

Junction temperature variations and their effect on the on-resistance, rDS(on), should be considered when designing with power MOSFETs. Since rDS(on) varies approximately linearly with temperature, power MOSFETs can be assigned temperature coefficients that describe this relationship.

Figure 2-7 shows that the temperature coefficient of rDS(on) is greater for high voltage devices than for low voltage MOSFETs. A graph showing the variation of rDS(on) with junction temperature is shown on most data sheets

Switching Speeds are Constant with Temperature

High junction temperatures emphasize one of the most desirable characteristics of the MOSFET, that of low dynamic or switching losses. In the bipolar transistor, temperature increases will increase switching times, causing greater dynamic losses. On the other hand, thermal variations have little effect on the switching speeds of the power MOSFET. These speeds depend on how rapidly the parasitic input capacitances can be charged and discharged. Since the magnitudes of these capacitances are

essentially temperature invariant, so are the switching speeds. Therefore, as temperature increases, the dynamic losses in a MOSFET are low and remain constant, while in the bipolar transistors the switching losses are higher and increase with junction temperature.

Drain-To-Source Breakdown Voltage

The drain-to-source breakdown voltage is a function of the thickness and resistivity of a device's N-epitaxial region. Since that resistivity varies with temperature, so does V(BR)DSS. As Figure 2-8 indicates, a 100°C rise in junction temperature causes a V(BR)DSS to increase by about 10%. However, it should also be remembered that the actual V(BR)DSS falls at the same rate as T_J decreases.

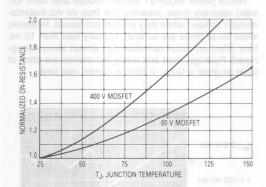


FIGURE 2-7 — THE INFLUENCE OF JUNCTION TEMPERATURE ON ON-RESISTANCE VARIES WITH BREAKDOWN VOLTAGE

Threshold Voltage

The gate voltage at which the MOSFET begins to conduct, the gate-threshold voltage, is temperature dependent. The variation with T_J is linear as shown on most data sheets. Having a negative temperature coefficient, the threshold voltage falls about 10% for each 45°C rise in the junction temperature.

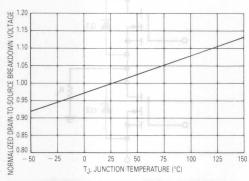


FIGURE 2-8 — TYPICAL VARIATION OF DRAIN-TO-SOURCE BREAKDOWN VOLTAGE WITH JUNCTION TEMPERATURE

Importance of T_{J(max)} and Heat Sinking

Two of the packages that commonly house the TMOS die are the TO-220AB and the TO-204. The power ratings of these packages range from 40 to 250 watts depending on the die size and the type of materials used in construction. These ratings are nearly meaningless, however, unless some heat sinking is provided. Without heat sinking the TO-204 and the TO-220 can dissipate only about 4.0 and 2.0 watts respectively, regardless of the die size.

Because long term reliability decreases with increasing junction temperature, TJ should not exceed the maximum rating of 150°C. Steady-state operation above 150°C also invites abrupt and catastrophic failure if the transistor experiences additional transient thermal stresses. Excluding the possibility of thermal transients, operating below the rated junction temperature can enhance reliability. A $T_{J(max)}$ of 150°C is normally chosen as a safe compromise between long term reliability and maximum power dissipation.

In addition to increasing the reliability, proper heat sinking can reduce static losses in the power MOSFET by decreasing the on-resistance. $r_{DS(on)}$, with its positive temperature coefficient, can vary significantly with the quality of the heat sink. Good heat sinking will decrease the junction temperature, which further decreases $r_{DS(on)}$ and the static losses.

Drain-Source Diode

Inherent in most power MOSFETs, and all TMOS transistors, is a "parasitic" drain-source diode. Figure 2-9, the illustration of cross section of the TMOS die, shows the P-N junction formed by the P-well and the N-Epi layer. Because of its extensive junction area, the current ratings of the diode are the same as the MOSFET's continuous and pulsed current ratings. For the N-Channel TMOS FET shown in Figure 2-10, this diode is forward biased when the source is at a positive potential with respect to the drain. Since the diode may be an important circuit element, Motorola Designer's Data Sheets specify typical values of the forward on-voltage, forward turn-on and reverse recovery time. The forward characteristics of the drain-source diodes of several TMOS power MOSFETs are shown in Figure 2-11.

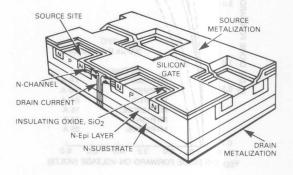


FIGURE 2-9 — CROSS SECTION OF TMOS CELL

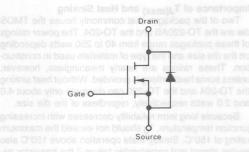


FIGURE 2-10 — N-CHANNEL POWER MOSFET SYMBOL INCLUDING DRAIN-SOURCE DIODE

Most rectifiers, a notable exception being the Schottky diode, exhibit a "reverse recovery" characteristic as depicted in Figure 2-12. When forward current flows in a standard diode, a carrier gradient is formed in the high resistivity side of the junction resulting in an apparent storage of charge. Upon sudden application of a reverse bias, the stored charge temporarily produces a negative current flow during the reverse recovery time, or t_{rr}, until the charge is depleted. The circuit conditions that influence t_{rr} and the stored charge are the forward current magnitude and the rate of change of current from the forward current magnitude to the reverse current peak. When tested under the same circuit conditions, the parasitic drain-source diode of a TMOS transistor has a t_{rr} similar to that of a fast recovery rectifier.

In many applications, the drain-source diode is never forward biased and does not influence circuit operation. However, in multi-transistor configurations, such as the totem pole network of Figure 2-13, the parasitic diodes

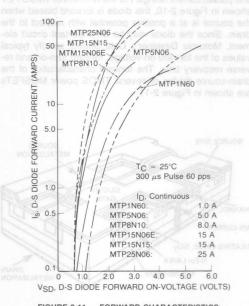


FIGURE 2-11 — FORWARD CHARACTERISTICS OF POWER MOSFETs D-S DIODES

play an important and useful role. Each transistor is protected from excessive flyback voltages, not by its own drain-source diode, but by the diode of the opposite transistor. As an illustration, assume that Q2 of Figure 2-13 is turned on, Q1 is off and current is flowing up from ground, through the load and into Q2. When Q2 turns off, current is diverted into the drain-source diode of Q1 which clamps the load's inductive kick to V+. By similar reasoning, one can see that D2 protects Q1 during its turnoff.

As a note of caution, it should be realized that diode recovery problems may arise when using MOSFETs in multiple transistor configurations. A treatment of the subject in Chapter 5 gives greater details.

TMOS power MOSFET intrinsic diodes also have forward recovery times, meaning that they do not insfantaneously conduct when they are forward biased. However, since those times are so brief, typically less than 10 ns, their effect on circuit operation can almost always be ignored. Package, lead and wiring inductance are often at least as great a factor in limiting current rise time.

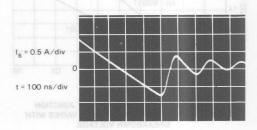


FIGURE 2-12 — REVERSE RECOVERY CHARACTERISTICS OF MTP15N15 DRAIN-SOURCE DIODE

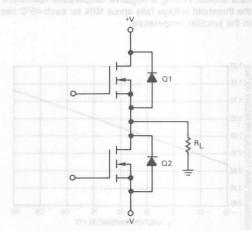


FIGURE 2-13 — TMOS TOTEM POLE NETWORK
WITH INTEGRAL DRAIN-SOURCE DIODES

Chapter 3: Using the TMOS Power MOSFET Designer's to receip and timed Data Sheets

Motorola Designer's Data Sheets are user oriented guides that provide information concerning all the basic TMOS parameters and characteristics needed for successful circuit design. An example of the MTM4N45 data

sheet is shown on the following pages. Helpful comments and explanations have been added to clarify some of the parameter definitions and device characteristics.

Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), SOA and VGS(th) Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

- · Represent the extreme capabilities of the de-
- Not to be used as design condition

- VGS

 Most Motorola TMOS power MOSFETs feature a rated VGS(max) of ±20 V. Logic level devices are the exception.
- · Exceeding Vqs(max) may result in permanent device degradation.
- Limit gate voltage spikes with a small 20 V zener diode if required. (10 V for L² devices)

ID - MAXIMUM CONTINUOUS DRAIN CURRENT IDM - MAXIMUM PULSED DRAIN CURRENT MAY BE LIMITED BY

- · PD
- rDS(on)
- Wire size and metallization
- · Combination of the above

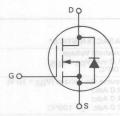
PD - MAXIMUM POWER AT A CASE TEMPERATURE OF 25°C

. Limit PD and TC so that TC + PD. ROUC < T_{J(max)}

T_{J(max)} — MAXIMUM JUNCTION TEMPERATURE

- · Reflects a minimum acceptable device service lifetime.
- Presently specified at 150°C for all Motorola power MOSFETs.
- · Operating at conditions that guarantee a junction temperature less than T_{J(max)} may enhance long term operating life





MAXIMUM RATINGS

Rating	Symbol	MTM4N45 MTP4N45	MTM4N50 MTP4N50	Unit
Drain-Source Voltage	VDSS	450	500	Vdc
Drain-Gate Voltage (RGS = 1.0 MΩ)	VDGR	450	500	Vdc
Gate-Source Voltage	VGS	±	20	Vdc
Drain Current Continuous Pulsed	I _D		.0	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		.6	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 t	o 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	R_{θ} JC	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

TMOS and Designer's are trademarks of Motorola Inc.

Designer's Data Sheets 120M reword 20MT ent prist 12 reigen0

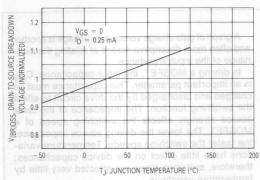
Motorola TMOS Power FETs are characterized on "Designer's Data Sheets." These data sheets permit the design of most circuits entirely with the information provided. Key parameters are specified at elevated temperature to provide practical circuit designs.

These data sheets permit the design of most circuits entirely with the information provided. Key parameters are specified at elevated temperature to provide practical circuit designs.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

2000	Characteristic				Symbol	Min	Max	Unit
OFF C	CHARACTERI	STICS						
	-Source Break		age		V(BR)DSS			Vdc
	$S = 0$, $I_D = 5.0$		MTM4	N45/MTP4N45 N50/MTP4N50	MO-M	450 500	_	
Zoro C				A STATUTE DELIVER	Ipss			mAdc
	Zero Gate Voltage Drain Current (VDS = 0.85 Rated VDSS, VGS = 0) -TC = 100°C					_	0.25	
						_	2.5	
Gate-				rs, converters, so		_	500	nAdc
(V _G	S = 20 Vdc, VD	(S = 0)	and antidepart	sort on sont or	1112 4			
		1	and Burning	D*001 is beilio	808			
16 b	S(th) Specifie	9V bris i	 No "negative res characteristic 	ning voltage sistance" region in the I	I-V			
		belimi		ture coefficient, as sho	wn in Figure 3-1			
ads	h Inductive Lo	Use Will	Characterized for	DSS • Speci	fied at 25°C and 100°C must be terminated to			
	9	0		TOWNS ASSESSMENT		ab add to se	IGSS • Specified	at max. rated V _G
ON	HARACTERIS	STICE*					d es dosign conditi	esu ed bi jol4 e
	Threshold Volt	Section 1			VCC/45		I	Vdc
(ID	= 1.0 mA, Vns				VGS(th)	2.0	4.5	Vuc
TJ	= 100°C	33		B 28 10 5		1.5	4.0	e Most Motordia
Drain	-Source On-Vo	oltage (VG	S = 10 V)	MT-7 (3) (3) 7	V _{DS(on)}	Logic level	V 05 = 10 (psm 2E	Vdc
	= 2.0 Adc)						3.0	devices are th
(I _D = 4.0 Adc)					Description of	7.5	A Providence of the	
		100°C)				-binded by	6.0	Exceeding, Vig nent device de
(ID	= 2.0 Adc, T _J =		tance		[DS(on)	V_DS name	6.0	
(I _D		On-Resist		RATINGS	rDS(on)	V_BS Hamel V_BS Hamel S devices		nènt daylos de
(I _D Static	= 2.0 Adc, T _J = Drain-Source	On-Resist			RUMIXAM -	V_DS items	6.0	nènt daylos de
Static (VG Forwa	= 2.0 Adc, T _J = Drain-Source S = 10 Vdc, I _D	On-Resist = 2.0 Add uctance				V_0s illami (2-devices)	6.0	Ohms
Static (VG Forwa	= 2.0 Adc, T _J = Drain-Source SS = 10 Vdc, I _D ard Transcondu SS = 15 V, I _D =	On-Resist = 2.0 Add uctance 2.0 A)			RUMIXAM -	V_0s illami (2-devices)	6.0	Ohms
Static (VG Forwa	= 2.0 Adc, T _J = c Drain-Source c _S = 10 Vdc, I _D ard Transcondu c _S = 15 V, I _D = 2	On-Resist = 2.0 Add uctance 2.0 A)	VGS(th)	RATINGS autog vonage	9FS	1.5	6.0 1.5 	Ohms mhos
Static (VG Forwa	= 2.0 Adc, T _J = Drain-Source SS = 10 Vdc, I _D ard Transcondu SS = 15 V, I _D =	On-Resist = 2.0 Add uctance 2.0 A)	VGS(th) • The gate voltage	je that must be applied	9FS to initiate con-	1.5	6.0 1.5	Ohms mhos
Static (VG Forwa	= 2.0 Adc, T _J = Drain-Source SS = 10 Vdc, I _D and Transcondu SS = 15 V, I _D = 3	On-Resist = 2.0 Add uctance 2.0 A)	VGS(th) The gate voltag duction (Figure	ge that must be applied 3-3).	9FS	1.5	6.0 1.5 	Ohms mhos
Static (VG Forwa	= 2.0 Adc, T _J = c Drain-Source c _S = 10 Vdc, I _D ard Transcondu c _S = 15 V, I _D = 2	On-Resist = 2.0 Add uctance 2.0 A)	VGS(th) • The gate voltag duction (Figure • Specified at 25°	je that must be applied 3-3). °C and 100°C	9FS to initiate con-	1.5	6.0 LL B	Ohms mhos
(ID Static (VG Forwa (VD	= 2.0 Adc, T _J = Drain-Source SS = 10 Vdc, I _D and Transcondu SS = 15 V, I _D = 3	On-Resist = 2.0 Add uctance 2.0 A)	VGS(th) • The gate voltag duction (Figure • Specified at 25°	ge that must be applied 3-3).	9FS to initiate con-	1.5	6.0 LL B	Ohms mhos
(ID Static (VG Forwa (VD	= 2.0 Adc, T _J = C Drain-Source SS = 10 Vdc, I _D SS = 15 Vdc, I _D = 003	On-Resist = 2.0 Add uctance 2.0 A)	VGS(th) The gate voltag duction (Figure Specified at 25° Negative tempe	je that must be applied 3-3). °C and 100°C	9FS to initiate con-	1.5	6.0 LL B	Ohms mhos
(ID Static (VG Forwa (VD	= 2.0 Adc, T _J = c Drain-Source s _S = 10 Vdc, I _D ard Transcondu s _S = 15 V, I _D = 1	On-Resist = 2.0 Add uctance 2.0 A)	VGS(th) The gate voltag duction (Figure Specified at 25° Negative tempe	e that must be applied 3-3). C and 100°C crature coefficient of ab	gFS to initiate con-	1.5	6.0 cc get a construction of the construction	Ohms mhos
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(ID Static (VG Forwa (VD	= 2.0 Adc, T _J =	On-Resist = 2.0 Add uctance 2.0 A)	VGS(th) • The gate voltag duction (Figure • Specified at 25' • Negative tempe °C (Figure 3-4).	ge that must be applied 3-3). "C and 100°C reature coefficient of ab	9FS to initiate con- out -6.7 mV/	V_2S perment (technolos) 1.5	6.0 cs general form of the following state of	Ohms mhos mhos MINAM — MGI MANAM — MGI
Static (VG Forwa (VD	= 2.0 Adc, T _J = C Drain-Source (SS = 10 Vdc, I _D (SS = 15 Vdc, I _D = 15 Vd,	On-Resist = 2.0 Add uctance 2.0 A)	VGS(th) • The gate voltag duction (Figure • Specified at 25' • Negative tempe °C (Figure 3-4).	je that must be applied 3-3). C and 100°C reature coefficient of ab VDS(on). * 'DS(on). Analogi	9FS to initiate con- out - 6.7 mV/	1.5	6.0 cos general de la companya de la	Ohms mhos mhos MINAM — MGI MANAM — MGI
(ID Static (VG Forwa (VD	= 2.0 Adc, T _J =	On-Resist = 2.0 Adc uctance 2.0 A)	VGS(th) • The gate voltag duction (Figure • Specified at 25' • Negative tempe °C (Figure 3-4).	pe that must be applied 3-3). C and 100°C prature coefficient of ab VDS(on). * rDS(on) Analog: Specific TMOS	gFS to initiate con- out -6.7 mV/ TDS(on) = VDS(on) D ous to the VCE(sat) of ed with a maximum V _(c) power MOSFETs.	1.5 1.5 f a bipolar device GS of 10 V for Mo	6.0 cos general de la companya de la	Ohms mhos mhos MAAA A A A A A A A A A A A A A A A A A
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(Ip Static (VG Forwa (VD	= 2.0 Adc, T _J =	On-Resist = 2.0 Ado uctance 2.0 A)	VGS(th) The gate voltag duction (Figure Specified at 25° Negative tempe °C (Figure 3-4).	je that must be applied 3-3). C and 100°C erature coefficient of ab VDS(on) • rDS(on) • Analog • Specifie TMOS • Specifie • Positive	gFS to initiate con- out - 6.7 mV/ TDS(on) VDS(on) In In UDS(on) Out to the VCE(sat) o' ad with a maximum V power MOSFETS. ad at 25°C and 100°C	1.5 f a bipolar device GS of 10 V for Moent promotes curre	6.0 general file of the file o	Ohms mhos mhos mhos manual man
Static (VG) Forwar (VD) MA	= 2.0 Adc, T _J =	On-Resist = 2.0 Ado uctance 2.0 A)	VGS(th) • The gate voltag duction (Figure Specified at 25° • Negative tempe °C (Figure 3-4).	ye that must be applied 3-3). C and 100°C erature coefficient of ab VDS(on). rDS(on). Analog. Specific TMOS Specific Positive sharing	out -6.7 mV/ TDS(on) TDS(on	1.5 f a bipolar device GS of 10 V for Moent promotes curre	6.0 general file of the file o	Ohms THE STATE OF
(Ip Static (VG Forwa (VD	= 2.0 Adc, T _J = C Drain-Source S _S = 10 Vdc, I _D and Transcondu S = 15 V, I _D = :	On-Resist = 2.0 Ado uctance 2.0 A)	VGS(th) • The gate voltag duction (Figure Specified at 25' • Negative tempe °C (Figure 3-4).	ye that must be applied 3-3). C and 100°C erature coefficient of ab VDS(on). rDS(on). Analog. Specific TMOS Specific Positive sharing	out -6.7 mV/ TDS(on) VDS(on) ID Sous to the VCE(sat) of odd with a maximum V(power MOSFETs. at at 25°C and 100°C at temperature coefficie when devices are pa	f a bipolar device GS of 10 V for Mo ent promotes curre ralleled.	6.0 SECOND SECON	Chms Chms Mhos Mhos MixAM — Mid Chms MixAM — Mid Chms MixAM — Mid Chms MixAM — Mid Chms Ch
(Ip Static (VG Forwa (VD	= 2.0 Adc, T _J =	On-Resist = 2.0 Ado uctance 2.0 A)	VGS(th) The gate voltag duction (Figure Specified at 25° Negative tempe °C (Figure 3-4).	ye that must be applied 3-3). C and 100°C erature coefficient of ab VDS(on). • rDS(on • Analog • Specific • Positive sharing	gFS to initiate con- out -6.7 mV/ "DS(on) "DS(on) "DS(on) "Do ous to the VCE(sat) o' dwith a maximum V, opwer MOSFETs. ed at 25°C and 100°C temperature coefficie when devices are pa	f a bipolar device GS of 10 V for Mo ent promotes curre ralleled.	6.0 general file of the file o	Ohms mhos mhos analogous to hearacteristic
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(Ip Static (VG Forwa (VD	= 2.0 Adc, T _J = C Prain-Source (Se = 10 Vdc, I _D) and Transcond (Se = 15 V, I _D = 10 Vdc, I _D) and Transcond (Se = 15 V, I _D = 10 Vdc, I _D) and I _D = 10 Vdc, I _D	On-Resist = 2.0 Ado uctance 2.0 A)	VGS(th) • The gate voltag duction (Figure Specified at 25' • Negative tempe °C (Figure 3-4).	vDS(on) VDS(on) VDS(on) VDS(on) VDS(on) PS(on) PS(on) Analoge Specific Positive sharing	gFS to initiate con- out - 6.7 mV/ "DS(on) "	f a bipolar device GS of 10 V for Moent promotes curreralleled. FS The MOSFET "g Equal to the slop (Figure 2-7). FS = $\frac{\Delta ID}{\Delta VGS}$	6.0 1.5 — and osamus so torola sin" parameter — e of the transfer ch	Ohms mhos mhos
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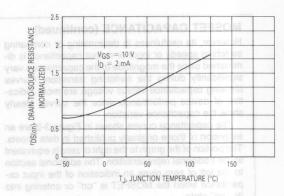


FIGURE 3-2 — NORMALIZED ON-RESISTANCE versus TEMPERATURE

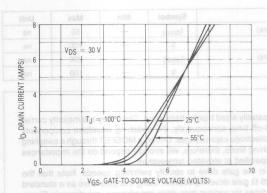


FIGURE 3-3 — TRANSFER CHARACTERISTICS

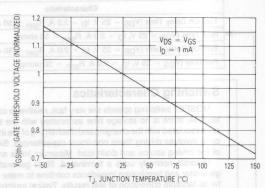


FIGURE 3-4 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

to a DYNAMIC CHARACTERISTICS a agV aA imminism at philosoticgs item most season of

Vito earl efficiently as O to be Characteristic	Symbol	Min	Max	Unit
Input Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz)	Ciss	— Cies be	1200	□ ⊕ pF
Output Capacitance (VDS = 25 V, VGS = 0, f = 1 MHz)	Coss	supply o	300	pF
Reverse Transfer Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz)	C _{rss}	ISTO WOL	80	pF

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (Cqd), and gate-to-source (Cqs). The PN junction formed during the fabrication of the TMOS FET results in a junction capacitance from drain-to-source (Cds). These capacitances are characterized as input (Ciss), output (Coss) and reverse transfer (Crss) capacitances on data sheets.

Specification of MOSFET capacitance at a VDS of 25 V has become somewhat of a standard, so that information is provided in all TMOS data sheets.

2500 $T_J = 25^{\circ}C$ $V_{GS} = 0$ 1500 500 OSS 25 VGS ◄ - VDS GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

FIGURE 3-5

(continued)

MOSFET CAPACITANCE (continued)

However, its usefulness in determining or comparing switching speeds or input or output capacitance is diminished since the magnitude of the capacitances vary significantly during the switching transition. Curves showing capacitance versus voltage are more indicative of device performance since the curves clearly show the capacitance variation.

The capacitance curves shown in Figure 3-5 are an extension of those originally published in data sheets. The portion of the graph to the right of zero is equivalent to the traditional representation. The additional section to the left of zero gives an indication of the input capacitance when the MOSFET is "on" or entering into its "on" state.

A graph of gate charge versus gate voltage is another and often more descriptive means of relating the magnitude of the input impedance.

In driving a MOSFET, the input capacitance, C_{iSS} is an important parameter. This capacitance must be charged and discharged by the drive circuit to effect the switching function. The impedance of the drive source strongly affects the switching speed of a MOSFET. The lower the driving source impedance, the faster the switching speeds. Temperature variations have little effect on the device capacitances; therefore, switching times are affected very little by temperature variations.

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Characteristic	Symbol	Min	Max	Unit
Turn-On Delay Time (V _{DS} = 25 V, I _D = 2.0 A, R _{gen} = 50 ohms)	td(on)	+	50	ns
Rise Time (V _{DS} = 25 V, I _D = 2.0 A, R _{gen} = 50 ohms)	t _r	-	100	ns
Turn-Off Delay Time (V _{DS} = 25 V, I _D = 2.0 A, R _{gen} = 50 ohms)	td(off)	-	200	ns
Fall Time (V _{DS} = 25 V, I _D = 2.0 A, R _{qen} = 50 ohms)	tf	-	100	ns

Switching Characteristics

MOSFET switching speeds are very fast, relative to comparably sized bipolar transistors. Since they are majority carrier devices, there is no storage time associated with the turn-off time; consequently, the switching waveform components are associated with the charging and discharging of the interelectrode capacitances. Driving a MOSFET through a switching cycle involves driving these non-linear capacitances. Switching times, therefore, will strongly depend on the impedances of the driving source and drain load. Maximum limits are specified at elevated temperature.

Motorola normally uses a terminated, 50 Ω generator in the gate drive to specify switching speeds. Note that the generator and termination impedance combine to make a 25 Ω gate drive impedance. Using this gate drive as a standard helps facilitate correlation of test results. Typical switching times for various gate drive impedances, are shown in Figure 3-8.

For Resistive Switching:

- $\bullet \ \, \text{During} \ t_{d(on)} \text{The drive circuit charges C_{iss} to $V_{GS(th)}$. No drain current flows; V_{DS} remains essentially at V_{DD}. }$
- During tr
 Ciss is charged by the drive circuit to VGS(on). Coss discharges from VDD to approach VDS(on) and ID increases from zero, approaching its maximum. As VDS approaches VDS(on), the rapid rise of Coss at low drain voltages delays the rise of ID, likewise the increase of Ciss inhibits the rise of VGS through the drive impedance.
- During t_{d(off)}
 Ciss begins to discharge through the gate circuit impedance. The transistor turns off and the drain supply charges Coss through the load. The initial rise of V_{DS} is slowed by the high value of C_{OSS} at low drain voltages.
- During tf
 Coss diminishes rapidly as the drain voltage rises. Virtually no additional charge is required to be sourced by the drain supply; VDS rises rapidly to VDD (and beyond if inductance is present in the load).

Resistive Switching

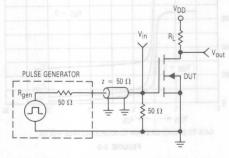


FIGURE 3-6 — SWITCHING TEST CIRCUIT

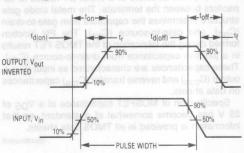


FIGURE 3-7 — SWITCHING WAVEFORMS

MOTOROLA TMOS POWER MOSFET DATA



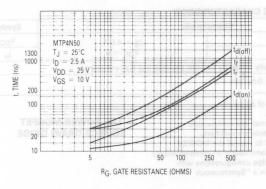


FIGURE 3-8

GATE CHARGE CHARACTERISTICS

Characteristic		Symbol	Min	Max	Unit
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = 4 Amps, V _{GS} = 10 V)	Qg	27 (typ)	32	nC
Gate-Source Charge		Qgs	17 (typ)	_	
Gate-Drain Charge		Q _{qd}	10 (typ)	12D	

Gate Charge Characteristics

Fundamentally, the gate charge versus gate-to-source voltage curves are used to determine the amount of charge, defined as Q_{Q} , required to bring C_{ISS} from zero volts to 10 V. Typically, the maximum rating is specified at an I_{Q} equal to the device's continuous rating at 25°C and at a supply voltage of 80% of maximum rated V_{DS}. Gate charge is essentially

In addition to typical and maximum values of Q_g , the data sheets also specify typical values of Q_{gd} and Q_{gs} . Q_{gd} is the charge required by C_{rss} (C_{gd}) during the fall of V_{DS} . This occurs during the plateau region of Figure 3-9. Q_{gs} refers to the total charge required by C_{rss} during the two intervals characterized by ramping up of V_{GS} before and after the plateau. During the first interval most of this charge flows into C_{gs} but during the second interval C_{rss} takes on the majority of the charge. Hence, the term " Q_{gs} " is somewhat of a misnomer.

A substantial amount of other data may be extracted from the curve. Estimation of the required average gate current for a diven switching according to the carter and marginity of the input approximation are second interval.

for a given switching speed, energy transferred to the gate, and magnitude of the input capacitance are some of its other

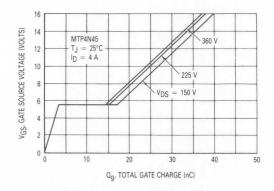


FIGURE 3-9 — Q_g TOTAL GATE CHARGE (nC)

SOURCE-DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Тур	Unit
Forward On-Voltage	Is = 4.0 A	V _{SD}	1.1	Vdc
Reverse Recovery Time	$v_{GS} = 0$	t _{rr}	420	ns

*Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

Rectifier" mode.

- An integral feature of all power MOSFET structures.
- Reverse recovery times are comparable with those of fast recovery rectifiers.
- Rated current equal to that of the MOSFET
 May be used as a commutator in complementary totem-pole or H-bridge configurations with inductive loads, or in a "Synchronous

THE POWER MOSFET SOURCE-DRAIN DIODE



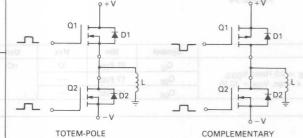
DUT WAVEFORM

90%

10%

+ V_{DD}

dl_D/dt



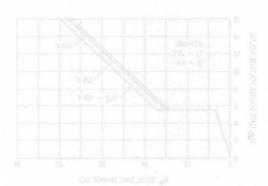
N-CHANNEL

P-CHANNEL/N-CHANNEL 2 PROTECTS

DURING TURN-OFF OF Q1, D2 PROTECTS Q1; LIKEWISE DURING TURN-OFF OF Q2, D1 PROTECTS Q2

TMOS power MOSFET intrinsic diodes also have forward recovery times, meaning that they do not instantaneously conduct when they are forward biased. However, since those times are so brief, typically less than 10 ns, their effect on circuit operation can almost always be ignored. Package, lead and wiring inductance are often at least as great a factor in limiting current rise time.

FIGURE 3-10 — SOURCE-TO-DRAIN DIODE TEST CIRCUIT AND WAVEFORM





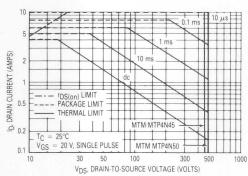


FIGURE 3-11 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

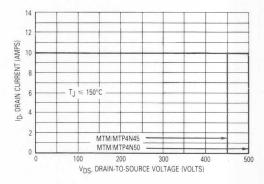


FIGURE 3-12 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

THERMAL RESPONSE

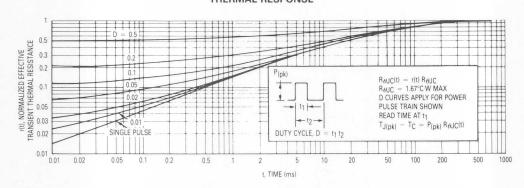


FIGURE 3-13 — MTM4N45/MTM4N50

Guaranteed Safe Operating Area

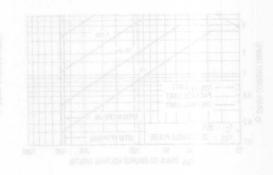
FBSOA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569. "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

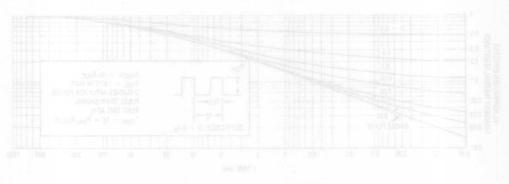
SSOA

The switching safe operating area in Figure 3-12 is the boundary that the load line may traverse without incurring damage to the device. The fundamental limits are the maximum rated peak drain current IDM, the minimum drain to source breakdown voltage V(BR)DSS and the maximum rated junction temperature. The boundaries are applicable for both turn-on and turn-off of the devices for rise and fall times of less than one microsecond.









Chapter 4: Design Considerations in Using Power MOSFETs

Protecting the Power MOSFET

Safe Operating Areas

To provide the designer with Safe Operating Area information for the various modes of operation the TMOS transistor may encounter, two different Safe Operating Areas are defined on the TMOS data sheets: the Forward Biased Safe Operating Area, or FBSOA (often referred to as simply SOA), and the Switching SOA or SSOA. The SSOA curves of MOSFETs describe the voltage and current limitations during turn-on and turn-off and are normally used in the same manner as the RBSOA curves of bipolar transistors.

FBSOA:

An FBSOA curve defines the maximum drain voltage and currents that a device can safely handle when forward biased, or while it is on or being turned on. Of the four limits dictated by the boundaries o, the FBSOA curve, the most unforgiving is the maximum drain-source voltage rating which is indicated by boundary A in Figure 4-1. If this rating is exceeded, even momentarily, the device can be damaged permanently. Thus, precautions should be taken if there may be transients in the drain supply voltage.

Maximum allowable drain current is time or pulse-width dependent and defines the second boundary of the FBSOA curve, represented by Line D. The limit is determined by the bonding wire diameter, the size of the source bonding pad, device characteristics and thermal resistance. Even though MOSFETs show rugged overcurrent capabilities, devices should not conduct more than their rated drain current for a given pulse duration. This includes transient currents such as the high in-rush current drawn by a cold incandescent lamp or the reverse recovery current required by a diode.

The third boundary, Line B is fixed by the drain-to-source on-resistance and limits the current at low drain-source voltages. Simply a manifestation of Ohm's Law, the limitation states that with a given on-resistance, current is limited by the applied voltage. The boundary does not describe a linear relationship, however, because the on-resistance increases gradually with increasing current.

The fourth limit, shown as Line C in Figure 4-1, is set by the package thermal limit. This power limited portion of the FBSOA curve is generated from the device thermal response curve, maximum allowable junction temperature and maximum $\rm R_{\theta JC}$ rating. Operation inside this curve insures that the maximum junction temperature does not exceed the 150°C maximum rating.

Since the transient thermal resistance decreases dramatically for shorter pulse durations, the peak power handling capability increases accordingly. For example, Figure 4-2 shows that at 100 μs the normalized single pulse transient resistance of the MTM8N40 is 0.033. Multiplication by R $_{\theta JC}$ (0.033 x 0.83°C/W) results in the effective thermal impedance for a single 100 μs pulse. From the definition of thermal resistance $\left(R_{\theta JC} = \frac{T_J - T_C}{T_J}\right)$

the magnitude of the power pulse that coincides with a

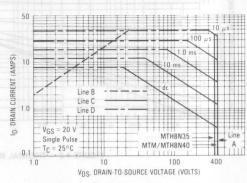


FIGURE 4-1 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA OF THE MTM8N40

T_J of 150°C and a T_C of 25°C is easily determined. In this case, (0.033 x 0.83°C/W = $\frac{150 - 25^{\circ}C}{P_D}$), P_D is 4564 W.

Therefore, at a V_{DS} of 200 V, the MTM8N40 can conduct about 23 A during a 100 μ s pulse without exceeding the T_J(max) rating of 150°C.

Normally the portion of the FBSOA curves that is determined by the package thermal limit is only of interest to designers who foresee a condition of simultaneous high voltage and high current for periods greater than 10 μ s. This situation can occur in linear applications or in switching applications that experience a fault condition such as a shorted load. For those applications the information contained in Figure 4-1 is incomplete since the data is based on single pulse testing at a case temperature of 25°C. For multiple pulses and case temperatures other than 25°C, the maximum allowable power dissipation can be computed as shown in AN569, "Transient Thermal Resistance General Data And Its Use."

To a large extent, thermal limitations determine the SOA boundaries for MOSFETs used in linear applications. The maximum allowable junction temperature $T_{J(max)}$ also affects the pulsed current ratings applicable when the MOSFET is used as a switch. With respect to current ratings, MOSFETs are more like rectifiers than bipolar transistors in that their peak current ratings are not gain limited, but thermally limited. Since $r_{DS(on)}$, on-state power dissipation, switching losses, pulse width, duty cycle and junction to ambient thermal impedance all influence $T_{\rm J}$, they also affect the maximum allowable pulsed drain current.

In switching applications the total power dissipation is comprised of switching losses and on-state losses. At low frequencies, the MOSFETs switching losses are small enough to ignore. However, as frequency increases the losses eventually become significant and force an increase in TJ. The break point between what is considered low and high frequencies depends on the gate drive impedance. With a low impedance gate-drive, switching losses are small below 40 to 50 kHz.

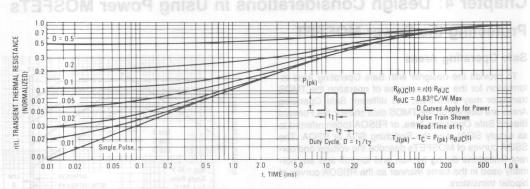


FIGURE 4-2 — THERMAL RESPONSE CURVE OF THE MTM8N40

Since the magnitude of the MOSFET capacitances and, therefore, switching speeds are nearly constant as T_J varies, power MOSFET switching losses are nearly temperature invarient. Without the additional complexity of temperature dependence, losses during the relatively high dissipation turn-on and turn-off intervals are easily modeled and estimated. These techniques are also shown in Motorola Application Note AN569.

Because on-state losses are often the bulk of the total power dissipation, they greatly affect the MOSFET's maximum allowable pulsed current capability. The computation of these losses is somewhat involved due to the variation of rps(on) with temperature and drain current. After computing the heating component of the drain current (RMS value), an iterative technique is used to determine the on-state power dissipation. The following example illustrates how on-state losses and junction temperature can be determined.

Assume the drain current waveform of an MTM8N40 is trapezoidal with the current rising from 8.0 A to 16 A in 25 μ s. The duty cycle is 50% and the frequency is 20 kHz. Heat sinking will be provided to keep the case temperature at 80°C. From Figure 4-2, the normalized transient thermal impedance for a 25 μ s pulse and 50% duty cycle is 0.5, yielding an effective thermal impedance of 0.415°C/W. [r(t) x R $_{\theta JC} = 0.5$ x 0.83°C/W].

Before proceeding, the on-resistance and the RMS value of the ID waveform must be determined. Since $^{\rm rDS(on)}$ is temperature dependent, the junction temperature must be roughly estimated. A TJ of 110°C seems appropriate in this case. From Figure 4-3, $^{\rm rDS(on)}$ at 110°C is 1.02 Ω .

This value of $r_{DS(on)}$ is derived from a typical curve and does not represent a worst case value. To obtain a worst case estimate, the ratio between the maximum rated $r_{DS(on)}$ and the typical $r_{DS(on)}$ under the same operating conditions can be used as a multiplier. In this situation, an $r_{DS(on)}$ maximum of 0.55 ohms is specified at an $r_{DS(on)}$ maximum of 0.55 ohms is specified at an $r_{DS(on)}$ for an analysis of 4.0 Å and a $r_{DS(on)}$ for these same conditions, $r_{DS(on)}$ is typically at 0.45 ohms (Figure 4-3). Assuming the ratio between typical and worst case values remains

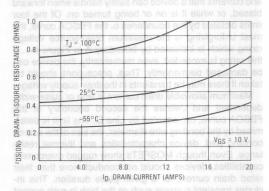


FIGURE 4-3 — ON-RESISTANCE versus DRAIN CURRENT FOR THE MTM8N40

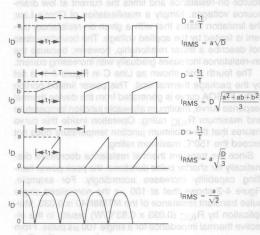


FIGURE 4-4 — RMS VALUES OF SOME COMMON SIDE BOTH CURRENT WAFEFORMS

fairly constant, the multiplier is 1.22, $\frac{rDS(on) MAX}{rDS(on) TYP} = \frac{0.55}{0.45}$. Therefore, the worst case rDS(on) at 12 A, 110°C is approximately 1.22 x 1.02 ohms, or 1.24 ohms. From the trapezoid waveform in Figure 4-4:

IRMS = D
$$\sqrt{\frac{a^2 + ab + b^2}{3}}$$
 = = 0.5 $\sqrt{\frac{8^2 + 8 \cdot 16 + 16^2}{3}}$ = 0.5 $\sqrt{\frac{8^2 + 8 \cdot 16 + 16^2}{3}}$ = 0.7 and PD = 1^2 RMS rDS(on) = (6.11)² 1.24 = 46.3 W

If switching losses are significant, they should be included at this step. Proceeding with the computation of T,I,

$$\Delta T_{JC} = P_D R_{\theta JC}$$

However, $A_{JC} = P_D R_{\theta JC}$
 $A_{JC} =$

then the calculated T_J of 99.2°C replaces the original 110°C estimate and $r_{DS(on)}$, P_D and T_J are recomputed. The initial guess was close, and 97.3°C is the final solution. Therefore the transistor is operating within its thermal limitations and its current handling capabilities.

SSOA

Switching Safe Operating Area defines the MOSFETs voltage and current limitations during switching transitions. Although an SSOA curve also outlines turn-on boundaries, it is normally used as a turn-off SOA. As such, it is the MOSFET equivalent of the Reverse Biased SOA (RBSOA) of bipolars.

Like RBSOA ratings, turn-off SOA curves are generated by observing device performance as it switches a clamped inductive load. An inductive load is used because it causes the greatest turn-off stress, but it must be clamped so as not to avalanche the transistor with an uncontrolled drain-source "flyback voltage." Switching speeds, which directly determine crossover times and switching losses, also influence the turn-off SOA.

As shown in Figure 4-5, the SSOA curve of the MOSFET is bounded by its maximum pulsed drain current, I_{DM} , and the maximum drain-source voltage, V_{DSS} , as long as switching times are less than 1.0 μ s. If MOSFETs are operated within their I_{DM} , V_{DSS} and $T_{J(max)}$ ratings, their SSOA curves guarantee that a secondary breakdown derating is unnecessary.

Drain-Source Overvoltage Protection

The most common cause of failure in a power MOSFET is due to an excursion across an SOA boundary. A good portion of these failures are a result of exceeding the maximum rated drain-source voltage, V(BR)DSS. Drain voltage transients caused by switching high currents through load or stray inductances can force VDS to exceed V(BR)DSS and may contain enough energy to de-

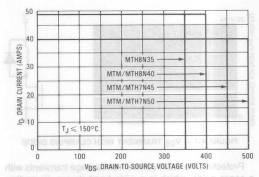


FIGURE 4-5 — MAXIMUM RATED SWITCHING SAFE OPERATING ARE OF THE MTM8N40

stroy the device if it begins to avalanche. Transients on the drain supply voltage can also destroy the power MOSFET.

Fortunately, if there is any danger of these destructive transients, the solutions to the problems are fairly simple. Figure 4-6 illustrates a FET switching an inductive load in a circuit which provides no protection from excessive flyback voltages. The accompanying waveform depicts the turn-off voltage transient due to the load and the parasitic lead and wiring inductance. The MTM20N10 experiences the unrecommended avalance condition for about 300 ns at its breakdown voltage of 122 volts.

One of the simplest methods of protecting devices from flyback voltages is to place a clamping diode across the inductive load. Using this method, the diode will clamp most, but not all, of the voltage transient. V_{DS} will still overshoot V_{DD} by the sum of the effects of the forward recovery characteristic of the diode, the diode lead inductance and the parasitic series inductances as shown in Figure 4-7.

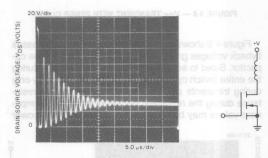


FIGURE 4-6 — V_{DS} TRANSIENT DUE TO UNCLAMPED INDUCTIVE LOAD

If the series resistance of the load is small compared to its inductance, a simple diode clamp may allow current to circulate through the load-diode loop for a significant amount of time after the MOSFET is turned off. When this lingering current is unacceptable, a resistor can be inserted in series with the diode at the expense of increasing the peak flyback voltage seen at the drain.

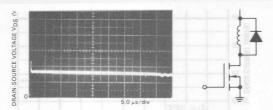


FIGURE 4-7 - VDS TRANSIENT WITH CLAMPING DIODE

Protecting the drain-source from voltage transients with a zener diode, which is a wide band device, is another simple and effective solution. Except for the effects of the lead and wiring inductances and the virtually negligible time required to avalanche, the zener will clip the voltage transient at its breakdown voltage. A transient with a slow dvDS/dt will be clipped completely while a transient with a rapid dv/dt might momentarily exceed the zener breakdown voltage. These effects are shown in Figure 4-8. Even though it is a very simple remedy, the zener diode is one of the most effective means of transient suppression. Obviously, the power rating of the zener should be scaled so that the clipped energy is safely dissipated.

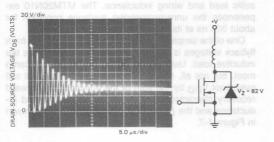


FIGURE 4-8 - VDS TRANSIENT WITH ZENER CLAMP

Figure 4-9 shows an RC clamp network that suppresses flyback voltages greater than the potential across the capacitor. Sized to sustain a nearly constant voltage during the entire switch cycle, the capacitor absorbs energy only during transients and dumps that energy into the resistance during the remaining portion of the cycle. Component values may be computed by considering the power

sized. Finally, the magnitude of the capacitance may be determined by relating the RC time constant to the period of the waveform.

As an example, a similar circuit has the following characteristics:

$$L = 10 \mu H^{Sd} + ds + Sg$$

= 3.0 A (load current just before turn-off

V_C = 60 V (desired clamp voltage)

The power to be absorbed by the clamp network is:

$$P = 1/2 \text{ Li}^2 \times f = 1.125 \text{ W} = 1.125 \text{ W}$$

The component values can be determined:

$$\frac{V_c^2}{P} = R = 3.2K \approx 3.3K$$

Let
$$\tau = RC = 5.0 \div f = 200 \ \mu s$$

 $C = 0.061 \ \mu F \approx 0.05 \ \mu F$

While this is a common and efficient cricuit, the switching speeds of MOSFETs may produce transients that are too rapid to be attentuated by this method. If the flyback voltage reaches its peak during the first 50 ns, the effectiveness of the circuit will be undermined due to the forward recovery characteristic of the clamp diode and any stray circuit inductance. It may be prudent in these cases to include a zener with a breakdown voltage slightly higher than the clamp voltage. When placed directly across the drain and source terminals, the lead lengths are short enough and the zener is fast enough to catch most transients. Since the zener's only purpose is to clip the initial flyback peak and not to absorb the entire energy stored in the inductor, the zener power rating can be smaller than that needed when one is used as the sole clamping element

A fourth way to protect power MOSFETs from large drain-source voltage transients is to use an RC snubber network like that of Figure 4-10. Although it effectively reduces the peak drain voltage, the snubber network is not as efficient as a true clamping scheme. Whereas a clamping network only dissipates energy during the transient, the RC snubber also absorbs energy during portions of the switching cycle that are not overstressing the transistor. This configuration also slows turn-on due to the additional drain-source capacitance that must be discharged.

Clamp Voltage, Vo

Vns out of

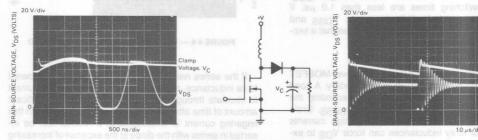


FIGURE 4-9 — VDS TRANSIENT AND RC CLAMP VOLTAGE WITH RC CLAMP NETWORK

No matter which scheme is used, very rapid inductive turn-off can cause transients during the first tens of nanoseconds that may be overlooked unless a wideband oscilloscope (B.W. ≥ 200 MHz) is used to observe the V_{DS} waveform.

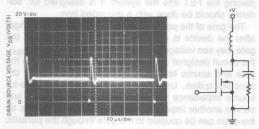


FIGURE 4-10 - VDS TRANSIENT WITH RC SNUBBER

Package and Lead Inductance Considerations

The drain and source parasitic package inductance can influence the magnitude of V_{DS} during rapid switching of very large currents. In Figure 4-11, the drain and source package inductance has been combined and placed in the source because that wirebond and lead length accounts for the bulk of the inductance. The magnitudes of L_S in the TO-204, (TO-3) and the TO-220 packages are around 12 and 8 nH, which are large enough to produce appreciable voltage during a very rapid rate of change in drain current. The polarity of the induced voltage is such that the drain-source voltage appearing at the chip is greater than that appearing at the device terminals.

As an example, assume that an MTP25N06 is turned off in 50 ns after conducting 50 A. A di/dt of this magnitude will produce about 8.0 volts across the parasitic package inductance (v = L di/dt = 8.0 nH 50 A/50 ns). If the drain-source voltage at the terminals is 50 V, then VDS at the die is 58 volts.

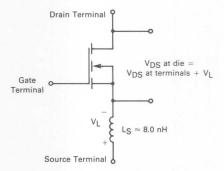


FIGURE 4-11 — VERY RAPID TURN-OFF INCREASES DRAIN-SOURCE VOLTAGE STRESS

Although all power MOSFETs experience some internally generated voltages during rapid switching, peak di/dt's are usually not extreme and the associated voltages are generally small. However, the current ratings of

power MOSFETs recently have increased rapidly and, consequently, their maximum di/dt capabilities have also risen. The MTM60N06, with its pulsed current rating of 300 A, falls into the category of such a device. The very large di/dt capabilities that accompany these current ratings can produce significant VDS stress in addition to that observed at the drain-source terminals.

To assure that the peak V_{DS} at the chip does not exceed the maximum V_{DSS} rating of the device, the following equation can be used:

 $V_{DS(max)} = V_{(BR)DSS} - L(di/dt)$

where $V_{DS(max)}$ is the maximum allowable voltage appearing across the drain-source terminals, $V_{(BR)DSS}$ is the maximum device rating, L is the parasitic source inductance and di/dt is the rate of change in I_D coincident with $V_{DS(max)}$.

Voltages appearing across the package source inductance also affect the magnitude of the gate-source voltage at the chip and are of such polarity that they slow both the turn-on and turn-off transitions. If large currents are being switched, the parasitic package inductance is large enough to be the factor that limits the MOSFET's switching speeds.

Except for circuits that produce very large di/dt's, the proceeding discussion of package inductance is of academic interest only. However, wiring inductance is often much larger than the package inductance and its effects are proportionately greater. Therefore, the above considerations may become very practical problems in applications in which the di/dt's are not extreme. The quality of the circuit layout dictates the degree of concern.

Avalanche and dv/dt Limitations of Power MOSFETs

Until recently a MOSFET's maximum drain-to-source voltage specification prohibited even instantaneous excursions beyond that voltage, since the first power MOSFETs were never intended to be operated in avalanche. As is still the case with most bipolar transistors, capability was simply not specified. Some devices happened to be quite rugged, while others were not. Now it is known that a power MOSFET can be constructed to sustain substantial currents in avalanche at elevated junction temperatures, so newly designed MOSFETs are replacing the original devices. "Ruggedized" is the term being used to refer to devices that carry some form of rating to define avalanche capability.

The MOSFET's ability to withstand rapid changes in drain-to-source voltage, especially during reverse recovery of the MOSFET's intrinsic diode, is another issue that has received much attention lately. In this case the first devices were very rugged except for the case of diode recovery. Again the latest devices show performance improvements and carry ratings to inform designers of their new strength.

Because of the interest in avalanche and dv/dt issues and their importance, a discussion of these topics is provided in Chapter 5, "Avalanche and dv/dt Limitations of the Power MOSFET."

Protecting the Gate a syst vineser sTansOM 19Woo

The gate of the MOSFET, which is electrically isolated from the rest of the die by a very thin layer of SiO2, may be damaged if the power MOSFET is handled or installed improperly. Exceeding the 20 V maximum gate-to-source voltage rating, VGS(max), can rupture the gate insulation and destroy the FET. TMOS FETs are not nearly as susceptible as CMOS devices to damage due to static discharge because the input capacitances of power MOSFETs are much larger and absorb more energy before being charged to the gate breakdown voltage. However, once breakdown begins, there is enough energy stored in the gate-source capacitance to ensure the complete perforation of the gate oxide. To avoid the possibility of device failure caused by static discharge, precautions similar to those taken with small-signal MOSFET and CMOS devices apply to power MOSFETs.

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging

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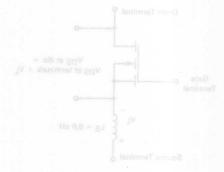
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should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

The gate of the power MOSFET could still be in danger after the device is placed in the intended circuit. If the gate may see voltage transients which exceed VGS(max), the circuit designer should place a 20 V zener across the gate and source terminals to clamp any potentially destructive spikes. Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device

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PIGURE 4-1 -- VERY RAPID TURN-OFF INCREASES

Although all power MOSFETs experience some internally generated voltages during rapid switching, peak divides are usually not extreme and the associated volt-

Chapter 5: Avalanche and dv/dt Limitations of the Power MOSFET

The power MOSFET's ability to withstand voltage and current transients inside and outside published safe operating areas is often of concern to design engineers. Since anticipating every possible fault condition that can occur in the field is very difficult, the use of a device that has some tolerance to transients is highly desirable.

By nature the power MOSFET is resistant to failure in certain modes. Its ability to withstand overcurrent stresses is a good example of one of its strengths. However, ruggedness in other modes is not a given, and device design and processing must target those types of failures if a MOSFET is to be robust in those modes, too.

Motorola's development of the E-FET, a "ruggedized" device sometimes referred to as TMOS IV, is a significant step toward extending the MOSFET's ruggedness to include several of the most common fault induced stresses. Designed-in ruggedness, combined with the MOSFET's ability to withstand forward bias stress, make the E-FET a very fault tolerant device in all major areas of concern, including what has been called the "commutating dv/dt" mode. The issues surrounding these significant modes of stress are discussed in detail below.

The Power MOSFET in Drain-to-Source Avalanche

The MOSFET's unique capability of high speed switching can lead to stresses that are not encountered with slower devices. Often gate drive circuits are designed for very fast switching speeds to lower switching times and increase circuit efficiency. These speeds may be so fast that the inductive kick occurring at turn off produces an extremely rapid rise in the drain-to-source voltage — perhaps so rapid that parasitic circuit elements and turn-on times undermine a protection clamp's ability to respond in time to protect the MOSFET. Such parasitics that diminish response times include the inductance in the wiring, leads, and packages. Forward recovery time of protection diodes may also delay response time.

Voltage transients of this type are usually brief, lasting only until the voltage clamp or snubber reacts. Nevertheless, for a short time the MOSFET is forced to conduct what may be a high avalanche current. Although the total energy that the device sees in breakdown is fairly small, failures may occur since ruggedness in avalanche is a strong function of the peak avalanche current. At high switching speeds such brief transients are a common source of overvoltage spikes.

Another cause of overvoltage transients is voltage spiking on the drain supply voltage. When this occurs, the peak magnitude of the associated avalanche current is difficult to predict since it depends on the nature of the transient. Pulse duration and energy may vary widely; consequently, the MOSFET's ability to survive high avalanche currents lasting for extended pulse widths is important.

The recent development of the E-FET has made available MOSFETs with the ability to survive both types of overvoltage transients. These new devices are sufficiently rugged to carry ratings that guarantee an avalanche current capability for the two types of overvoltage transients discussed above.

An energy rating alone is a poor indication of a device's ability to survive overvoltage transients. Manufacturers can easily fabricate high energy values by carefully choosing test conditions that allow dissipation of energy over a long pulse width. An extreme example is the 12 A, 60 V MTP3055E that can dissipate 75 joules if allowed to conduct 1 A in avalanche for 1 second. However, one of these devices is likely to fail with very little energy dissipation if it is forced to conduct more than 40 A in avalanche.

The bottom line is that the propensity for failure is almost exclusively a function of two parameters: peak current in avalanche and peak (not average) junction temperature. Except for raising the average junction temperature — thereby enhancing the chance of hotspot failure — the total energy dissipated has only secondary effects.

Avalanche Test Methods and Ratings

Understanding the causes of overvoltage transients and the conditions that determine the propensity for failure provide a foundation for defining the most appropriate avalanche test methods. There are two viable tests: each offers its own benefits. The most common test circuit and its associated current and voltage waveforms are shown in Figures 1 and 2. Testing in this circuit is appropriately referred to as Unclamped Inductive Switching, or UIS, as there is no diode clamp across the coil to limit the flyback voltage appearing at the drain.

Although there is controversy surrounding some of the test conditions (such as coil size, initial and final junction temperatures and peak current), circuit operation is very straightforward. The gate drive is turned on and current in the coil is allowed to ramp up to the desired test current, which is primarily set by the coil size, the supply voltage and the on time of the gate drive ($\Delta I = (V_{DD}/L)\Delta t$). When the load current reaches the desired value, the MOSFET is abruptly turned off. Since the load current cannot change instantaneously, the inductive energy drives the drain-to-source voltage to $V_{(BR)DSS}$; the MOSFET then dissipates the stored energy in avalanche.

In this circuit the total energy dissipated by the MOSFET may not be equal to that stored in the coil. During avalanche, additional energy is transferred from the V_{DD} supply to the MOSFET. For low test currents (<10 A) the total energy dissipated is approximately equal to 1/2LI² times the multiplier, V(BR)DSS/(V(BR)DSS-V_{DD}), which accounts for the additional transferred energy. For higher test currents the energy dissipated in the coil's resistance may also become significant, subtracting from what is dissipated in the device. In such cases, the exact amount of energy transferred to the test unit is somewhat difficult

FIGURE 5-1 — TYPICAL TEST CIRCUIT FOR UNCLAMPED INDUCTIVE SWITCHING

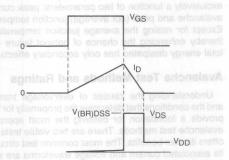


FIGURE 5-2 — WAVEFORMS ASSOCIATED WITH TEST CIRCUIT

A second test circuit is shown in Figure 3, and again circuit operation is simple. In this case, the MOSFET conducts a fixed, controllable current in avalanche. Since there is no inductor in this circuit, results are independent of the series resistance of the test coil and the magnitude of V_{DD}. An important feature of this method is that the junction temperature continually increases during the time of avalanche. Therefore, it is clear that the greatest stress occurs at the end of the avalanche pulse when the avalanche current and junction temperature are at their maximum values.

Determining the moment of maximum stress during a UIS test is difficult since peak current occurs at the beginning of the avalanche period when the junction temperature is at its minimum. Because the relationship between failure, instantaneous current, degree of hotspotting, and average junction temperature is not well understood, it is difficult to pinpoint the moment of maximum stress or to compare the stress in the UIS test to the stress in the constant current test. Nevertheless, the UIS test is preferred over other methods since it is easy to implement and already enjoys wide acceptance as a meaningful test method.

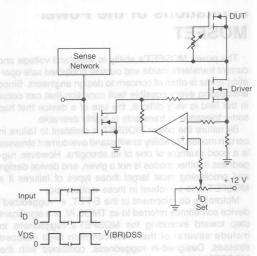


FIGURE 5-3 — ALTERNATE ASC TEST CIRCUIT THAT FORCES A CONSTANT CURRENT IN AVALANCHE

Stresses expected in the field should be used to guide the setting of UIS test conditions. Test currents should be equal to or greater than the continuous rating of the device. Junction temperatures should be elevated, bound only by the maximum rating.

There are two ways to achieve the elevated junction temperature specified in a UIS rating. The first is simply to externally heat the case of the device and the second is to begin the test at room temperature and raise the junction temperature by controlling the energy that the device under test must dissipate. However, in avalanche the many FET cells of the die may not share current evenly. This may cause the peak junction temperature to be much higher than the average. Consequently, forcing an elevated junction temperature with self heating tends to detect devices prone to hotspotting and is a more rigorous test.

Motorola's Avalanche Ratings

Motorola's E-series MOSFETs, which carry an "E" suffix, are designed to withstand the stress of drain-to-source avalanche. For E-FETs introduced to date, UIS failure can only be induced by either exceeding the device's pulsed current rating or its maximum junction temperature rating. With such a capability, an appropriate method of rating avalanche energy becomes clear. Current in avalanche is bounded by the pulsed current rating and energy dissipation is limited by thermal impedance and maximum junction temperature. The following example shows how the energy rating of the MTP3055E is calculated.

Consider the UIS rating of the MTP3055E specified at its continuous current rating of 12 A, a duty cycle of 1% and a case temperature of 25°C. For a typical V(BR)DSS of 70 V, peak power in avalanche is 840 W. For a maximum junction temperature rating of 150°C and a case

the transient thermal impedance $Z_{\theta JC}$ is calculated to be 0.149°C/W. From the thermal resistance rating of the MTP3055E ($R_{\theta JC} = 3.12^{\circ}$ C/W), r(t) is found to be equal to 0.048, a dimensionless number. The next step is to use the r(t) curve on the MTP3055E data sheet to determine the pulse width corresponding to an r(t) of 0.048. That pulse width, which is the time required to attain a 150°C junction temperature, is 38 μ s. The device rating, 32 mJ, is obtained by computing the avalanche energy corresponding to 840 W dissipated for 38 μ s. Similar computations yield ratings for other conditions such as elevated case temperature, other drain currents or multiple pulses. E-FETs introduced in the future are expected to have ratings that can be determined in a similar manner.

The above calculations are based on a constant current during avalanche, which is quite unlike the decaying avalanche current present in UIS testing. One way to determine coil size for UIS testing is to set the energy stored in the unknown coil equal to the energy rating calculated above. In this case the equation, W = 1/2 LI² [V(BR)DSS/V(BR)DSS – VDD], yields a inductance of 143 μH for W = 32 mJ, I = 12 Å, V(BR)DSS = 70 V, and VDD = 25 V. Although the energies are the same, the UIS test is slightly less rigorous since the avalanche interval is roughly twice as long as the time of avalanche during a constant current test.

Four points regarding UIS testing are worth mentioning here. First, a UIS rating per se does not guarantee the ultimate goal, system reliability. Several other variables such as average and peak junction temperature, the quality of system design and reliability of system components also affect Mean Time Between Failure (MTBF). Millions of bipolar and MOSFET circuits have very satisfactory MTBFs even though the UIS capability of their power devices is unspecified.

Second, UIS ratings apply to only a specific set of test conditions and predictions of ruggedness outside those conditions are speculative. For example, in some devices elevated junction temperature or higher avalanche currents may substantially reduce energy handling capability.

Third, although excessive V_{DS} is a common cause of MOSFET failure, the incidence of overvoltage transients should not be blamed for all power MOSFET failures. The list of potential causes is long and investigations into the reason for failure should not be limited to the one that is currently receiving all the attention in the press. A similar situation occurred in recent years when two other prevailing scapegoats — electrostatic discharge and dv/dt — were faulted for causing many more problems than they probably deserved.

Finally, some have stated that a UIS test is a guarantee of a device's ability to handle diode recovery stress, which is discussed in detail below. Although a device that is rugged with respect to avalanching usually has a broad "Commutating Safe Operating Area," there are exceptions to this rule. In some devices, areas of the die other than those associated with the parasitic bipolar affect

Drain-to-Source dv/dt Ratings

Static dv/dt washin who had TEREOM and northwarupo

Power MOSFET performance is eventually limited by extremely rapid changes in drain-to-source voltage. These very high dv/dts can disturb proper circuit performance and even cause device failure in certain situations.

High dv/dts occur under three conditions, and each has its own dv/dt threshold before problems arise. The first is called "static dv/dt" and occurs when the device is off and is intended to remain off. A voltage transient across the drain and source can be coupled to the gate via the drain-to-gate parasitic capacitance, C_{rss}. Depending on the magnitude of the gate-to-source impedance and the displacement current flowing into the gate node (i = C dv/dt), V_{GS} may rise above V_{GS(th)}, causing false turn-on.

Obviously, for this case dv/dt immunity depends to a large extent on the gate-to-source impedance. This dependence underscores the importance of proper gate termination to promote good noise immunity and is one of several reasons why operation of power MOSFETs with the gate open circuited is a poor practice. With its gate shorted to its source, all Motorola TMOS devices will withstand static dvDs/dts of greater than 30 V/ns, which is well in excess of values encountered in typical applications.

If the gate-to-source impedance is high and a voltage transient occurs between drain and source, false turn-on is more likely than device failure. Typically the transient will be coupled to the gate and cause the MOSFET to begin its turn-on. But as VGS rises and the MOSFET begins to turn on, the rise in VDS falters and the dv/dt is reduced. Thus, the phenomena is self-extinguishing and generally is not destructive to any circuit element.

Turn-on of the MOSFET's parasitic bipolar transistor, which is shown in Figure 4, is a potential route to device destruction due to static dv/dt. If the base-emitter shorting resistance is too large, displacement current flowing through C_{Cb} will lower the parasitic BJT's ability to sustain collector-emitter voltage. Although such a scenario is plausible, concerns about spurious BJT turn-on are generally unnecessary because the resistance of R_{be} is kept

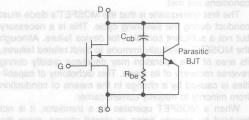


FIGURE 5-4 — INHERENT IN EVERY POWER MOSFET IS A PARASITIC BJT

low. Additionally, displacement current is lower at high voltage, when stand-off capability is most critical, because the magnitude of C_{Cb} falls with increasing V_{DS}. So, the dv/dt turn-on threshold cited above (greater than 30 V/ns) also applies to the MOSFET's parasitic BJT.

Dynamic dv/dt

The second mode in which dv/dt may be a concern occurs when the MOSFET abruptly interrupts current in an inductive load and an extremely rapidly-rising flyback voltage is generated. Since the vast majority of loads appear inductive at very high switching speeds, the device experiences simultaneous stresses imposed by high drain current, high VDS and displacement currents in the parasitic capacitances. Problems associated with this "dynamic dv/dt" (so named because the device is being switched off and is generating its own dv/dt) are evidenced by device failure.

Unless extraordinary circuit layout techniques are used (for example, hybrid circuits that minimize package and lead inductance) maximum attainable dv/dts in the dynamic mode range from 10 to 50 V/ns, depending on the V_{DSS} rating of the device. Among the various MOSFET types, maximum turn-off speeds do not differ widely and maximum attainable dv/dt is largely determined by the magnitude of the voltage that the drain can be switched through. Consequently, a 1000 V MOSFET can generate a greater dynamic dv/dt than a 60 V device, regardless of die size.

MOSFETs fabricated from all TMOS mask sets are tested and have been found to be immune to self generated dv/dts during very rapid, clamped inductive turnoff. The test circuit used has an extremely tight RF layout, and the switching speeds and dv/dts generated are assumed to be practical limits.

Diode recovery "dv/dt" and and anomul all mond

The third instance in which rapidly rising drain-to-source voltage has been thought to cause failure is during the reverse recovery of the MOSFET's intrinsic diode. Those that first studied this problem believed that dv/dt was the prime cause of failure, but more recent work has shown that dv/dt is only one of several factors that induce stress in a source-drain diode during reverse recovery.[1,2] Consequently, in this text these stresses are not classified strictly as dv/dt induced problems and the mode of stress is referred to as "diode recovery stress." Unlike the dv/dt modes discussed above, diode recovery stress is an occasional cause of system failure, but only when three specific conditions are met.

The first prerequisite is that the MOSFET's diode must conduct during the switching cycle. This is a necessary but not a sufficient condition for device failure. Although the MOSFET is virtually immune to dv/dt related failures, its area of safe operation may decrease greatly during reverse recovery of its diode. This dichotomy of capabilities is caused by a change in the means of conduction from minority to majority current carrier.

When a MOSFET operates as a transistor, it is not troubled by storage times or stored charge, since the MOSFET is a majority carrier device. Its diode, on the other hand, is a minority carrier device. Consequently, it

has forward and reverse recovery times due to the storage of minority carrier charge.

The second condition required to induce failure due to commutating stress is that charge stored during reverse recovery must be removed rapidly. Faster removal of charge increases current densities and peak electric fields. Since the turn-on speed of the transistor in the opposite leg of the half bridge has the greatest effect on the speed of commutation, it has a great influence on device stress.

The third and final requirement is that the stored charge must be extracted through a reapplied voltage of at least 30 to 50% of the device's maximum V_{DS} rating. During reverse recovery, as the diode is driven from forward to reverse conduction, the rapidly rising drain voltage forces the stored charge into the base of the parasitic bipolar transistor. If the resulting emitter current is sufficiently high, it can, in conjunction with the re-applied drain voltage, induce the phenomenon of avalanche injection[3], the cause of bipolar transistor "second breakdown."

The criteria above excludes most circuits as candidates for diode recovery problems. All single transistor topologies are immune, and many multiple transistor topologies are not subjected to commutation stress because the third condition is not met. The following examples help define which multiple transistor applications may develop problems. The first circuit is representative of the most commonly cited problem; the second is one in which commutating dv/dt is not normally a concern.

Consider the bidirectional DC motor speed controller illustrated in Figure 5. The direction of rotation depends upon which transistor receives the PWM signal at its gate; varying the duty cycle provides speed control. When one transistor is controlling motor speed, the opposite one is inactive as a MOSFET, but its diode serves as a commutating rectifier. To reduce audible noise, designers often operate their systems at frequencies greater than 20 kHz, so switching speeds are also high.

Reviewing the motor controller operation shows how turn-on of the drive transistor, in this case Q1, impresses commutating dv/dt stress on Q2's diode. A cycle begins with the turn on of Q1, which delivers current to the load. Q1 then turns off and remains off for the rest of the cycle,

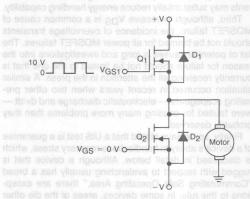


FIGURE 5-5 — A PWM DC MOTOR CONTROLLER IMPRESSES
DIODE RECOVERY STRESS ON THE POWER TRANSISTORS

and the inductive load draws current from the negative supply through D2. When Q1 turns on at the beginning of the next cycle, load current begins to be supplied by Q1 instead of Q2's diode. But of greater importance, Q1 also supplies the reverse recovery charge for D2. Current in D2 and Q2's drain-to-source voltage are shown in Figure 6. The time thought to be most stressful is also depicted in the figure. Note that the three elements required for diode recovery stress are present. The diode of Q2 is experiencing the combined stress of reapplied high voltage, presence of minority carriers, and rapid extraction of charge, as evidenced by high di/dt and dv/dt.

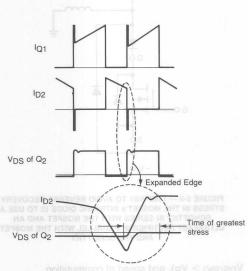


FIGURE 5-6 — TYPICAL WAVEFORMS IN A PWM DC MOTOR CONTROLLER

A second example, although it is in many ways similar to the first, is not usually subjected to commutating diode stress. It is the 1/2 bridge switch mode power supply, whose basic configuration is shown in Figure 7. The crucial difference between this system and the motor control circuit in Figure 5 is that the transistors are switching alternatively. Under normal operation one transistor will not turn on into a diode that is conducting current (which is a second, abbreviated, way to state the criteria for failure).

The idealized waveforms in Figure 8 show that output rectifiers D1 and D2 are the primary freewheeling rectifiers and the MOSFET diodes are essentially inactive. In reality, however, each intrinsic diode must clamp the energy in the transformer's leakage inductance when the opposite transistor turns off. Generally this is an acceptable situation since energies involved are small, diode conduction is brief, reapplied voltage is only a fraction of the device rating, and reverse recovery is slowed by parasitic inductance. Consequently, in these circumstances the intrinsic diode's commutation characteristics are usually not an issue.

For applications satisfying the three requirements, there are circuit solutions that deal with the problem if it occurs. One such approach is shown in Figure 9. Obviously, the intent of this circuit is to circumvent the MOSFET's limitations by not allowing the intrinsic diode to conduct and thereby accumulate stored charge. However, the higher parts count, additional cost and the voltage drop due to the diode in series with the FET are undesirable. Another solution is to limit dv/dt and voltage stress by using snubbers or by slowing the turn-on of the MOSFET in the opposite leg of the 1/2 bridge.

The optimum solution is to use devices that are indifferent to recovery stress and that have safe operating area curves that define and guarantee their capability. With the introduction of the E-FET, Motorola is making strides in both of these areas.

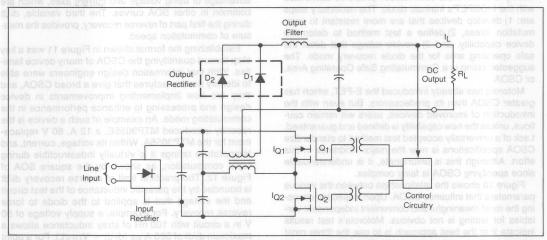


FIGURE 5-7 — ALTHOUGH THE MOSFETS INTRINSIC DIODES

ACT AS FREEWHEELING RECTIFIERS IN THE 1/2 BRIDGE

SMPS, THEY GENERALLY DO NOT EXPERIENCE DIODE

RECOVERY STRESS

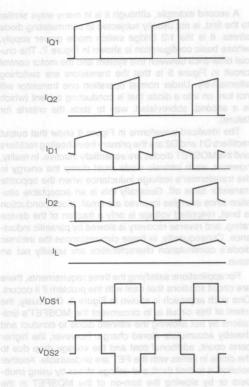


FIGURE 5-8 — TYPICAL WAVEFORMS OF A 1/2 BRIDGE SWITCHED-MODE POWER SUPPLY

Proposed CSOA Specification

One of the tasks before the power electronics community is to eliminate commutation problems associated with the MOSFET's intrinsic diode. The necessary steps are: 1) develop devices that are more resistant to commutation stress, 2) define a test method to determine device capability, and 3) provide ratings that detail the safe operating area for the diode recovery mode. The suggested rating is a Commutating Safe Operating Area, or CSOA.

Motorola has already introduced the E-FET, which has greater CSOA than its predecessors. But even with the introduction of improved devices, users will remain cautious, unless the new capability is defined and guaranteed. Lack of a universally accepted test method to standardize CSOA specifications is now the major hindrance in this effort. Although this is unfortunate, it is understandable since specifying CSOA is fairly complex.

Figure 10 shows the relationships between the various parameters that influence CSOA. Upon inspection choosing the most meaningful and convenient independent variables for testing is not obvious. Motorola's test results indicate that the best approach is to use the three most critical circuit dependent parameters. They are the forward current in the diode just before commutation (IFM), reapplied voltage (or peak drain-to-source voltage when

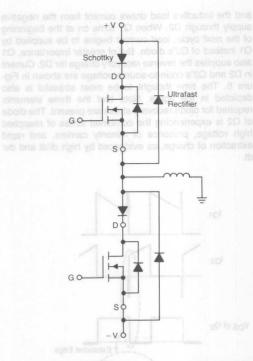


FIGURE 5-9 — ONE WAY TO AVOID REVERSE RECOVERY STRESS IN THE MOSFET'S INTRINSIC DIODE IS TO USE A SCHOTTKY IN SERIES WITH THE MOSFET AND AN ULTRAFAST RECTIFIER IN PARALLEL WITH THE MOSFET AND THE SCHOTTKY

VDS(PK) > VR), and speed of commutation.

An example of a CSOA specification for a 15 A, 60 V device is shown in Figure 11. This representation has the advantage of using voltage and current axes, which are common in other SOA curves. The third variable, di/dt during the first part of reverse recovery, provides the measure of commutation speed.

Establishing the format shown in Figure 11 was a key step toward quantifying the CSOA of many device families. With that information design engineers were able to identify device features that give a broad CSOA, and they are now implementing improvements in device design and processing to enhance performance in the commutating mode. An example of such a device is the recently introduced MTP3055E, a 12 A, 60 V replacement for the MTP3055A. Within its voltage, current, and temperature ratings it is virtually indestructible during rapid commutation, as shown by the square SOA of Figure 12. The practical limit of reverse recovery di/dt is bounded by the parasitic inductance of the test circuit and the voltage that is applied to the diode to force reverse recovery. For example, a supply voltage of 50 V in a circuit with 100 nH of stray inductance allows a maximum di/dt of 500 A/ μ s (di/dt = V_{DD}/L). For a point of reference, total D-S package inductance of the TO-220 is about 10 nH.

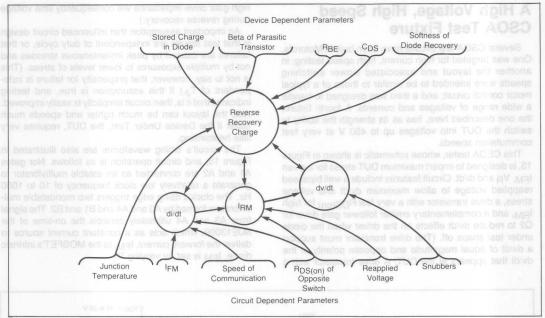


FIGURE 5-10 — DURING COMMUTATION MANY PARAMETERS
AFFECT TOTAL DEVICE STRESS

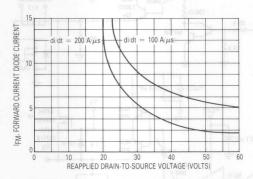


FIGURE 5-11 — TYPICAL COMMUTATING SAFE OPERATING AREA OF A 15 A, 60 V DEVICE NOT DESIGNED TO WITHSTAND DIODE RECOVERY STRESSES

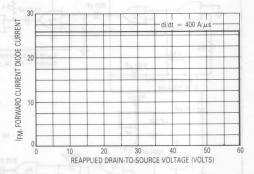


FIGURE 5-12 — COMMUTATING SAFE OPERATING AREA OF THE MTP3055E IS MUCH BROADER THAN ITS PREDECESSORS

Other methods of specifying diode recovery stress have been proposed. Using a single dv/dt value was the initial favorite because of its simplicity and the suspicion that failures are predominantly dv/dt induced. This idea was discarded for several reasons. First, devices do not fail solely due to dv/dt. In fact, when failures occur, they are rarely noted during peak dv/dt but are found later during maximum voltage stress and reduced dv/dt. Second, dv/dt varies considerably during reverse recovery and selecting a single representative value is difficult and too simplistic. Third, dv/dt during commutation is a function of

device characteristics and circuit conditions and is not something that the user can easily control, except with snubbers. Fourth, displacement current caused by diode recovery dv/dt is dwarfed by reverse recovery current, making the rate of extraction of stored charge much more important. Finally, some intrinsic diodes are much snappier than others (that is, the return of the diode current from the reverse recovery peak to zero is very abrupt and the rise in VDs to VR is very fast), and those diodes should have to withstand the dv/dts that they inherently create.

A High Voltage, High Speed **CSOA** Test Fixture

Several CSOA test circuits have been built at Motorola. One was targeted for high current, high speed testing; in another the layout and associated slower switching speeds were intended to be similar to those of a typical motor control circuit; and a third was designed to handle a wide range of voltages and currents. A fourth fixture, the one described here, has as its strength the ability to switch the DUT into voltages up to 450 V at very fast commutation speeds.

This CSOA tester, whose schematic is shown in Figure 13, is designed to impart maximum DUT stress for a given IFM, VR and di/dt. Circuit features include a well bipassed reapplied voltage to allow maximum dv/dt and voltage stress, a drive transistor with a very low RDS(on) for high IRM, and a complementary emitter follower gate drive for Q2 to reduce dv/dt effects on the driver when the diode under test snaps off. (The drive transistor must support a dv/dt of equal magnitude and opposite polarity of the dv/dt that appears at the DUT. A drive transistor with a

high gate drive impedance will consequently limit voltage during reverse recovery.)

An important assumption that influenced circuit design is that test results are independent of duty cycle, or that failures are caused by peak instantaneous stresses and not by multiple exposures to lower levels of stress. (This is not to say, however, that propensity for failure is independent of T_J.) If this assumption is true, and testing indicates that it is, then circuit simplicity is vastly improved. Also the layout can be much tighter and speeds much faster if the Device Under Test, the DUT, requires very little heatsinking.

The circuit's timing waveforms are also illustrated in Figure 13, and circuit operation is as follows. Nor gates A1 and A2 are connected as an astable multivibrator to generate a relatively low clock frequency of 10 to 1000 Hz. The clock's rising edge triggers two monostable multivibrators formed by A3 and A4 and B1 and B2. The signal from A3 and A4 ultimately controls the on-time of the MJE13009, which acts as a constant current source to deliver the forward current, IFM, to the MOSFET's intrinsic diode. IFM is set by varying R1.

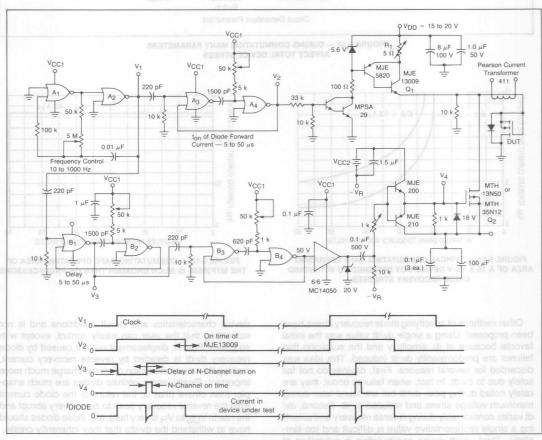


FIGURE 5-13 — SCHEMATIC AND TIMING WAVEFORMS OF A HIGH VOLTAGE, HIGH SPEED CSOA TEST CIRCUIT

The second monostable, B1 and B2, provides a delay before Q_2 is turned on. Minimum delay is set to 10 μ s to allow accumulation of stored charge in the diode's junction. After that delay the monostable formed by B3 and B4 sends a turn-on signal for 2 to 10 μ s. For the duration of the turn-on pulse, Q_2 applies reverse voltage to the DUT's source-drain diode and forcefully extracts reverse recovery charge. During reverse recovery the current burden of Q_2 includes the current delivered by the current source. After Q_2 turns off the current source is also gated off and the system remains at rest until the next cycle.

A few circuit features make device testing easier. First, the drain of the DUT is attached directly to the system groundplane. This greatly simplifies monitoring V_{DS} and improves measurement accuracy since using a differential measurement technique or floating an oscilloscope is unnecessary with this layout. Additionally, this method allows use of a probe tip adaptor that provides an excellent ground connection for the oscilloscope. These pains are needed because the magnitude of V_{DS} is the most important CSOA parameter and its rate of change can be greater than 10 V/ns.

A second mundane but very necessary feature is the capability of the circuit to withstand DUT failure. Current surges at failure are principally limited by the rDS(on) of the drive transistor Q₂ or its cut off current at the gate-to-source voltage that is applied. In either case the MOSFET's ruggedness with respect to current surges and the low duty cycle and limited on-time give the driver the margin of safety it needs to survive.

Using the CSOA Specification

The CSOA format was chosen to make the rating easy to relate to operating conditions in an application. The designer must only maintain V_{DS} and I_{FM} within specified limits and remember that di/dt is specified as a maximum allowable value. Pushing devices to their limit in a 1/2 bridge PWM DC motor controller produces failures that

track those seen in the CSOA testers. Therefore, the test method and circuit are appropriate for simultating stress in common applications. Nevertheless, designers should be aware of how important circuit parameters can skew the comparison.

Three other circuit parameters can degrade CSOA. They are solely under the control of the design engineer and are therefore difficult to include in a CSOA specification. The first is the gate to source impedance of the DUT. If RGS or LGS is high during reverse recovery, VGS can exceed VGS(th) due to the large dv/dt that the intrinsic diode generates. This dv/dt does not fully turn-on the MOSFET but forces it into the active region and slows the reverse recovery process, as seen in Figure 14. Since operating in this mode increases commutation power losses and clearly involves dv/dt turn-on (of the MOSFET, not the parasitic BJT), decreasing ZGS is normally the best approach. However, slowing reverse recovery with higher gate-to-source impedance can reduce VDS peaks and may even keep the device from avalanching, which is also shown in Figure 14.

Junction temperature is the second parameter that degrades CSOA. Although one might intuitively suspect that T_J has a first order effect on CSOA, test results to date indicate that it does not. These results are easier to believe when one recalls that RBSOA (Reversed Biased Safe Operating Area) of bipolars is also relatively independent of T_J. Another indication that T_J has a secondary effect is that DUT voltage and current waveforms are fairly constant as T_J changes. Varying other more dominant parameters often causes waveform changes that signal impending DUT failure.

The final parameter over which the circuit designer has strict control is the parasitic circuit inductance between the positive and negative rails of the 1/2 bridge. This inductance is unclamped and is likely to briefly avalanche the DUT at very high commutation speeds. In all cases this inductance should be minimized. The practical lower limit is in the 100 to 200 nH range.

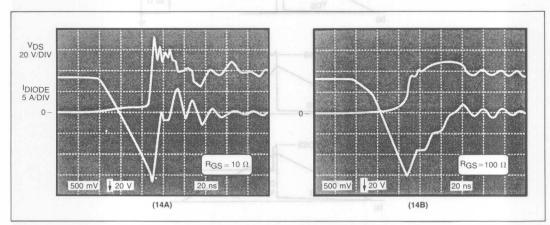


FIGURE 5-14 — IF THE MOSFET OF THE REVERSE RECOVERING RECTIFIER HAS A HIGH GATE-TO-SOURCE IMPEDANCE, REVERSE RECOVERY TIME IS LONG AND PEAK VOLTAGE STRESS IS LESS

Relationship Between CSOA and UIS

It is tempting to believe that a UIS test (Unclamped Inductive Switching) is an adequate substitute for a CSOA test. The argument given is that the common cause of device failure in the two modes is activation of the parasitic bipolar transistor due to high RBE, or base-emitter shorting resistance. Although this reasoning seems to make sense, it is flawed in two ways.

The first is that some devices may pass a UIS test and then fail in the commutating dv/dt mode due to device deficiencies other than high RBE. With its voltage termination rings, gate feeds, bonding pads and cell interconnections, the power MOSFET is much more than a few thousand paralleled cells. In some manufacturer's devices it is clear that these secondary structural features can limit performance in one test and not the other.

The second problem with correlation of UIS and CSOA test results is caused by a flaw in the present UIS test method. A study of UIS waveforms clarifies this point. As evidenced by different voltage waveforms in Figure 15, a device may react to overvoltage stress in at least three ways. Some devices fail immediately in avalanche and VDS collapses to about zero volts. Other MOSFETs can maintain their $V_{(BR)DSS}$ during the entire transient — if the current and pulse duration are not too great. In the third case, the drain-to-source voltage of some devices may collapse to a lower level. The lower voltage in avalanche is associated with activation of the MOSFET's parasitic bipolar transistor. Thus, the magnitude of V_{DS} during avalanche is the transistor's $V_{(BR)CEO}$.

If the UIS supply voltage is increased above V(BR)CEO, there is no mechanism to limit avalanche current and the

DUT normally fails. Therefore, the magnitude of the supply voltage can have a great effect on a device's energy handling capability. Improving the present UIS test method to detect devices that exhibit $V_{(BR)CEO}$ snapback is relatively simple. Instead of checking only for device failure, the V_{DS} waveform in avalanche can be sampled to ensure that it remains above the transistor's maximum V_{DS} rating.

As switching speeds and test currents increase in the commutating dv/dt mode, the device under test is likely to see overvoltage transients. During the final phase of reverse recovery the diode current is returning from its negative peak toward zero. This current can be thought of as decreasing drain current. If the diode recovers abruptly, or snappily, the associated di/dt can be extremely large, perhaps greater than 1000 A/ μ s. These rates of change in current are opposed by parasitic inductances, and the polarity of the induced voltages is such that they add to the reapplied voltage and increase the voltage stress on the DUT.

Figure 16 shows the reverse recovery waveforms of a 10 A, 50 V device from manufacturer "A." The effect of the device's $V_{(BR)CEO}$ is clearly evident. The clipping of the V_{DS} waveform at the device's $V_{(BR)CEO}$ (which corresponds to the value observed in UIS testing) and the coincident drain current show that the device is in avalanche. Even though the device passes this test, reliability in this mode of operation is uncertain since the parasitic bipolar is clearly being activated. If V_{R} is increased to greater than $V_{(BR)CEO}$, failure is likely. Because of its tendency to break back to a $V_{(BR)CEO}$, this device could fail in the commutating dv/dt mode, yet survive a UIS test.

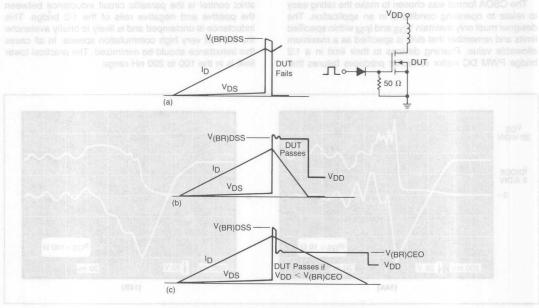


FIGURE 5-15 — A MOSFET CAN HAVE ONE OF THREE RESPONSES TO AN OVERVOLTAGE TRANSIENT

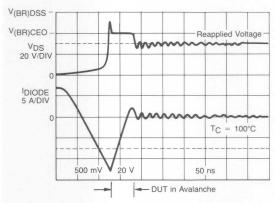


FIGURE 5-16 — COMMUTATION AT VERY HIGH SPEEDS CAN CAUSE AVALANCHING OF THE DUT

References:

- D. W. Berning and D. L. Blackburn, "Power MOSFET Failure During Turn-Off: The Effect of Forward Biasing the Drain-Source Diode," Proceedings of the 1986 IEEE Industrial Applications Society Annual Meeting, October 1986.
- K. Gauen, W. Schultz, "Proper Testing Can Maximize Performance in Power MOSFETs," EDN, May 14, 1987.
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- W. Schultz, K. Gauen, "Commutating SOA in Monolithic Freewheeling Diodes," *Powertechnics*, January 1986.
- The Power Transistor in Its Environment, Thompson-CSF, 1979.

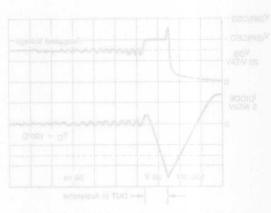


FIGURE 5-16 — COMMUTATION AT VERY HIGH SPEEDS CAN CAUSE AVALANCHING OF THE OUT

References

- D. W. Berning and D. L. Blackburn, "Power MOSFET Failure During Turn-Off: The Effect of Forward Blasing the Drain-Source Diode," Proceedings of the 1986 IEEE Industrial Applications Society Annual Meeting, October 1986.
- K. Gauen, W. Schultz, "Proper Testing Can Maximize Performance in Power MOSFETs," EDN, May 14, 1987.
- S. Krishna, and P. L. Hower, "Second Breakdown of Transistors During Inductive Turn Off," Proc. of IEEE, Vol. 62 March 1973
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- The Power Transistor in its Environment, Thompson-CSE, 1979.

Chapter 6: Gate Drive Requirements

Power MOSFET Gate Drive Requirements

Bipolar power transistors have been around for decades — drive circuits for these devices abound. Power MOSFETs are new arrivals. They differ from their bipolar counterparts especially in their input characteristics. These differences and their implications must be understood in order to insure that the MOSFET is operated in an optimum fashion.

Driving a power MOSFET is tantamount to driving a capacitive reactance network. Depending on the region of operation, the input "sees" either C_{iSS} , the Common-Source Input capacitance, or C_{rSS} , the Common-Source Reverse Transfer capacitance. C_{iSS} is the sum of the gate-to-source capacitance, C_{gS} , and the drain-to-gate capacitance, C_{dg} . C_{gS} is made up of a voltage independent capacitance between the gate structure and the source metallization and a gate-to-channel capacitance which varies significantly with operating conditions. C_{rSS} (C_{dg}) on the other hand, is mainly the MOS capacitance between gate and drain regions. Its value increases sharply during the latter stages of turn-on.

The device capacitances, especially the reverse transfer capacitance, and the gate-drive source impedance largely determine the device switching speed. Since the MOSFET input capacitances vary significantly with the die area, a given gate-drive will switch a smaller device such as the MTP5N06 more rapidly than the larger MTM15N40. However, two considerations complicate the task of estimating switching times. First, since the magnitude of the input capacitance, Ciss, varies with VDS, the RC time constant determined by the gate-drive impedance and Ciss changes during the switching cycle. Consequently, computation of the rise time of the gate voltage by using a specific gate-drive impedance and input capacitance yields only a rough estimate. The second consideration is the effect of the "Miller" capacitance, Crss, which is referred to as Cdg in the following discussion. An example best explains why it influences switching

When a high voltage device is "on," V_{DS} is fairly small and V_{GS} is about 15 V. C_{dg} is charged to $V_{DS(on)} - V_{GS}$, which is a small negative potential if the drain is considered the positive electrode. When the drain is "off" and is blocking a relatively high drain-to-source voltage, C_{dg} is charged to quite a different potential. In this case the voltage across C_{dg} is a high positive value since the potential from gate-to-source is near or below zero volts and V_{DS} is essentially the drain supply voltage.

During turn-on and turn-off, these large swings in gate-to-drain voltage tax the current sourcing and sinking capabilities of the gate-drive. In addition to charging and discharging C_{gs} , the gate-drive must also supply the displacement current required by C_{dg} (igate = C_{dg} dVDG/dt). Unless the gate-drive impedance is very low, the VGS waveform commonly plateaus during rapid changes in the drain-source voltage.

Input Capacitance

The traditional capacitance curves as shown in Figure 6-1 are somewhat meaningful, but they are not complete. Unfortunately, because they are incomplete, they can also be misleading. The fallacy of that presentation is that each capacitance is shown as a function of VDS and not as a function of the voltage across that capacitor. For Coss, Figure 6-1 is correct as shown because the independent voltage is VDS with VGS = 0 V. However, these curves are normally used to determine input impedance, and for Ciss and Crss the curves omit important information. A discussion of the variation of Crss with VDG best illustrates this point.

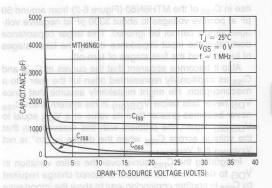


FIGURE 6-1 — THIS TRADITIONAL REPRESENTATION OF POWER MOSFET CAPACITANCES IS ACCURATE BUT NOT COMPLETE.

The first step towards understanding the variation of Crss with voltage is to study the change in VDG during the switching transition. When the device is off, VDS is essentially at the drain supply voltage. At that same time VGS is at or near zero volts, which means that VDG is a high positive value. When the device is in the "on" state, a quite different situation occurs. VGS is at roughly 10 V and VDS is at VDS(on). Therefore VDG is equal to VDS(on) — VGS(on), which is normally a negative value. It is this negative swing in VDG that the traditional curves do not address.

Now the importance of this additional information becomes evident. One possible presentation of the complete curve is given in Figure 6-2. The variables plotted on the abscissa (VGS and VDS) and the test conditions (VDS = 0 and VGS = 0) reflect the common source test circuit and the test conditions used to generate the two sections of the curves. Consequently, this is the format shown on Motorola's data sheets. A C_{TSS} (or C_{ISS}) versus V_{DG} curve is identical except that the voltage axis is simply V_{DG} , where V_{DG} takes on negative values to the left of zero and positive values to the right of zero. The dramatic

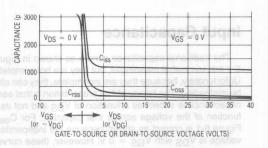


FIGURE 6-2 — EXPANDING THE TRADITIONAL CAPACITANCE CURVES TO SHOW THE VALUES OF Ciss AND Crss AS THE MOSFET MOVES INTO THE "ON" STATE GIVES A COMPLETE PICTURE OF THE CAPACITANCE VARIATION.

rise in C_{rss} of the MTH6N60 (Figure 6-2) from around 50 pF at positive voltages to about 3300 pF at negative voltages simply cannot be ignored. This larger capacitance dominates the input impedance during the latter stages of turn-on and the first stages of turn-off.

Also it becomes apparent that the curves of C_{rss} and C_{iss} as traditionally represented often lull the user into a misconception. He might mistakenly assume that since V_{DS} never falls below $V_{DS(on)}$ in his system, then C_{rss} never becomes greater than its value at a V_{DS} equal to $V_{DS(on)}$. Again, the problem with this reasoning is that the voltage across C_{rss} when the device is "on" is not $V_{DS(on)}$ but $V_{DS(on)} - V_{GS(on)}$.

Integrating the C_{rss} curve over the entire variation in V_{DG} to determine the amount of stored charge required by C_{rss} is another convincing way to show the importance of providing the complete capacitance curves. A rough piece-wise linear approximation suffices to illustrate this point. For the two regions above and below $V_{DG} = 0$ V, the charge required is roughly the change in V_{DG} times the average value of C_{rss} in each region. For a 480 V bus, for example, the charge to the right of zero is 24 nC

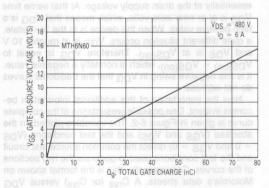
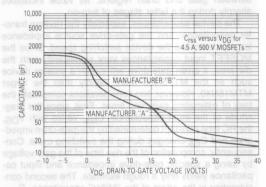


FIGURE 6-3 — INTEGRATING THE CAPACITANCE versus
VOLTAGE CURVES GIVES ACCURATE VALUES OF GATE
CHARGE

esumation of required gate drive.

Estimation of the amount of charge transferred to the gate-to-source capacitance is also enlightening. In this case Δ VGS is roughly 10 V and CgS (= CisS - CrSS) is about 1100 pF. The charge in this instance is 11 nC (= 1100 pF x 10 V). Interestingly, even though CgS is much larger than CrSS at a VDS of 25 V, CrSS under these conditions requires about four times as much charge. Also, integrating each of the two input capacitance curves over the change in voltage that each one sees as the MOSFET switches theoretically yields the required gate charge. From the numbers computed above (24 \pm 23 \pm 11), the required Qg is 58 nC, which closely tracks with the 10 V value (52 nC) shown in Figure 6-3.

One other problem area may arise when using capacitance measurements to compare input impedance of devices from different manufacturers. Typically, C_{iss} and C_{rss} are specified at a V_{DS} of 25 V, and comparisons at that value may be a poor indication of the relative sizes at other voltages. For instance, Figure 6-4 shows the C_{rss} curves of two 500 V, 4.5 A devices from different manufacturers. At a V_{DS} of 25 V the device from manufacturer



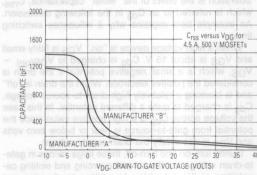
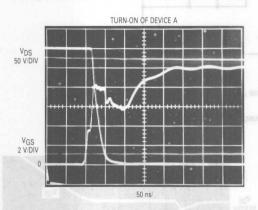


FIGURE 6-4 — SINCE CAPACITANCE CURVES OF DEVICES FROM DIFFERENT MANUFACTURERS SOMETIMES CROSS, USING A SINGLE VALUE OF CAPACITANCE TO COMPARE INPUT IMPEDANCE IS NOT A GOOD IDEA. IN THESE TWO FIGURES THE SAME INFORMATION IS SHOWN IN TWO DIFFERENT FORMATS.

"B" has a $C_{\rm rss}$ about 50% less than that of the device from manufacturer "A". However, the difference is actually pretty insignificant when compared to the large differences between values at other voltages. Note too that the curves cross and that overall the device from manufacturer "A" actually has the lower $C_{\rm rss}$.

Photographs of switching times in Figure 6-5 confirm what might be expected from a study of the complete

capacitance curves — device "A" is the faster switch. The gate charge waveforms shown in Figure 6-6 are a more dependable means of judging relative switching speed. For these reasons manufacturers are de-emphasizing the importance of capacitance specifications at a single value of VDS, namely 25 V. Circuits for testing the MOSFETs inter-terminal capacitances are given in Chapter 12.



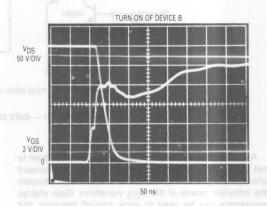


FIGURE 6-5 — ALTHOUGH DEVICE "B" HAS THE LOWER c_{rss} at a v_{DS} of 25 V, device "A" is the faster switch since its capacitance is lower at other voltages. $r_{GS} = 25~\Omega$, $r_{DD} = 5~A$, $r_{DD} = 300~V$

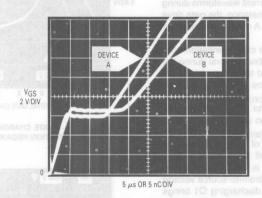


FIGURE 6-6 — GATE CHARGE WAVEFORMS ARE A MORE ACCURATE MEANS OF PREDICTING SWITCHING SPEEDS THAN CAPACITANCE SPECIFICATIONS. ID = 5 A, VDD = 300 V, IG = 1 mA

Gate Charge Specifications

Another means of specifying the size of the input impedance of a power MOSFET is to provide a gate charge curve. As the name suggests, such a curve indicates the amount of charge that must be supplied to the gate to effect the various stages of turn-on. These curves and the associated gate charge ratings are gradually replacing input capacitance specifications because of their simple format, ease of use, and the wealth of information they contain.

Understanding the gate charge test circuit aids in the interpretation of the gate charge waveforms. All gate charge test circuits, such as the one shown in Figure 6-7, employ a constant current source to charge the MOSFET's input capacitance. A constant IG ensures that C_{iSS} is charged at a fixed rate (i = q/t). The V_{GS} waveform then, is a representation of V_{GS} versus gate charge as well as V_{GS} versus time.

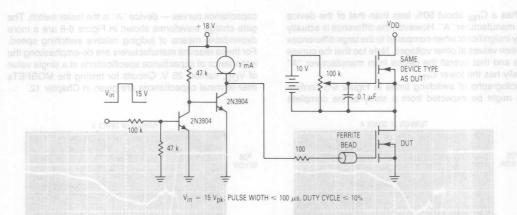


FIGURE 6-7 — GATE CHARGE TEST CIRCUIT

A second current source is usually used in the drain to set the desired drain test current. As will be discussed shortly, using a current source as a load helps sharpen the inflection points of the VGS waveform. Gate charge waveforms can be used to show turn-off behavior, but they are normally used to describe turn-on characteristics.

Figure 6-8 shows the gate-to-source voltage, the drain-to-source voltage and the drain current waveforms during turn-on of the MTP15N06. In this instance, the gate drive is a 1 mA current source and a 15 A current source is the load in the drain.

Each inflection point on the gate charge waveform defines the beginning or end of a distinct interval during the turn-on process. The time required to deliver charge Q1 to the gate is the turn-on delay time. At Q2 the drain-tosource voltage has fallen to VDS(on) and all switching is complete. When a charge equal to Q3 is supplied, the gate is charged to VGS(on) and no more gate charge is required. The magnitude of VGS(on) is somewhat arbitrary, but in this case a VGS(on) of 10 V requires 15.5 nC of gate charge. During turn-off the amount of time required to remove Q3 minus Q2 is the delay time. Removal of Q2 minus Q1 allows the drain-to-source voltage to rise to the supply voltage, and discharging Q1 brings VGS back to zero volts. Obviously, to satisfy conservation of charge, the charge supplied to the gate during turn-on is equal to and opposite that required for turn-off.

The slope of curve at any point can be interpreted as being the reciprocal of the capacitance during that portion of the switching interval (i = C dv/dt yields $C = \Delta \, Q_g/\Delta \, V_{GS}$). Even a brief look at a typical gate charge waveform reveals that the slope or input capacitance takes on at least three different values. As V_{GS} rises from zero volts, C_{iSS} is relatively small, which makes charging rather easy. During the next portion of the curve, the capacitance appears to be infinite since additional charge brings little, if any, change in V_{GS} . When the plateau ends, V_{GS} is free to rise again, but not nearly as fast as it did during the first interval. The capacitance curves and a description of the change in V_{DG} during the switching transition aid in explaining why there are three distinct slopes during the switching interval.

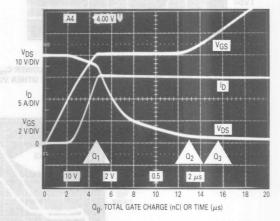


FIGURE 6-8 — GATE CHARGING WAVEFORMS ARE RIPE WITH INFORMATION REGARDING MOSFET SWITCHING

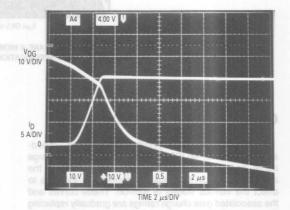
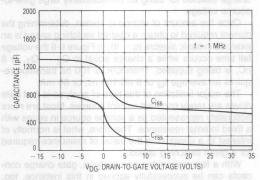


FIGURE 6-9 — AS V_{DG} APPROACHES ZERO VOLTS, SWITCHING SLOWS CONSIDERABLY DUE TO A DRAMATIC INCREASE IN C_{rss}.

The slopes of the gate charge waveform in the first and third intervals can be directly related to capacitance values shown on the capacitance curves. In the first interval the slope of the gate charge curve indicates that $C_{\rm iSS}$ is equal to 4 nC/7 V or about 570 pF. The similarity between this value and the magnitude of $C_{\rm iSS}$ in Figure 6-10 at higher voltages is not a coincidence. Until $V_{\rm GS}$ rises beyond $V_{\rm GS}(th)$, the MOSFET remains off and $V_{\rm DS}$ remains constant and equal to the supply voltage. Consequently, during this interval $C_{\rm iSS}$ is also constant.



vinsnibo Figure 6-10 — COMPLETE C_{iss} AND C_{rss} CURVES do on the part of the MTP15N06

On the other side of the plateau, C_{iSS} takes on a much larger value. There the change in charge divided by the change in VGS yields a capacitance of around 1300 pF. This corresponds to the value of C_{iSS} at drain-to-gate voltages below -5 V. Therefore, for circuit modeling in the first and third intervals of turn-on the magnitude of C_{iSS} can be estimated by measuring slopes of the gate charge waveform or by selecting values of C_{iSS} from opposite ends of the capacitance curve.

Estimation of C_{iss} during the plateau is also possible. Even though the slope of the curve is near zero, C_{iss} is not infinite as it may first appear. In this region the delta V_{GS} is approximately zero, so no charge enters C_{gs} . All the charge instead enters C_{rss} , which makes the magnitude of C_{rss} and its variation with V_{DG} the parameters of importance. The analysis is simplified somewhat if it is recognized that since $\Delta V_{GS} = 0$, $\Delta V_{DG} = \Delta V_{DS}$. That allows computation of C_{rss} from $\Delta Q/\Delta V_{DG}$ instead of $\Delta Q/\Delta V_{DG}$.

During the the VGS plateau there is a distinct change in the slope of the VDS waveform as the voltage nears VDS(on). In the first portion of the plateau $C_{\rm RS}$ is approximately 100 pF (4 nC/40 V), which appropriately corresponds to the highest drain-to-gate voltage in Figure 6-10. After that inflection point the turn-on process slows considerably, hinting of a much larger capacitance. Indeed, $C_{\rm RS}$ during the second portion of the plateau is roughly 7 nC/10 V or 700 pF. That value corresponds to a VDG of around -5 V on the $C_{\rm RS}$ versus VDG curve. So although $C_{\rm RS}$ varies throughout its entire range during the VDS transition, it could be modeled as taking on only a pair of values. One value would correspond to positive drain-to-gate voltages and a second figure for negative voltages.

The drain-to-gate voltage waveform associated with Figure 6-8 is shown in Figure 6-9. This photograph clearly shows that just before V_{DG} changes polarity the slope changes and switching slows due to an abrupt increase in C_{TSS} .

A look at the gate-to-source capacitance and its variation with VGS completes the analysis of how the input impedance varies during the switching cycle. From Figure 6-10 and the equation Cgs = Ciss-Crss, Cgs is easily determined. It is commonly assumed that Cgs is an invariant capacitor formed by the polysilicon gate and the source metallization. This belief is supported by the traditional representation of the capacitance curves. However, for many devices a large portion of Cgs is the capacitance between the gate and the channel, and this capacitance varies considerably as the device turns on.

The now familiar pattern of modeling the capacitor with two values reappears. From Figure 6-10 the value of Cgs before and during turn-on is nearly 500 pF whereas after turn-on it falls to less than 200 pF. As was previously shown for the MTH6N60, integrating these curves over the correct voltage ranges yields gate charge figures that are very close to data on gate charge curves.

There is some confusion regarding the slope of the V_{GS} waveform during the plateau region. It is often stated that during the plateau the slope is an indication of the gain of the device. This is true for resistive loads, but the reactive nature of the load also strongly affects the magnitude of the slope.

In many gate charge test circuits a MOSFET that is the same device type as the device under test is used as a constant current source in the drain. For an ideal current source the turn-on load line is capacitive, that is, the drain current reaches its steady state value just as the drain voltage begins to fall. Except for the premature dip in $V_{\mbox{\scriptsize DS}}$ due to the MOSFET being an imperfect current source, Figure 6-8 illustrates this phase relationship quite nicely.

Figure 6-8 also clearly shows that the slope of the V_{GS} waveform in the plateau region is zero. This should be expected from the load line shown in Figure 6-11. First I_D rises to 15 A before any appreciable change in V_{DS}. Then during the entire V_{DS} transition I_D is constant, requiring no change in V_{GS}.

Once the basic concepts of gate charge characterization are mastered, understanding the effect of varying load

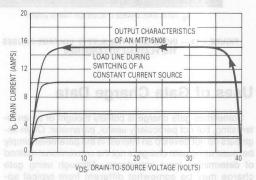


FIGURE 6-11 — CURRENT SOURCE YIELDS A CAPACITIVE LOAD LINE AT TURN-ON

current and supply voltage is simple. As ID increases, the required gate-to-source voltage, which is dictated by the transfer characteristics, also increases. As Figure 6-12 shows, this causes the plateau to occur at higher voltages. Figure 6-13 shows the effect of changing VDD. Varying VDD changes the potential through which C_{TSS} must be charged. The increased charge requirements account for the lengthening of the plateau at greater supply voltages.

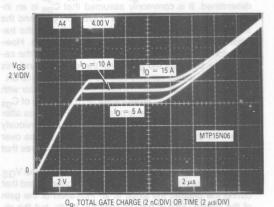
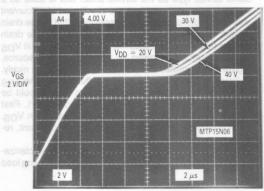


FIGURE 6-12 — INCREASING DRAIN CURRENT RAISES THE HEIGHT OF THE PLATEAU



Q₀, TOTAL GATE CHARGE (2 nC/DIV) OR TIME (2 μs/DIV)

FIGURE 6-13 — INCREASING THE SUPPLY VOLTAGE CAUSES THE PLATEAU TO LENGTHEN

Uses of Gate Charge Data

Sometimes gate charge is politely thought of as an interesting, but not particularly useful, parameter. Often engineers do not develop an interest in the parameter simply because using gate charge is not the conventional method of determining input impedance. Although using gate charge may be somewhat different from typical approaches, it is not difficult, and it certainly is a useful and informative specification.

Of course, the most straightforward use of gate charge data is to help determine the amount of charge that must be supplied to the gate to fully turn-on a device. That charge can be separated into three parts, each of which coincides with the requirements of a portion of the switching interval. The first portion defines the charge needed during the turn-on delay; the second indicates the charge necessary to effect the rise or fall of VDS; and the charge in the third region is associated with the turn-off delay. Also the curve clearly defines the penalty of additional charge exacted for using an unnecessarily large gate-to-source voltage.

Once the amount of charge is known, determining the current required to obtain a desired switching speed is an exercise in basic algebra (q = it). In Figure 6-8 the voltage fall time occurs while a charge equal to Q_2-Q_1 , or 8 nC, is being supplied. Therefore, a 100 ns transition requires an average Ic of 8 nC/100 ns, or 80 mA.

The major limitation of this type of analysis is that gate drives are rarely constant current sources. Most are more accurately represented as a voltage source in series with a fixed internal resistance. Therefore, what is normally of interest to a designer is the value of resistance required for a given switching speed.

With a few reasonable assumptions, gate charge concepts can be successfully applied in this instance, too. The basic concepts here are (1) except for extraordinarily fast switching speeds (<50 ns) the rise of the gate-to-source voltage stalls in a plateau region, regardless of the type of gate drive and (2) the drain-to-source voltage excursions occur during the plateau of Vos.

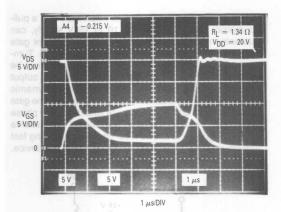
When the gate voltage stalls during turn-on, the voltage across the gate drive resistance is simply V_{GG} – V_{GS}(plateau) and I_G is equal to this voltage drop divided by the drive impedance (Figure 6-14c). The nearly constant I_G during the fall of V_{DS} is shown in Figure 6-14b. This provides the link to the use of gate charge data.

Suppose, for example, that the desired VDS fall time during turn-on of the MTP15N06 is 2 μ s. This time and the 8 nC of required gate charge, which is the charge during the plateau of Figure 6-12, fix the necessary gate drive current at 4 mA (8 nC/2 μ s). For a 10 A load the plateau occurs at a VGS of 7.5 V, and with a 10 V gate drive the potential across the gate drive internal impedance is only 2.5 V. These figures yield a gate resistance of 620 ohms (= 2.5 V/4 mA). As the oscilloscope waveforms of Figure 6-14 show, this method of selecting gate drive impedance is fairly accurate. As expected, decreasing the gate drive impedance by a factor of ten brings a tenfold decrease in switching time.

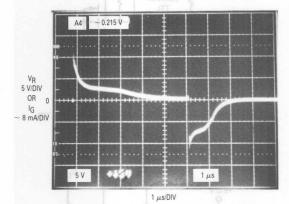
It is also enlightening to pursue the reason for the more rapid turn-off in Figure 6-14 even though the gate drive impedance at turn-on and turn-off are the same. The answer is simple; the gate current is greater due to a higher potential across the internal impedance. The current during the turn-off plateau is VGS(plateau) $^-$ VGS(off) divided by RG. In this case the numbers are (7.5 $^-$ 0 V) \div 620 ohms, or about 12 mA, instead of the 4 mA at turn-on. As it should be, the ratio of currents is proportional to the switching speed.

The second major benefit of the concept of gate charge is that it enhances understanding of the MOSFET's switching behavior. Three examples prove this point. First,

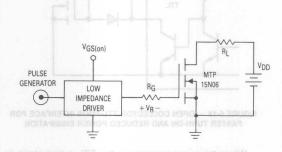




(a) GATE-TO-SOURCE AND DRAIN-TO-SOURCE VOLTAGE WAVEFORMS DURING RESISTIVE SWITCHING



(b) GATE CURRENT



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FIGURE 6-14 — BECAUSE THE GATE-TO-SOURCE VOLTAGE
AND GATE CURRENT ARE RELATIVELY CONSTANT DURING
THE V_{DS} EXCURSIONS, GATE CHARGE CAN BE USED TO
ESTIMATE GATE DRIVER IMPEDANCE FOR A DESIRED
SWITCHING SPEED.

understanding that the MOSFET is controlled by gate charge helps in predicting the effect of the gate drive impedance on switching speeds. Theoretically, halving the impedance of the gate drive should double the rate of charging and halve the switching times. This has been shown to hold true over a five decade change in gate drive current

Second, the concepts reveal the weakness of using or specifying only the values of capacitance at a single point on the capacitance versus voltage curves. And third, they show that even though CGS is the larger of the input capacitances at a VDS of 25 V, CrSS has the greater effect during most of the switching interval.

A more subtle benefit of the gate charge curve is that it provides the data required for accurate device modeling. As was shown earlier, the input impedance and the switching behavior of the MOSFET can be modeled by selecting values of C_{TSS} and C_{gS} from the slopes of the gate charge waveform. Using these values yields results that are much more meaningful than those obtained by using a single value of each capacitor at V_{DS} of 25 V.

The trend towards the use of higher switching frequencies in such applications as the series resonant power supply make estimation of required gate charge and transferred energy of increasing importance. As operating frequencies increase, the MOSFET's "high input impedance" eventually consumes substantial drive current. Charging and discharging $C_{\rm ISS}$ (and $C_{\rm OSS}$) every cycle can result in an energy loss large enough to affect overall efficiency. In addition to its other more common uses, the gate charge curve also helps in estimating the energy consumed by the gate.

The familiar formulas, $E=1/2~CV^2$ and 1/2~QV, apply only to fixed values of capacitance. For voltage dependent capacitors such as the $C_{\rm ISS}$ of the power MOSFET, the gate voltage versus gate charge curve must be integrated between $V_{\rm GS}({\rm off})$ and $V_{\rm GS}({\rm on})$ to determine transferred energy. This energy is stored in $C_{\rm ISS}$ during turn-on and is normally lost when the gate is clamped to the source at turn-off. Multiplication of this energy by the switching frequency gives the associated power loss.

For example, consider the energy stored in the input capacitance of the MTM15N50. For a V_{GG} of 10 V the area under the curve in Figure 6-15 is 0.625 μ J. This loss

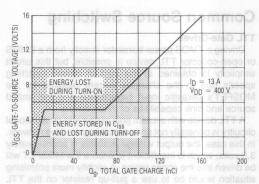


FIGURE 6-15 — THE GATE CHARGE CURVE OF THE MTM15N50 GIVES INFORMATION REGARDING THE ENERGY CONSUMED WHILE DRIVING THE MOSEFET'S GATE.

normally goes unnoticed even though this device is one of the largest available. Even at a switching frequency of 1 MHz, the dissipated energy is only 0.625 watts. Note, however, that if the gate is driven to a V_{GG} of 16 V then the losses rise to 1.275 μJ and 1.275 W.

Yet to be included in this analysis of drive losses is the energy consumed by the gate drive as it delivers the required gate charge. Figure 6-16 shows the equivalent circuit of an idealized gate drive network in which S₁ completes the charging path and S₂ controls discharging.

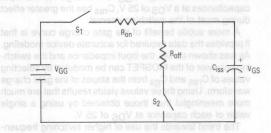


FIGURE 6-16 — IDEALIZED GATE DRIVE CIRCUIT

Regardless of the magnitude of the equivalent resistance and the rate of charging, the size of C_{iSS} and $V_{GS}(on)$ determine the energy transferred during turn-on and dissipated at turn-off. Likewise, the energy dissipated in R_{On} is also independent of the size of R_{On} and the gate drive current. Again, integration of a Q versus V curve gives energy, but this time the appropriate voltage is $V_{GG}-V_{GS}$. This integration is equivalent to finding the area between the gate charge curve and $V_{GS}=V_{GG}$.

Now the picture of the gate drive losses is complete. Total losses are simply VGS(on) times the required gate charge.

Common Source Switching

TTL Gate-Drives

Driving a TMOS power transistor directly from a CMOS or open-collector TTL device is possible, but this circuit simplicity is obtained at the cost of slower switching speeds due to the charging current required by the MOSFET's parasitic input capacitance and the limited source and sink capabilities of these drivers.

A TTL device with a totem pole output and no additional circuitry is generally not an acceptable gate-drive network. In this case, the output voltage available is approximately 3.5 volts, which is insufficient to ensure the MOSFET will be driven into the ohmic region. A slightly more promising situation would be to use a pull-up resistor on the TTL output to utilize the entire 5.0 V supply, but even the full 5.0 V on the gate would not guarantee the MOSFET will conduct even half of its rated continuous drain current.

The open-collector TTL device, when used with a pull-up resistor tied to a separate 10 to 15 V supply, can guarantee rapid gate turn-off and ensure sufficient gate voltage to turn the MOSFET fully on (Figure 6-17). Turnon is not as rapid because the pull-up resistor must be sized to limit power dissipation in the lower TTL output transistor. However, when concerned about dynamic losses incurred while switching an inductive load, the gate fall time is more critical than the rise time due to the phase relationship between the drain current and drain-source voltage. Figure 6-18 shows a configuration providing fast turn-on, yet reducing power dissipation in the TTL device.

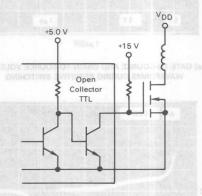


FIGURE 6-17 — DRIVING TMOS WITH OPEN COLLECTOR TTL

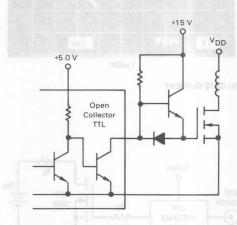


FIGURE 6-18 — OPEN COLLECTOR TTL-TMOS INTERFACE FOR FASTER TURN-ON AND REDUCED POWER DISSIPATION

When the lower transistor in the TTL output stage is turned on, shunting the MOSFET input capacitance to ground, modeling the bipolar as a saturated device may not be appropriate. The current sinking capabilities of TTL devices in the low output state is limited by the beta of the pull-down transistor and its available base current, which varies with the product line and TTL family. Table 1 shows the current source and sink capabilities of various TTL families.

Although the TTL peak current sinking capability might be twice the continuous rating, faster turn-off can be achieved by using an outboard transistor to clamp the gate-to-ground (Figure 6-19). In this configuration, the bipolars are operating as emitter followers. As such, they are never driven into saturation and their associated storage times do not significantly affect the switching frequency limit.

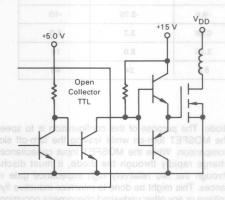


FIGURE 6-19 — OPEN COLLECTOR TTL DRIVING PROPERTY OF DESCRIPTION O

CMOS Gate Drives

Driving the power MOSFET directly from CMOS presents a different set of advantages and disadvantages. Perhaps most important, CMOS and power MOSFETs can be operated from the same 10 to 15 volt supply. A gate voltage of at least 10 volts will ensure the MOSFET is operating in its ohmic region when conducting its rated continuous current. This benefit allows the designer to directly interface CMOS and TMOS without any additional circuitry including external pull-up resistors. Again, however, circuit simplicity results in slower MOSFET switching due to the limited current source and sink capabilities of CMOS devices. Table 2 compares the output current capabilities of standard CMOS gates to that of the CMOS buffers (MC14049, 14050). Note that while the current sinking capacity of the buffers is improved significantly over that of the standard CMOS gate, the current sourcing capacity is not. The figures in Tables 1 and 2 indicate the current at which the device can still maintain its output voltage within the proper logic level for a given logic state.

TABLE 1 — TTL Output Current Source and Sink Capabilities

	edep sonermo Output Drive beau							
Family	High (Source)	Low (Sink)						
74LS00	0.4 mA	8.0 mA						
7400	0.8 mA	16 mA						
9000 emil e	mize Am 8.0 off stora	16 mA						
74H00	1.0 mA	20 mA						
74500	1.0 mA	20 mA						

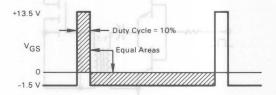
As an illustration, with a VDS of 15 V, a standard CMOS gate can typically source 8.8 mA in the HIGH state without its output falling below 13.5 volts.

If the switching speeds of CMOS buffers are not rapid enough, the discrete buffers suggested for use with TTL devices (Figures 6-18 and 6-19) can also be used to interface CMOS to TMOS. The only difference is the pull-up resistors are unnecessary for CMOS. Another difference in the two technologies that may affect the maximum switching frequency limit is that the TTL gates typically have faster switching times.

Other Gate Drives

In certain situations pulse transformers are an effective means of driving the gate of a power MOSFET. They provide the isolation needed to drive bridge configurations or to control an N-Channel MOSFET driving a grounded load. One of the simplest examples of such a circuit is the first circuit in Table 3 where the rise, fall, and delay times for this and the other circuits to be discussed are tabulated.

The diode in Circuit 1 is present simply to limit the flyback voltage appearing across the drive transistor Q1. A transformer turns ratio of one-to-one was chosen to provide an appropriate voltage at the secondary given the 15 volt primary supply voltage. A potential problem with this circuit is that the duty cycle influences the magnitude of VGS because the volt-seconds produced during the on and off intervals at the secondary must sum to zero. Figure 6-20 indicates that increasing the duty cycle decreases the maximum gate-source voltage. As the duty cycle increases above 33%, for the given primary voltage of 15 volts, the peak gate voltage falls below 10 volts and may eventually drop to a point where the device is no longer operating in the ohmic region. Increasing the primary voltage to 20 volts would increase the maximum allowable duty cycle.



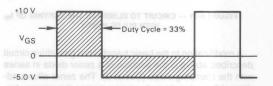


FIGURE 6-20 — VARIATION OF V_{GS} WITH DUTY CYCLE IN PULSE TRANSFORMER GATE-DRIVE

The basic pulse transformer topology of Circuit 1 also has both maximum and minimum pulse width limitations in addition to those imposed by the volt-seconds requirements. The current in the primary winding may ramp-up to excessive levels due to magnetic saturation, especially

ssled for u	buffers sugge	V _{DD}	Min (mA)	Typ (mA)	Min (mA)	Typ (mA)
Current	V _{OH} = 2.5 V	5.0 V	-2.1	-4.2	-1.25	-2.5
Source	V _{OH} = 9.5 V	10 V	ult.feaister	-2.25	-1.25	-2.5 Jim
Capability	V _{OH} = 13.5 V	15 V	-3.0	-8.8	-3.75	-10
Current	V _{OL} = 0.4 V	5.0V	0.44	0.88	3.2	6.0
Sink	V _{OL} = 0.5 V	10 V	obler Gar	2.25	8.0	16
Capability	V _{OL} = 1.5 V	15 V	3.0	8.8	24	40

in the smaller pulse transformers, if the pulse width is too wide. On the other hand, very short pulse widths may cause two different problems. First, transformer leakage inductance may limit current sourcing capability during a significant portion of the turn-on interval of a very small pulse width. Second, the pulse width must be wide enough to allow the magnetizing current (I_m) to ramp-up significantly, because the stored energy (defined by the current in the magnetizing inductance) provides turn-off drive to the MOSFET gate. To eliminate the problem of I_m varying with pulse width and to improve turn-off drive, the circuit shown in Figure 6-21 may be used.

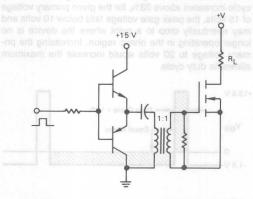


FIGURE 6-21 — CIRCUIT TO ELIMINATE THE VARYING OF $I_{\rm m}$ WITH PULSE WIDTH

A modification to the basic transformer gate-drive circuit described above is the addition of a zener diode in series with the clamping diode (Circuit 2). The zener allows additional flyback voltage to appear across the primary terminal, when Q1 is turned off. When this additional potential is induced across the secondary, it initially provides greater reset voltage levels and, thus, more rapid gate turn-off. Naturally, inherent in this circuit are the same duty cycle, pulse width and frequency limitations that accompanied Circuit 1.

Circuit 3 is very similar to Circuit 1 except the gate resistances are scaled upward and one is shunted by a

diode. The purpose of this configuration is to speed up the MOSFET turn-on while leaving the turn-off slow in comparison. While the MOSFET input capacitance can charge rapidly through the diode, it must discharge through the two relatively high impedance gate resistances. This might be done to minimize inductive flyback voltage or any other undesired phenomena occurring during very rapid turn-off.

A variation of the push-pull converter is used to drive the gate of the MOSFET in Circuit 4. When Q1 is turned on, the 10 volts across the lower of the two primary windings induces the same potential in N2. The voltage seen at the secondary, due to the 2:1 step-down ratio (N1 + N2/N3), equals the primary supply voltage. At turn-off, the potential across N2 reverses and is clamped to the 10 V supply by D1. Now N2 induces its voltage in N1 and the potential appearing at the secondary reverses in polarity but the magnitude is still 10 volts. If the pulse width is long enough to generate sufficient magnetizing current, this circuit yields good current sinking capabilities.

Two opto-coupled drive circuits are shown in Circuits 5 and 6. Circuit 5 is one of the most straightforward ways of developing a low impedance gate-drive from the output of the optocoupler. This circuit, however, is plagued by long switching delays that limit the useful operating frequency. These delays are inherent in the optocoupler and their magnitudes are affected by the phototransistor's output load impedance. If this impedance is lowered, as accomplished with Circuit 6, the gate-drive turn-off delay is significantly lower. Besides the complexity of these circuits, especially Circuit 6, the gate-drive's bipolar output transistor, Q2, must remain on the entire time that the MOSFET is off. The energy dissipated in these two drivers during low duty cycle operation may be critical if efficiency is a major concern.

Circuits 7 and 8 are similar versions of a circuit that can be used as a high performance gate-drive. The base currents for the bipolar drives must be push-pulled as shown in Figure 6-22. MOSFET turn-on is initiated during a positive transition of the input pulse. Q1 is turned on, supplying the required base current for Q3, which is Baker clamped to minimize its turn-off storage time. Both circuits have excellent turn-on times because of the low impedance path provided between the supply and the gate of the MOSFET.

	TABLE 3 — Switching Speeds		Gate Switching Times (ns)				0	rain Switc	hing Times (na)
Performance Push-Pull Circuit	of Various TMOS Gate Drives		Turn-on Delay (V _{in} vs V ₁)	Turn-on Rise Time	Turn-off Delay (V _{in} vs V ₁)	Turn-off Fall Time	Turn-on Delay (V _{in} vs V ₂)	Turn-on Fall Time	Turn-off Delay (V _{in} vs V ₂)	Turn-off Rise Time
	119 A									
Circuit 1 Simple Pulse Transformers	*15 V V1 V	100 100	15 \$3,00	85	35 490	230	25 3900	25	185 250	20
Circuit 2 Pulse Transformer w/Flyback Zener	115 V V1 0 V2	V 0.55	3800 15	90	25	190	30	25	125	35
Circuit 3 Pulse Transformer	115 V V1 V1 V1 V2	With Diode D1	30	95	220	1250	60	35	640	230
w/Speed-up Diode	V _{ino} oi oi one 1 2 de pures (comuned)	Without Diode D1	[V ₁₀ vs V ₁)	1500 ₀₁₁	280	1100	(A ^{III} A2 A ^S)	340 ou	660	230

TABLE 3 — Switching Speeds		DI	(ate Switcl	ning Times (ns)	D	rain Switc	hing Times (ns	:)
of Val	of Various TMOS Gate Drives (continued)		Turn-on Delay (V _{in} vs V ₁)	Turn-on Rise Time	Turn-off Delay (V _{in} vs V ₁)	Turn-off Fall Time	Turn-on Delay (V _{in} vs V ₂)	Turn-on Fall Time	Turn-off Delay (V _{in} vs V ₂)	Turn-off Rise Time
CHURCH 3 CITCUIT 4 Quasi Push-Pull Transformer Drive	01 N ₂ 1.11 V ₁ 1.10 V ₂ 1.8 V ₁ 1.0 V ₂ 1.0 V ₃ 1.0 V ₁ 1.0 V ₂ 1.0 V ₂ 1.0 V ₁ 1.0 V ₂ 1.	Wirth Diode D1	30 15	85	40	230	30	25	160	35
Circuit 5 Standard Opto-Coupling Circuit	V _{CC} 33 k 240 11 100 V ¹ 1 V ₁₀ 750 750 750 15 k	o ∨ 0 ∨ 0 ∨ 0 ∨ 0 ∨ 0 ∨ 0 ∨ 0 ∨ 0 ∨ 0 ∨	3900	460	1600	140	4000	80	1750	20
Circuit 6 High B.W. Opto-Coupling Circuit	VCC 100 V1 1 k 4N25 6535 03 (1 350) 01 3350		3700	420	450	120	3800	75 52	520	20
Circuit 7 High Performance Push-Pull Circuit	115 V V V V V V V V V V V V V V V V V V		New-on Delay Tuon-on	3 atta 5 wito 1 win en 60	25	30	10 30 A ³)	20	Turn-off Turn-off (Vin 42 V2)	15 1mm-oi

TA	ABLE 3 — Switching Speeds		Gate Switc	hing Times (ns)	D	rain Switc	hing Times (ns)
of Vario	ous TMOS Gate Drives (continued)	Turn-on Delay (V _{in} vs V ₁)	Turn-on Rise Time	Turn-off Delay (V _{in} vs V ₁)	Turn-off Fall Time	Turn-on Delay (V _{in} vs V ₂)	Turn-on Fall Time	Turn-off Delay (V _{in} vs V ₂)	Turn-off Rise Time
	*Transformer Space:								
Circuit 8 High Performance Push-Pull Circuit	V _{in} O1 V _i O2 470	20	60	45 430	70	40	25	85	15
Circuit 9 Low Power Schottky TTL	1/6 SN74LS05 VI	110	5000	60	600	480	1000	375	150
Circuit 10 Paralleled Low Power Schottky TTL	3/6 SN74LS05	45	1800	30	210	180	310	140	50
Circuit 11 Paralleled SN7407 Buffers with Pull-Up	15V V2	30 25 (A ^[4] As A ⁴)	710	30 30	140	60 60 80	60	130 (A ^(t) As A ^(S))	30
Resistance	na two described appears	Turn on Delay		ng Times (ns) Turn off Dolay	Turn-off Fall	Turn on Delay	Turn-on Fall	Turn off Delay	Turn off Rise

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	TABLE 3 — Switching Speeds		Gate Switc	hing Times (ns			Drain Switc	hing Times (n	s)
of Val	rious TMOS Gate Drives (continued)	Turn-on Delay (V _{in} vs V ₁)	Turn-on Rise Time	Turn-off Delay (V _{in} vs V ₁)	Turn-off Fall Time	Turn-on Delay (V _{in} vs V ₂)	Turn-on Fall Time	Turn-off Delay (V _{in} vs V ₂)	Т
Circuit 12 SN7407 Buffer Driving a	15 V V R1 = 2.0 k	30	140	20	20	50	20	40	
Complementary Emitter-Follower	SN7407 R1 = 5.1 k	60	430	20	20	110	40	40	The second second second
Circuit 10	6 6 MC14049 V	9)							
Circuit 13 Six Paralleled CMOS Inverters (MC14049UB)	V ₁₀ V ₂₀₀ V ₂ V ₁ V ₁ V ₁	30	920	20	130	100	160	90	
Circuit 14 Dual Peripheral Driver MC1472)	-50 V -15 V -V	370 30	100	170 18	80 20	280	50 52	230	
of Var	*Transformer Specs: Ferroxcube 3019P3CB $N_1 = N_2 = N_3 = 10$ Turns #19 Trifilar Wound $L_p \approx 0.6$ mH	Turn-on Delay (V _{fin} vs V ₁)	Turn-on Rise Time	Turn-off Delay (V _{In} vs V ₁)	Turn-off Fall Time	Turn-on Delay (V _{In} vs V ₂)	Turn-on Fall Time	Turn-off Delay (V _{(n} ve V ₂)	

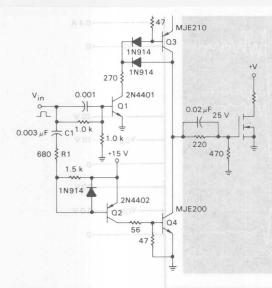


FIGURE 6-22 — PUSH-PULL BASE DRIVE FOR CIRCUITS 7 AND 8

Turn-off occurs when the falling edge of the input pulse is differentiated by the series combination of R1 and C1, thus turning on Q2. Base current is then free to flow into Q4, clamping the gate-to-ground or a negative potential. The duration of the clamping interval may be adjusted by varying the RC network. Before the occurrence of another input pulse, the MOSFET will remain off due to the 470 Ω gate-source resistance.

Circuits 9 through 12 are examples of how TTL devices may interface with the TMOS power MOSFET. The first of the circuits, number 9, has a very simple interface beinverter from excessive power dissipation when the TTL output is low. Putting three such buffers in parallel, Circuit 10, reduces all the associated switching times by a factor of nearly two-thirds.

Another TTL device with an open collector output is utilized in Circuit 11. Two of the six buffers in the SN7407 operate in parallel with only a pull-up resistor and the gate of the MOSFET connected to the collector of the high voltage (30 volts) output transistors. The associated switching times are quite respectable given the simplicity of the drive circuit.

Another application of the SN7407, as mentioned earlier, is to use it to drive a discrete complementary emitter-follower buffer (Circuit 12). Lowering the pull-up resistor, R1, increases the turn-on speed at the expense of increasing gate turn-off power dissipation.

Figure 6-23 shows an MTM12N10 being driven by a CMOS MC14050CL Hex Buffer. To obtain the maximum output current source and sink capability, all six buffer elements are paralleled.

While the pull-up resistor is not a necessity (as it is with open-collector TTL devices), it does balance the current source and sink capabilities of the CMOS buffer. Without that resistor, one could expect slower turn-on but the drive circuit would be more efficient because the CMOS device no longer must sink the current drawn through R1 when the CMOS outputs are low. Of course, fewer than the six paralleled inverters could be used at the cost of slower switching. Figure 6-24 shows the switching waveforms without a pull-up resistor. For the six buffer elements in parallel the peak I_G during turn-on is about 350 mA and 900 mA during turn-off.

While not as fast as other more elaborate drive circuits, the MC14050CL offers an inexpensive single power supply device that interfaces directly to CMOS and MHTL circuitry.

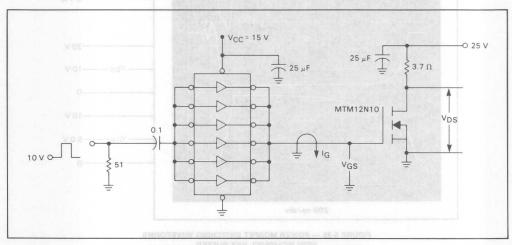
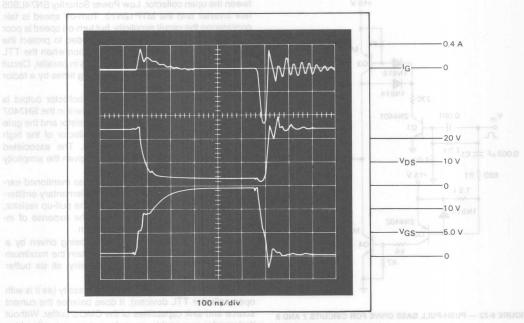
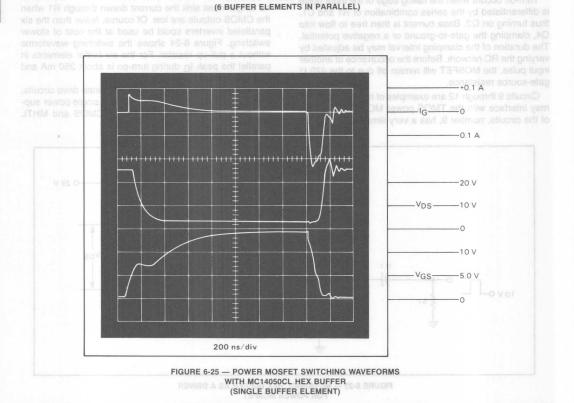


FIGURE 6-23 — MC14050CL HEX BUFFER AS A DRIVER FOR POWER MOSFET



evinb erlitud no-mul newole Jodko Figure 6-24 — POWER MOSFET SWITCHING WAVEFORMS
solved SOMO and seusped insignified and medical with MC14050CL HEX BUFFER



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Figure 6-25 shows the results of the MTM12N10 being driven by a single MC14050CL buffer element. Note the time scale has been doubled to allow V_{GS} to rise to its upper rail. The gate current scale is a factor of four smaller: peak gate currents of about 70 mA during turn-on and 240 mA during turn-off are seen.

Several ICs that were originally intended for other applications have been adopted by some circuit designers looking for fast, yet simple and efficient MOSFET gatedrive schemes. One such device is the MC1472, a dual peripheral driver, designed to interface MOS logic to high current loads such as relays, lamps and printer hammers. Because each of the two output transistors can sink 300 mA, MOSFET turn-off times are short when this device is used in a gate-drive network. Turn-on times are also short in Circuit 14 because the value of R1 is so low that it only minimally impedes the current during the charging of the MOSFET input capacitances. The advantage of this large current sourcing capability is once again offset by the significant currents that will flow whenever the MC1472 output is low to turn the MOSFET off. In fact, for the 25 ohm pull-up resistor and a V_{CC1} of 15 volts, that

current approaches the combined sinking capabilities of the two output transistors in that package.

The DS0026 Clock Driver has been designed to drive high capacitance loads. It features a peak output current of 1.5 A and transition times of about 30 ns when driving capacitance loads equivalent to the $C_{\rm iSS}$ of a power MOSFET. Input drive voltages for the DS0026 are compatible with Series 54/74 TTL devices, such as the MC7405 Hex Inverter (OC). Detailed information regarding transition times versus load capacitance and power dissipation can be found in the DS0026 data sheet.

Figure 6-26 identifies the DS0026 driving an MTM12N10. To illustrate the high peak gate currents that can be sourced by the DS0026, no resistance was included between driver output and MOSFET gate. It is important to remember that, with gate current transitions occurring in the low nanosecond range, any lead inductance between driver and gate will add (L/Rg) delay to the gate circuit. Keep the distance between driver output and gate terminal as short as possible when fast switching times are important.

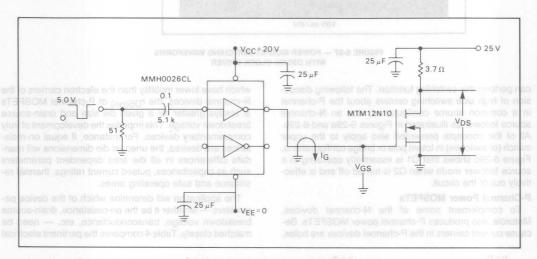


FIGURE 6-26 — DS0026 CLOCK DRIVER AS A DRIVER FOR POWER MOSFET

Input/output waveforms of the MTM12N10 are shown in Figure 6-27. Although not shown, the maximum drain current was 5.8 A. Figure 6-27 shows that 1.2 A gate current spike that occurs during the turn-on phase, and the 1.5 A negative current pulse occurring during the turn-off phase as C_{gd} is re-charged through the 3.7 ohm load resistor by the 25 V supply. The high voltage pulse that occurs as V_{DS} rises towards 25 V can be attributed to the kick-back of the 3.7 ohm load resistor's parasitic inductance of about 90 nH. This drain voltage spike can be limited by the insertion of an appropriately sized resistor in series with the DS0026 and the gate of the MTM12N10, to increase the $R_{g}C_{iSS}$ time constant, if the increase in turn-on time is acceptable.

Other examples of ICs that are used to drive the gate of a power MOSFET are the MC1555 timer, the TL494 pulse width modulation control circuit and the MC75451 peripheral driver. As power MOSFETs gain in popularity, more drivers specifically designed for MOSFETs will appear.

High Side Switching

In some situations, connecting the load to the negative bus is either convenient or necessary. In such instances the switching element must be referenced to the positive rail as shown in Figure 6-28. As with PNP and NPN bipolars, both P-channel and N-channel power MOSFETs



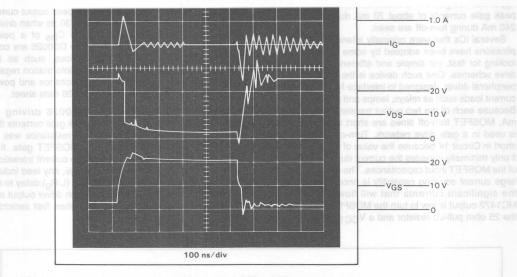


FIGURE 6-27 — POWER MOSFET SWITCHING WAVEFORMS
WITH DS0026 CLOCK DRIVER

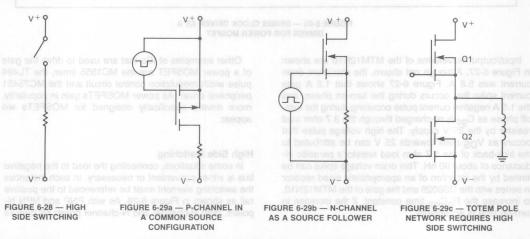
can perform this switching function. The following discussion of high side switching centers about the P-channel in a common source configuration, and an N-channel source follower as illustrated in Figures 6-29a and 6-29b. All of the concepts presented also apply to the upper switch (or switches) in totem pole or bridge configurations. Figure 6-29c shows that Q1 is essentially operating in a source follower mode when Q2 is turned off and is effectively out of the circuit.

P-Channel Power MOSFETs

To complement some of the N-channel devices, Motorola also produces P-channel power MOSFETs. Because current carriers in the P-channel devices are holes.

which have lower mobility than the electron carriers of the N-channel devices, the rDS(on) of P-channel MOSFETs is always greater for a given die size and drain-source breakdown voltage. This impedes the development of truly complementary devices. For instance, if equal on-resistances are desired, the unequal die dimensions will mandate differences in all die area dependent parameters such as capacitances, pulsed current ratings, thermal resistance and safe operating areas.

The application will determine which of the device parameters — whether it be the on-resistance, drain-source breakdown voltage, transconductance, etc. — need be matched closely. Table 4 compares the pertinent electrical



MOTOROLA TMOS POWER MOSFET DATA

parameters of the MTP8P10 with those of N-channel devices that may be considered as device complements. Besides showing the MTP8N10 is not always the best choice for a complement to the MTP8P10, the table also indicates the die area of a P-channel device must be approximately doubled to achieve the on-resistance of an N-channel device with the same V(BR)DSS rating.

P-channel power MOSFETs can simplify certain circuit configurations much in the same way that PNP bipolars can. The circuit simplicity obtained when using P-channel devices to switch a grounded load, for instance, may more than offset the price differential between the N- and P-channel devices.

In Figure 6-30 the source is connected to the positive rail and the drain is attached to the load. As such, the MOSFET is off when $V_{GS}=0$ V and begins to turn on as V_{GS} (a negative quantity) rises in absolute magnitude above the device threshold voltage. Current would then be free to flow from the source-to-drain and into the load. Still, a logic signal, which is normally referenced to ground, must be used to control the gate. A level shifter, followed by a discrete emitter-follower buffer can supply the proper logic levels while at the same time provide rapid MOSFET switching. The NPN-PNP buffer could be omitted if slower switching is desired.

N-Channel High Side Switching

Instead of using a P-channel as the high side switch, another choice is to use a less expensive N-channel power MOSFET with the load placed in the source circuit — a source follower.

Since there is no voltage gain in a source follower, the gate voltage must equal the output voltage plus the gate-source voltage at that particular load current. Also, for efficient power transfer, the source voltage, when switched on, should approach the positive rail (limited by rDS(on)). Thus, the gate voltage should be well above the positive rail, i.e., $V_G = V_{GS(on)} + V_{SD} = V_{GS(on)} + V_{DD}$. For hard gate turn-on, V_{GS} should be greater than

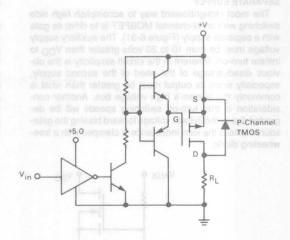


FIGURE 6-30 — LEVEL SHIFTER FOR P-CHANNEL MOSFET DRIVING A GROUNDED LOAD

10 V. Consequently, the gate voltage for a 12 V system could approach 22 V. This higher than V_{DD} supply gate voltage can be achieved by several techniques:

- A separate gate supply at least 10 V greater than VDD.
- 2. Pulse Transformer
- 3. Optoisolator
- 4. Bootstrapping
- 5. Voltage doubler clause and to viused on't incline
- 6. Inductive (flyback)

TABLE 4 — Complements of MTP8P10 and all beasembles calls are replaced away

		P-Channel		N-Channel		11-71
		MTP8P10	MTP8N10	MTP12N10	MTP20N10	Units
Drain-So	urce Voltage (Max)	100	100	100	100	Vdc
-	Continuous	8.0	8.0	12	20	Adc
ID	Pulsed	25	20	30	60	Adc
Max Power Dissipation		75	75	75	75	Watts
Threshold Voltage		2.0 to 4.5	2.0 to 4.5	2.0 to 4.5	2.0 to 4.5	Vdc
On-Resistance @ ID/2 (Max)		0.4	0.5	0.18	0.15	ohms
Transcon	iductance (Min)	2.0	1.5	3.0	6.0	mhos
Input Cap	pacitance (Max)	1200	400	1200	1400	pF
Output C	apacitance (Max)	600	350	500	1200	pF
Reverse	Transfer Capacitance (Max)	180	150	250	400	pF
Fall Time	e (Max)	150	60	100	200	ns
Rise Time	e (Max)	150	120	150	450	ns
Normalize	ed Die Area	1.0	0.45	0.66	1.0	_

SEPARATE SUPPLY

The most straightfoward way to accomplish high side switching with an N-channel MOSFET is to drive its gate with a separate supply (Figure 6-31). The auxiliary supply voltage must be from 10 to 20 volts greater than VDD to initiate turn-on. Inherent in the circuit simplicity is the obvious disadvantage of the need of the second supply, especially since its output must be greater than what is commonly the system's high voltage bus. Another consideration is that turn-off switching speeds will be degraded due to the flyback voltage forward biasing the gatesource unless the load inductance is clamped with a freewheeling diode.

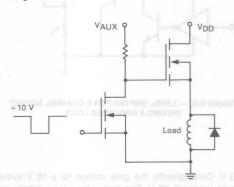


FIGURE 6-31 — HIGH SIDE SWITCHING USING AN AUXILIARY SUPPLY

PULSE TRANSFORMERS

Pulse transformers are a very popular and practical way of driving an N-channel MOSFET serving as the upper element in a bridge network or as any other high side switch. The beauty of the transformer drive is that the gate-drive signal is easily referenced to the source of the MOSFET, as Figure 6-32 illustrates. Circuits 1 through 4, (page 1-6-11 and 1-6-12) will perform just as well with the load common to the source and the drain tied to the positive rail. Other considerations for pulse transformer gate-drive design are also addressed in that section.

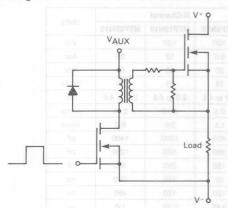


FIGURE 6-32 — PULSE TRANSFORMER DRIVER

OPTOISOLATORS SHOULD HIM OF 989TM and to an

A third way to drive a source follower is to reference the gate-drive signal to the source of the MOSFET with the aid of an optoisolator. Figure 6-33 is an example of such a drive network. As long as the $\rm V_{CC2}$ supply and the emitter of the optoisolator remain referenced to the source, the load can be common to either the source or the drain. The additional supply to power the output of the optoisolator must be able to raise the gate voltage above $\rm V_{DD}$. Either the supply must be isolated from the $\rm V_{DD}$ supply or must be generated from it with a bootstrapping technique.

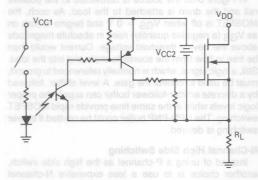


FIGURE 6-33 — DRIVING A SOURCE FOLLOWER WITH AN OPTOISOLATOR

BOOTSTRAPPING

The simplicity of bootstrapping makes that method the one of choice if its limitations are inconsequential in the specific application or they can somehow be circumvented. The bootstrapping circuit in Figure 6-34 generates the required gate-to-source signal. One of the main problems with this topology is that the load cannot remain in

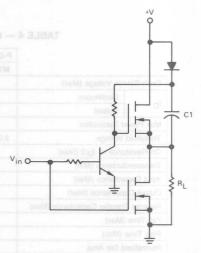


FIGURE 6-34 — BOOTSTRAPPING CIRCUIT TO DRIVE A GROUNDED LOAD WITH N-CHANNEL TMOS

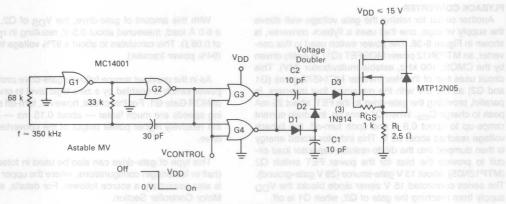


FIGURE 6-35 — N-CHANNEL SOURCE FOLLOWER WITH VOLTAGE DOUBLER DRIVE

the on state for an unlimited period of time because the finite charge stored in C1 is eventually bled off. A second problem is that this circuit cannot switch high voltages since C1 will be charged to the system supply voltage and then this potential will be impressed across the gate-to-source. Fortunately, in applications that require grounded loads, such as those in the automotive industry, the supply voltages are often compatible with this method of bootstrapping.

VOLTAGE DOUBLER

The gate voltage can be raised much higher than the source or supply voltage by using a voltage doubler, as shown in Figure 6-35. Voltage multipliers using diodes and capacitors require an oscillator input of which a simple and inexpensive method of obtaining this signal uses a CMOS astable multivibrator, designed with a quad two-input NOR gate MC14001. Gates G1 and G2 form the MV and the parallel connected gates G3 and G4 serve as a low output impedance buffer stage for driving the doubler

network. When these gates are powered with the same V_{DD} supply as the power MOSFET high side switch, the output of the doubler (input to the FET gate) will approach twice V_{DD}, due to the voltage doubling effect of diodes D1–D3, capacitors C1, C2 and the input capacitance $C_{\dot{i}SS}$ of the FET switch. Obviously, V_{DD} cannot exceed the maximum voltage of the CMOS (+18 V).

If greater switch output voltage is required with increasing VDD, the CMOS supply can be zenered and more diode-capacitor stages cascaded to raise the gate voltage.

With the component values shown, the astable MV will oscillate at about 350 kHz. This signal and, consequently, the switch can be gated ON and OFF by applying the indicated control voltage to the second input of gates G3 and G4. However, due to the low power output of the CMOS IC, switching speeds are quite slow — tens of milliseconds — limiting this circuit to slow switching applications. Turn-off time can be substantially improved by employing an input capacitance Ciss discharging clamp transistor.

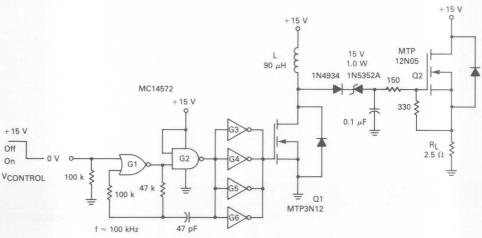


FIGURE 6-36 — N-CHANNEL SOURCE FOLLOWER WITH FLYBACK CONVERTER DRIVE

FLYBACK CONVERTER

Another circuit for raising the gate voltage well above the supply voltage, one that uses a flyback converter, is shown in Figure 6-36. The power switch used in this converter, an MTP3N12 power MOSFET (Q1), is easily driven by the CMOS, 100 kHz, astable multivibrator (MV). This circuit uses two of the Hex Inverter MC14572 gates (G1 and G2) as the MV with the remaining four inverters, in parallel, providing the gate-drive to the FET, about 25 mA peak to charge Ciss. When Q1 turns on, the drain current ramps-up to about 0.8 A and upon turn-off, the flyback voltage reaches about 60 V. This inductor stored energy is then dumped into the diode-resistor-capacitor load circuit to provide the bias for the power FET switch Q2 (MTP12N05), about 13 V gate-source (28 V gate-ground). The series connected 15 V zener diode blocks the VDD supply from reaching the gate of Q2, when Q1 is off.

With this amount of gate-drive, the V_{DS} of Q2, under a 6.0 A load, measured about 0.5 V, resulting in $r_{DS}(on)$ of 0.08 Ω . This calculates to about a 97% voltage transfer (94% power transfer).

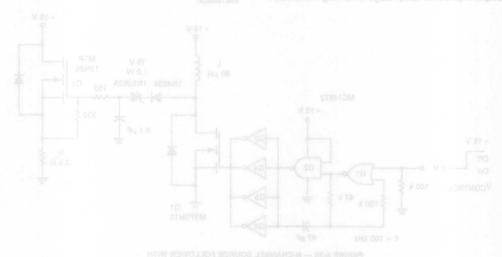
As in the previous source follower gate-drive circuit, the power switch is enabled by a zero logic level to one input of NOR Gate G1. For this circuit, however, turn-off switching speeds are much faster — about 0.15 ms — due to the relatively higher power output of the converter gate-drive.

This type of gate-drive can also be used in totem-pole (half or full-bridge) configurations, where the upper switch is also essentially a source follower. For details, see the Motor Controller Section.

1-6

ne on state for an unlimited period of time because the vite charge stored in C1 is eventually blad off. A second collection is that this circuit cannot switch high voltages are often expense supply voltages. The charged to the system supply voltage twitch this method to the charged to the system supply voltage are often compatible with this method ing Vpp, the CMOS (+18 V).

The gate voltage can be raised much higher than the source or supply voltage by using a voltage doubler, as shown in Figure 6-35. Voltage multipliers using diodes and capacitors require an oscillator input of which a simple and inexpensive method of obtaining this signal uses a 2MOS astable multivibrator, designed with a quad two-put NOR gate MC14001. Gates G1 and G2 form the MV and the parallel connected gates G3 and G4 serve as an own output improvement of the parallel connected gates G3 and G4 serve as a



Chapter 7: Paralleling Power MOSFETs

Paralleling Power MOSFETs in Switching Applications

In some applications, the most beneficial characteristic of the power MOSFET is its ability to be paralleled to increase current conduction and power switching capabilities. Current sharing among devices is important in all of the modes in which the MOSFET may conduct current. These modes are:

- 1 Fully "on" during static conditions.
- 2 Switching applications including transient (turnon and turn-off) and pulsed conditions.
- 3 Applications in which the drain-source diode will conduct current.
- 4 Linear applications. State = ADMR 109 = ADT

Since the considerations for each case are quite different, each must be investigated independently before the MOSFET can be regarded as a device that is easily paralleled. The following sections show that the MOSFET can be paralleled in each of the four modes provided certain simple recommendations are followed.

Static Current Sharing Design Considerations

Although increasing junction temperature raises the on-resistance and the conduction losses of the power MOSFET, definite benefits are attributable to the positive temperature coefficient of rDS(on). If a portion of the chip begins to hog current, the localized temperature will increase, causing a corresponding increase in the rDS(on) of that portion of the chip, and current will shift away to the cooler, less active, portions of the die. This trait accounts for the tendency of the device to share current over the entire surface of the die's active region. Because current crowding and hotspotting are eliminated under normal operating conditions, there is no need to derate power MOSFETs to guard against secondary breakdown.

The argument supporting current sharing within a device, due to the positive temperature coefficient of rDS(on), is easily extended to the case of paralleled devices. As within a single device with some imbalance in rDS(on) over the die's active area, an imbalance or mismatch of rDS(on) between devices will cause an initial current loading imbalance between devices. The resulting rise in junction temperature and on-resistance of the device with the lowest rDS(on) will decrease that device's drain current and will establish a more equal distribution of the total load current in all paralleled devices.

While this tendency is definitely observable, its influence on the degree of current sharing is often overestimated. In the power MOSFET, the current sharing mechanism is not triggered simply by high junction temperature, but by the difference in T_J between the low and high $r_{DS(on)}$ devices. Due to the generally small thermal coefficient of $r_{DS(on)}$, this difference in junction temperature sometimes must be substantial to attain a high degree of current sharing.

Since the ultimate concern is for optimum reliability, the emphasis should not be placed on obtaining large deltas in $T_{\rm J}$ to force a greater degree of current sharing. On the contrary, the effort should be focused on decreasing $T_{\rm J}$ of the hottest device. This is accomplished by close thermal coupling of the paralleled devices, provided that the total heat sinking capability is not compromised by doing so. This will tend to minimize the differences in both case and junction temperature. Before a worst case example of these concepts can be examined, some knowledge of the range of the variation of $r_{\rm DS(on)}$ within production devices must be obtained.

Unless devices are matched for identical on-resistances, there will be at least a slight mismatch in their individual drain currents. The worst case situation is obviously the paralleling of devices with the widest possible variation in $r_{DS(on)}$. Two wafer lots of the MTP8N18 were sampled to obtain some idea of the range of variation of $r_{DS(on)}$ within the same wafer lot and between wafer lots. In addition to information on $r_{DS(on)}$, Table 1 contains data on the parameters important to dynamic current sharing which will be addressed later. From this information, one will have to design for a worst case $r_{DS(on)}$ mismatch of 30%.

TABLE 1 — Variation of rps(on), gfs, and Vgs(th) in Two Wafer Lots of the MTP8N20*

	rDS(on)		g	FS	VGS	Sample		
	Min	Max	Min	Max	Min	Max	Size	
Wafer Lot I	0.231	0.297	3.704	4.878	2.300	4.080	100	
Wafer Lot II	0.239	0.305	3.571	4.878	3.685	3.910	50	

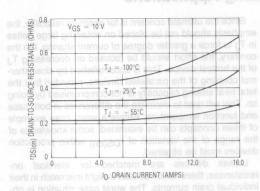
*Data was taken on first generation TMOS devices. The most recent devices may give different dispersions.

rDS(on) is influenced by the magnitude of the drain current and the junction temperature. Ip and TJ are, in turn, a function of the power dissipation, which is strongly dependent upon rDS(on). The quality of heat sinking and thermal coupling between devices also affects ID and TJ. These interdependent relationships make an analytical attempt to determine the degree of current sharing between several devices with a given rDS(on) mismatch rather complicated. An example of an iterative analytical process used to accomplish this end follows. The estimated ID mismatch is somewhat dependent on the initial assumptions.

Design requirements could include the following:

- 1. Maximum desired junction temperature is 125°C.
- Sufficient heat sinking will be supplied to maintain a 90°C case temperature when T_A = 35°C during maximum power dissipation.
- 3. Assume worst case rDS(on) mismatch for the MTP8N20 is 0.230 to 0.400 ohms @ ID = 4.0 A and TJ = 25°C.

From these conditions, the worst case variation in I_D , P_D and T_J needs to be determined. First, the thermal coefficient of $r_{DS(on)}$, C_T , must be determined from the on-resistance versus drain current curve (Figure 7-1).



eldleagg is FIGURE 7-1 — ON-RESISTANCE versus
DRAIN CURRENT — MTP8N18

$$C_{T} \begin{vmatrix} I_{D} = 8.0 \text{ A} = \frac{\Delta r_{DS(on)}}{\Delta T} = \frac{r_{DS(on)}}{\Delta T} \begin{vmatrix} T_{J} = 100^{\circ}\text{C} & r_{DS(on)} \\ 100^{\circ}\text{C} - 25^{\circ}\text{C} \end{vmatrix}$$

$$= \frac{0.47 - 0.32 \Omega}{75^{\circ}\text{C}} = 0.002 \Omega^{\circ}\text{C}$$

In addition to assuming that C_T is invariant with temperature and drain current, it is also supposed that thermal coupling between device heat sinks is negligible. From the maximum desired junction temperature ($T_J = 125^{\circ}C$), case temperature ($T_C = 90^{\circ}C$), and the junction to case thermal resistance ($R_{\theta JC} = 1.67^{\circ}C/W$) of the MTP8N20, the maximum power dissipation and case to ambient thermal resistance are easily calculated.

$$P_D = \frac{T_J - T_C}{R_{\theta JC}} = \frac{125-90^{\circ}C}{1.67^{\circ}C/W} = 20.96 \text{ W}$$

$$R_{\theta CA} \frac{T_C - T_A}{P_D} = \frac{90-35^{\circ}C}{20.96 \text{ W}} = 2.62^{\circ}C/W$$

Attention is then focused on the device with the lowest $r_{DS(on)}$ since it will be dissipating the most power. At a T_J of 125°C its $r_{DS(on)}$, drain current, and V_{DS} are:

To determine the operating conditions of a high resistance device operated in parallel with a low resistance device, an iterative technique must be employed. The approach is to estimate the junction temperature of the cooler device and from that, compute the rps(on) at that TJ, the current and power dissipated, and the new junction temperature. The computations are then repeated until the process converges on the correct solution.

The first iteration proceeds as follows:

$$\begin{split} & \text{TDS(on)} \\ & \text{TJ} = 100^{\circ}\text{C} \\ & = & \text{TDS(on)} \\ & \text{TJ} = 25^{\circ}\text{C} \\ & \text{T} \\ & \text{J} = 25^{\circ}\text{C} \\ & \text{T} \\ & \text{J} = 25^{\circ}\text{C} \\ & \text{J} \\ & \text{J} = 25^{\circ}\text{C} \\ & \text{J} \\ & \text{$$

After two more iterations, the algorithm converges. The results are tabulated for comparison with those of the low resistance device in Table 2. In addition to the case of negligible thermal coupling, the idealized situation of perfect thermal coupling of the cases is also included for direct comparison. The performance trade-off between the two examples is that little thermal coupling will achieve a greater degree of current sharing at the expense of higher junction temperature in the hottest device (119°C versus 125°C). Since TJ(max) most directly influences reliability, close thermal coupling of devices is encouraged. The manufacturer can best do this by paralleling chips on a common heat sink.

TABLE 2 — Static Current Sharing Performance of Mismatched MTP8N20

0 0		Perfect Thermal Case Coupling					
rDS(on) Min Device	rDS(on) Max Device	rDS(on) Min Device	rDS(on) Max Device				
0.230	0.400	0.230	0.400				
7.00	5.38	7.14	5.24				
21.0	16.1	21.3	15.78				
125	104	119	110				
0.430	0.558	0.419	0.570				
	Case C TDS(on) Min Device 0.230 7.00 21.0 125	TDS(on) Max Device 0.230 0.400 7.00 5.38 21.0 125 104	Case Coupling Case Coupling rDS(on) Min Device rDS(on) Min Device 0.230 0.400 0.230 7.00 5.38 7.14 21.0 16.1 21.3 125 104 119				

A point essential to the above calculations is that the steady state thermal resistance was employed to compute the junction temperatures. For pulsed conditions $R_{\theta JC}$ can vary significantly, and the transient thermal resistance obtained from the thermal response curves must be used to make this calculation. During switching transitions, there is insufficient time to establish differences in junction temperature and power MOSFETs may not current share in the same manner.

Dynamic Current Sharing Design Considerations

The term "dynamic" is broadened here to include not only current during turn-on and turn-off, but also peak current during narrow pulses and small duty cycles. Under these conditions, not enough RMS current is present to cause differential heating of the junctions which triggers the tendencies of the devices to share current. Since the argument supporting current sharing under static conditions is based on differences in junction temperature due to an imbalance of power dissipation and drain currents, that reasoning does not support the concept of current sharing during dynamic conditions. However, even without the benefit of the positive temperature coefficient, power MOSFETs can current share reasonably well with simple and efficient gate-drive circuitry.

The issues of greatest concern to those interested in dynamic current sharing of paralleled MOSFETs are listed and described in order below.

- Device parameters that influence dynamic current sharing.
- Variation of pertinent device parameters from lot to lot.
- 3. Required device parameter matching to achieve safe levels of current distribution.
- 4. The effects of switching speed on dynamic current sharing.
- 5. The requirements and effects of circuit layout.
- 6. The possibility of self-induced oscillations.

Device Parameters That Influence Dynamic Current Sharing

The device parameters that influence the degree of dynamic current sharing are the transconductance (gES), gate-source threshold voltage [VGS(th)], input capacitance, and the on-resistance rDS(on). However, the device characteristic that most accurately predicts how well paralleled MOSFETs will current share during turn-on or turn-off is the transconductance curve, i.e., the relationship between the drain current and the gate-source voltage. To obtain optimum current distribution during turnon and turn-off, the ideal situation is to have all gatesource voltages rising (or falling) simultaneously on devices with identical transconductance curves. This combination would ensure that as the devices switch through the active region, none would be overstressed by a current imbalance. Figures 7-2a, 7-2b and 7-2c show the nearly perfect degree of current sharing obtainable solely by matching the gfs curves. The current probe used induced a 20 ns delay in the current waveform in the oscillograms

Since plotting the entire g_{fS} curve of each device is very time consuming, matching $V_{GS}(th)$ or g_{FS} at some drain current has been suggested as a simpler criterion for matching paralleled MOSFETs. While much of the literature suggests the importance of matching $V_{GS}(th)$, which is normally defined as the minimum gate voltage at which a small drain current (usually specified as 1.0 mA) begins to flow, this does not accurately indicate the shape of the I_D versus V_{GS} curve at higher currents.

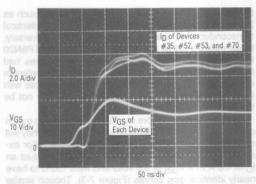


FIGURE 7-2a — PARALLELED TURN-ON

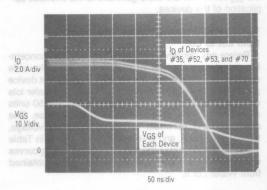


FIGURE 7-2b — PARALLELED TURN-OFF

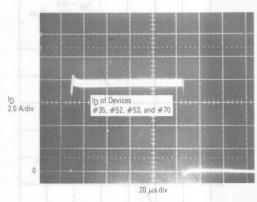


FIGURE 7-2c — COMPOSITE ID WAVEFORM FOR TURN-ON AND TURN-OFF

FIGURE 7-2 — INDIVIDUAL I_D WAVEFORMS OF FOUR PARALLELED MTP8N18 WITH MATCHED TRANSCONDUCTANCE CURVES — RESISTIVE LOAD (DRAIN CURRENT WAVEFORMS ARE DELAYED 20 ns) transconductance curves above 100 mA. Conversely, those devices out of a group of one hundred MTP8N20 found to have the widest variation of grs curves had thresholds that varied by only 4%. Therefore, for optimum current sharing, the ideal solution is to use devices with identical curves, and comparing thresholds may not be the best way to achieve this.

Another simple, yet more consistent, method is to match devices by comparing the maximum drain current they will conduct at a gate voltage higher than VGS(th). For example, all four devices shown in Figure 7-2 conduct an ID of 4.0 A at a VGS of 6.0 volts and were found to have nearly identical gFS curves (Figure 7-3). Though similar to matching thresholds, this method matches points on the gfs curve that are more germane to the intended application of the devices.

Variation of Pertinent Device Parameters from Lot to Lot

Before any definitive statement may be made concerning the degree or type of matching required for safe dynamic current sharing, the variation of pertinent device parameters from lot to lot must be known. Two wafer lots of the MTP8N20, with sample sizes of 100 and 50 units respectively, were characterized for this pupose. The maximum and minimum values of threshold voltage, transconductance, and on-resistance are shown in Table 1. Figure 7-4 illustrates the widest variation in gFS curves within Wafer Lot I and is similar to the results obtained from Wafer Lot II.

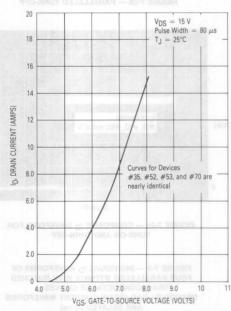


FIGURE 7-3 — TRANSCONDUCTANCE CURVES OF MATCHED MTP8N20

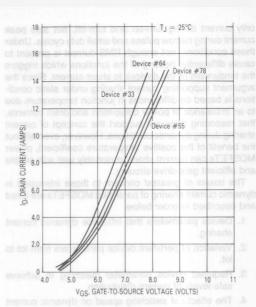


FIGURE 7-4 — WIDEST VARIATION IN TRANSCONDUCTANCE
CURVES FOUND IN WAFER LOT I

Obviously, the possibility of larger than expected variations in these pertinent parameters diminishes as the number of sampled wafer lots increases. To get an adequate sampling of available devices, the user could characterize devices with different date codes or obtain units from several distributors.

Required Matching for Safe Levels of Current of Safe Levels of Current

After characterization and determining the degree of variation possible, the effects of matching or mismatching the critical device characteristics can be observed. The circuit used for this study is shown in Figure 7-5. Some of the possible modifications of the circuit include adding resistors in series with the gate to slow the turn-on and turn-off, and a second MOSFET may be included to clamp the gate bus to ground to observe the effects of very rapid turn-off

In this discussion of resistive switching, Figure 7-2 will serve as a standard for comparisons since matching transconductance curves has achieved such good performance. Extreme care was taken to provide as pure a resistive load as possible. The 1.6 ohm load was constructed from 39, 62-ohm carbon composition resistors connected in parallel between two copper plates. Though the drain wiring and load inductances were very small, during rapid turn-on, the L/R time constant of the circuit may be the factor that limits the current rise times and not the switching speed of the MOSFETs.

One of the worst case situations is to parallel devices with greatly mismatched gFS curves. Representing the

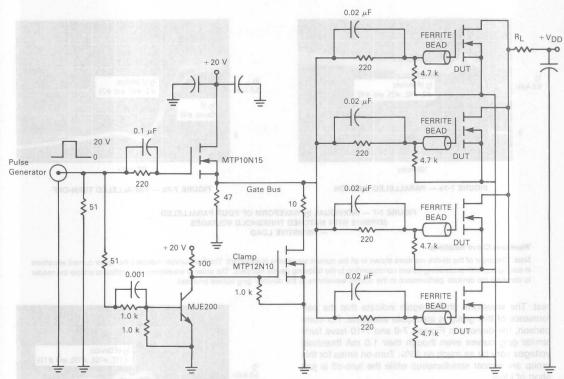


FIGURE 7-5 — DYNAMIC CURRENT SHARING TEST CIRCUIT

widest variation in the gFS curves in Wafer Lot I, Figure 7-4 shows the curve of a device that will begin to turn on with a rising VGS slightly sooner than the other three devices. It may be expected that device #33 will turn on first and possibly fail due to current overload. However, since the variation in the ID versus VGS curves of these mismatched devices is small, the failure will not occur. As shown in Figure 7-6, parallel operation of these mis-

matched devices in the given circuit poses no significant reliability hazard.

Matching the 1.0 mA thresholds does not guarantee the nearly perfect results of matching the gFS curves, as shown in Figure 7-7. Although their thresholds were matched to within 2%, these devices exhibited a fairly wide variation in gFS curves (Figure 7-8) which resulted in device #45 beginning its turn-off slightly sooner than the

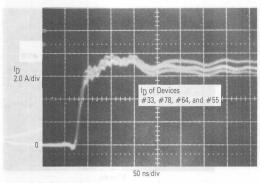


FIGURE 7-6a — PARALLELED TURN-ON

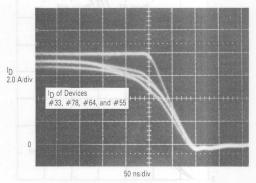


FIGURE 7-6b — PARALLELED TURN-OFF

FIGURE 7-6 — INDIVIDUAL ID WAVEFORMS OF FOUR PARALLELED MTP8N18 WITH MISMATCHED TRANSCONDUCTANCE CURVES — RESISTIVE LOAD



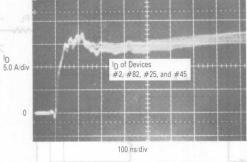


FIGURE 7-7a — PARALLELED TURN-ON

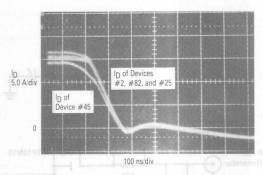


FIGURE 7-7b — PARALLELED TURN-OFF

FIGURE 7-7 — INDIVIDUAL I_D WAVEFORM OF FOUR PARALLELED MTP8N18 WITH MATCHED THRESHOLD VOLTAGES

— RESISTIVE LOAD

Waveform/Curve Relations

Note: The order of the device numbers shown in all the current waveforms is important. The first number indicates the upper current waveform in each group with succeeding curves corresponding to the following device numbers. The order of waveforms is identified to enable the reader to correlate the devices' performance in the current waveforms to the devices' gFS curves provided.

rest. The waveform photos again indicate that the performance of this group is also quite adequate. For comparison, the devices in Figures 7-9 and 7-10 have fairly similar gFS curves even though their 1.0 mA threshold voltages vary by as much as 33%. Turn-on times for this group are almost simultaneous while the turn-off is just short of ideal.

Because the MTP8N20 of the two wafer lots were so close in characteristics, the worst conceivable mismatch that might occur could not be found. In order to study the effects of such a wide disparity between parameters, an MTP12N10 was paired with three closely matched

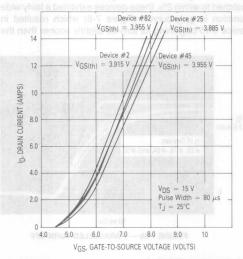


FIGURE 7-8 — TRANSCONDUCTANCE CURVES OF MTP8N20 WITH MATCHED THRESHOLD VOLTAGES

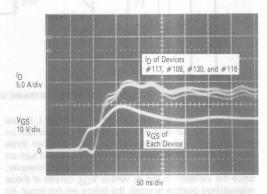


FIGURE 7-9a — PARALLELED TURN-ON

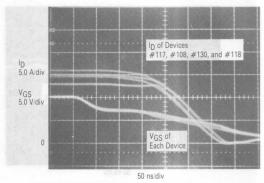


FIGURE 7-9b — PARALLELED TURN-OFF

FIGURE 7-9 — INDIVIDUAL ID WAVEFORMS OF FOUR MTP8N20 WITH MATCHED TRANSCONDUCTANCE CURVES AND MISMATCHED THRESHOLD VOLTAGES

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TABLE 3 — Parameter Comparison of One MTP12N10 and Three MTP8N20s

Device Number	Device Type	rDS(on) ID = 4.0 A (Ohm)	VGS(th) ID = 1.0 mA (Volts)	9fs ID = 4.0 A VGS = 15 V (Volts)	C _{rss} (pF)	C _{iss} (pF)	C _{oss} (pF)
#122	MTP12N10	0.145	3.600	4.300	90	685	395
#52	MTP8N20	0.238	3.955	4.762	45	700	220
#53	MTP8N20	0.256	3.900	4.444	45	700	245
#70	MTP8N20	0.255	3.930	4.444	45	700	235

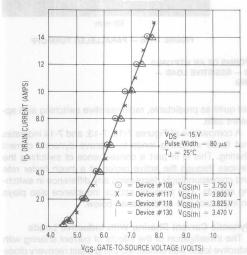


FIGURE 7-10 — TRANSCONDUCTANCE CURVES OF MTP8N20 WITH THRESHOLD VOLTAGE VGS(th) MISMATCH

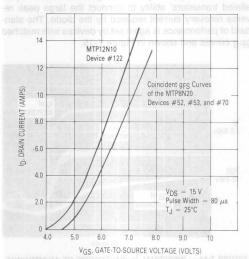


FIGURE 7-11 — TRANSCONDUCTANCE CURVES OF AN MTP12N10 AND THREE MTP8N20

MTP8N20. The MTP12N10 is a 12 A, 100 V device with the same die dimensions as the MTP8N20. Table 3 and Figure 7-11 compare the different device characteristics. The result of paralleling these four devices is shown in Figure 7-12.

The MTP12N10 is the last device to begin turn-on even though its transconductance curve rises earlier than those of the MTP8N20. This is due to the larger C_{rss} (reverse transfer or gate-drain capacitance) which is effectively multiplied in value by the device gain due to the Miller effect. Although not completely simultaneous, the turn-off is smooth. By the time the MTP8N20 have completely switched off, the MTP12N10 has moved well into the active or constant current region. At that time, the total

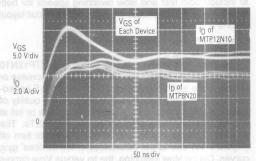


FIGURE 7-12a — PARALLELED TURN-ON

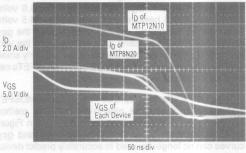


FIGURE 7-12b — PARALLELED TURN-OFF

FIGURE 7-12 — INDIVIDUAL ID WAVEFORMS OF AN MTP12N10
PARALLELED WITH THREE MTP8N20 — RESISTIVE LOAD



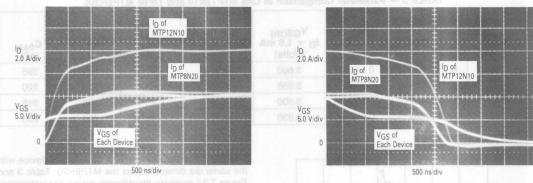


FIGURE 7-13a — PARALLELED TURN-ON

FIGURE 7-13b — PARALLELED TURN-OFF

FIGURE 7-13 — INDIVIDUAL ID WAVEFORMS OF AN MTP12N10
PARALLELED WITH THREE MTP8N20 — RESISTIVE LOAD —
SLOW SWITCHING

load current has been substantially reduced and the slightly unsynchronized turn-off poses no threat to the MTP12N10 at these switching speeds.

It is apparent that for this specific application, i.e., resistive switching at moderate switching speed, device matching improves paralleled performance but is not necessary for safe operation. This recommendation will be extended to include both fast and slow switching speeds for both resistive and inductive loads provided certain circuit layout criteria are met.

Effects of Switching Speed on Dynamic Current Sharing

The gate-drive circuit used to switch the MTP12N10 and the three MTP8N20 was altered to either increase or decrease the switching speed. The four 0.02 μF speedup capacitors were removed to determine the quality of current sharing as the gate-source voltages rise or fall at speeds that are fairly slow for power MOSFETs. The MTP12N10 is the first to turn on and the last to turn off (Figure 7-13) due to the differences in the devices' gFS curves. During slow switching, the ID versus VGS curves can be used to accurately predict the ID curves. For instance, the MTP12N10 begins to turn on when the composite gate-source voltage waveform reaches 4.0 volts, but the MTP8N20 hesitate until VGS reaches 4.5 volts. Since the ID waveforms are easily related via the gFS curves to the rising or falling gate voltages and the variation in the ges curves over a product line are fairly small, slow switching of unmatched TMOS power MOSFETs can be a safe undertaking.

To judge the effects of rapid turn-off, a second MOSFET was added to clamp the gate-to-ground. This method achieves the 20 ns current fall times depicted in Figure 7-14. During such rapid switching, the VGS and gFS curves can no longer be used to accurately predict device performance due to package and lead parasitics such as the package source inductance. Once again however, these mismatched devices performed well as they were switched very rapidly through the active region. Although

not quite as predictable, rapid resistive switching also appears safe.

A comparison of Figures 7-12, 7-13, and 7-14 indicates that faster switching tends to improve dynamic current sharing. This is in part a consequence of switching the devices through the active region at a much faster rate and correspondingly decreasing any difference in switching speeds. The parasitic source inductance also plays an important role as discussed below.

Dynamic Current Sharing With Inductive Loads

The investigation of the effects of current sharing with inductive loads was conducted using a fast recovery diode (40 A, 400 V) placed in parallel with a 135 μ H inductor as a load. The diode was included not so much to protect the MOSFET against flyback voltages, but to test the paralleled transistors' ability to conduct the large peak reverse recovery current required by the diode. The standard of performance is again set by devices with matched gFS curves and shown in Figure 7-15.

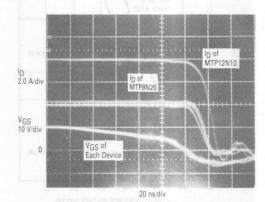


FIGURE 7-14 — INDIVIDUAL I_D WAVEFORMS OF AN MTP12N10
PARALLELED WITH THREE MTP8N20 — RESISTIVE LOAD — RAPID
TURN-OFF

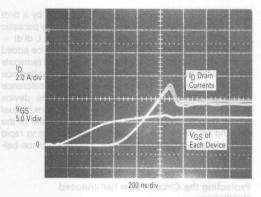


FIGURE 7-15a — PARALLELED TURN-ON

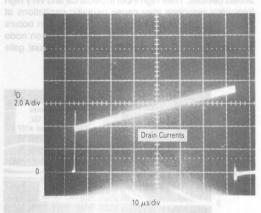


FIGURE 7-15b — COMPOSITE TURN-ON AND TURN-OFF
WAVEFORM

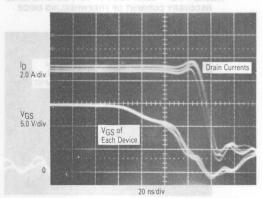


FIGURE 7-15c — PARALLELED TURN-OFF

FIGURE 7-15 — INDIVIDUAL ID WAVEFORMS OF MATCHED MTP8N20 SWITCHING AN INDUCTIVE LOAD — DEVICES #35, #52, #53, and #70

To obtain a larger sample size for the worst case inductive testing, 250 additional MTP8N20 of unknown wafer origin were characterized for their widest variation in gFS curves. The mismatched transconductance curves are shown in Figure 7-16. Figure 7-17 depicts both rapid and slow inductive turn-on and turn-off. This group of figures represents the greatest current imbalance seen in any set of mismatched MTP8N20 under any load conditions. While there are obvious current mismatches, they require only a small amount of derating to guardband against possible harmful situations. The keys to success are: 1) that pertinent device characteristics do not vary widely; and, 2) strict attention is given to the symmetry of the circuit layout.

Circuit Layout — A Critical Concern

Even with identically matched devices, dynamic current sharing between MOSFETs will be poor if an asymmetrical circuit layout is used. Obviously, if the gate-drives are different, unequal rates of gate-source voltage rise and fall can cause unsynchronized switching and even device failure in extreme cases. As the switching speeds of these devices are increased, the designer's perception as to what may constitute an important parasitic circuit element must change. When approaching the maximum switching speeds of power MOSFETs, even small variations in lead length may influence their paralleled switching performance. Unequal source wiring inductances are especially deleterious.

Figures 7-18a and 7-18b illustrate the effects of an imbalance in source wiring inductance. The devices and circuit layout are both closely matched except that an additional source lead inductance of 50 nH (1.5 inches of #22 wire formed into a 1-1/2 turn loop) was added to one device. As can be seen in the photographs, any source lead or wiring inductance will degenerate both the turn-on and turn-off speeds. Fortunately, perhaps the most important consideration for successful operation of paralleled MOSFETs is completely within easy control of the circuit designer. The circuit should be free from parasitics and as symmetrical as possible, especially for higher switching speeds.

Another obvious consideration is that the output impedance of the gate-drive circuits must be matched. Mismatched gate-drives will cause unsynchronized charging or discharging of the input capacitances, forcing the devices to begin switching at different times and rates.

The Benefit of Parasitic Source Inductance

Provided that the circuit layout is symmetrical, especially with respect to the source wiring inductance, faster switching can actually benefit the degree of current sharing between paralleled MOSFETs. During switching transitions of less than 100 ns, the source package inductance (approximately 7.0 nH) plays an important part in determining the shape of the rising and falling drain current waveform. The following example assumes the wiring inductance is negligible and relates only the effect of the source package inductance. The intent of this illustration is to show the significance of the package inductance and by extension relate the importance of the usually much larger wiring inductance.



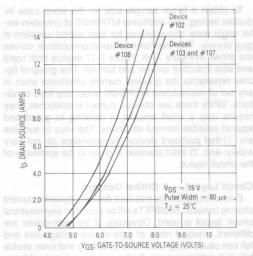


FIGURE 7-16 — WIDEST VARIATION IN TRANSCONDUCTANCE CURVES OF 250 ADDITIONAL MTP8N20

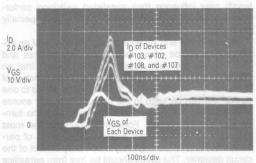


FIGURE 7-17a — RAPID TURN-ON SUPPLYING REVERSE RECOVERY CURRENT OF FREEWHEELING DIODE

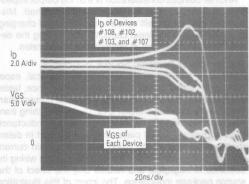


FIGURE 7-17c — RAPID INDUCTIVE TURN-OFF

Assuming a very rapid turn-off accompanied by a di/dt of 8.0 A/50 ns, the voltage appearing across the parasitic lead inductance is approximately 1.1 volts (v = L di/dt = 7.0 nH x 8.0 A/50 ns). This inductive drop must be added to the voltage appearing across the gate-source terminals to reveal the potential impressed at the chip. A difference in gate voltage of this size makes a significant difference in the magnitude of the drain current as the device switches through the active region. Therefore, equal source inductances will tend to equalize the rate of the rise and fall of the individual drain currents during rapid switching of paralleled MOSFETs. In effect, source ballasting is achieved during rapid switching.

Protecting the Circuit From Self-Induced Oscillations

Two of the most highly esteemed characteristics of the power MOSFET can combine to cause a problem in paralleled devices. Their high input impedance and very high frequency response may cause parasitic oscillations at frequencies greater than 100 MHz. This problem occurs when all gates are driven directly from a common node as in the circuit in Figure 7-19. Without individual gate

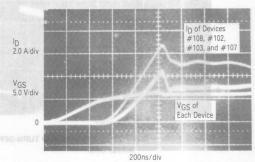


FIGURE 7-17b — SLOW TURN-ON SUPPLYING REVERSE RECOVERY CURRENT OF FREEWHEELING DIODE

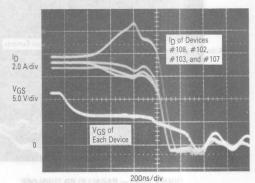
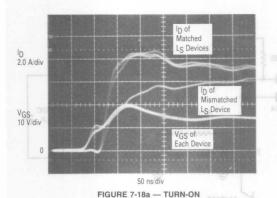


FIGURE 7-17d — SLOW INDUCTIVE TURN-OFF

FIGURE 7-17 — INDIVIDUAL I_D WAVEFORMS OF MISMATCHED MTP8N20 SWITCHING AN INDUCTIVE LOAD





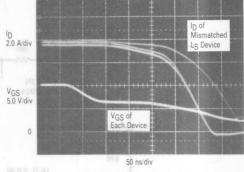


FIGURE 7-18b — TURN-OFF

FIGURE 7-18 — EFFECTS OF IMBALANCED SOURCE INDUCTANCES ON PARALLELED PERFORMANCE

resistances a high-Q network (Figure 7-20) is established that may cause the device to oscillate when operating in or switching through the active region. The device transconductance, gate-to-drain parasitic capacitance, and drain and gate parasitic inductances have all been shown to influence the stability of the circuit.

Although potentially serious, this problem is easily averted. By decoupling the gates of each device with lossy elements such as resistors or ferrite beads, the Q of the circuit can be sufficiently degraded to the point that oscillations are no longer possible (note dotted resistors shown in Figure 7-19). For the maximum switching speeds, the value of gate decoupling resistors should be kept as low as safely allowable. A value in the range of 10 to 20 ohms is generally sufficient.

A Practical Application — An Inductive

To show the feasibility of paralleling power MOSFETs in an application that imposes stresses typical of an inductive load, four MTP8N20's were paralleled in the circuit

shown in Figure 7-21. At a 50% duty cycle and a VDD of 44 V, the MOSFETs delivered about 450 W to the RC load. To minimize the power that the drain-source zener clamp must dissipate, MOSFET turn-off speed was limited by the placement of an 82 Ω resistor in series with each gate.

Again, the performance of interest is that of mismatched devices. In this case, fifty units from a newly designed mask set were tested for the widest variation in onresistance (0.255 Ω to 0.230 Ω). The three highest rDS(on) devices were grouped with the lowest rDS(on) unit. Since a low rDS(on) usually indicates a high gFS, the transconductance curves of these devices were also mismatched.

The degree of current sharing among these four units was well within safe operating limits. As expected, the lowest rps(on) device carried the greatest on-state current. For clarity, only the on-state currents of the lowest and highest rps(on) units are shown in Figure 7-22. The currents of the other two devices were nearly identical to device #8. As Figure 7-23 shows, the drain current of the lowest rps(on) device, #11, peaked slightly due to its different qps curve.

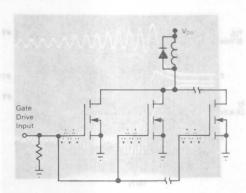


FIGURE 7-19 — METHOD FOR DRIVING PARALLELED MOSFETS USING GATE DECOUPLING RESISTORS

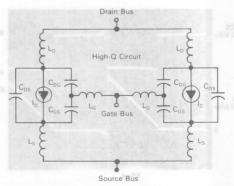
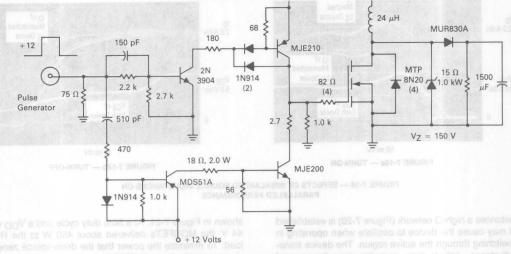


FIGURE 7-20 — PARASITIC HIGH-Q EQUIVALENT CIRCUIT
OF PARALLELED MOSFETs WITHOUT GATE DECOUPLING
RESISTORS



belimit asw been floamed T FIGURE 7-21 - CURRENT SHARING TEST CIRCUIT WITH AN INDUCTIVE LOAD 101-9180 Application

Each device was mounted on a separate heat sink, and the case temperatures were monitored to detect any thermal imbalances. Because of its low rDS(on), theory predicts that the case temperature of device #11 will be higher than the others. However, since the operating frequency was fairly high (40 kHz), the difference in switching losses may have also influenced the temperature comparison. Whether it was due to a variation in rDS(on) or gfs curves, the temperature difference was very small (54.3°C for device #11 and 52.3°C for device #8) and did not significantly affect device performance, i.e., the degree of current sharing.

The following is a summary of recommendations and findings concerning static and dynamic current, sharing in paralleled power MOSFETs.

- For static current sharing, the current mismatches are determined by the rDS(on) mismatch. A small degree of guardbanding or rDS(on) matching will ensure safe operation.
- 2. For dynamic current sharing, the turn-on and turn-off waveforms are largely determined by the transconductance curves. If matching is deemed necessary in a particular application, selecting devices by comparing gFS curves is the most accurate approach. A simple, yet adequate, substitute is to match a single point on the gFS curves at which the devices conduct significant drain currents.
- 3. Increasing the switching speeds in symmetrical circuits tends to equalize the rate of current rise and

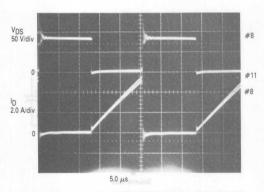


FIGURE 7-22 — ID WAVEFORMS OF LOW AND HIGH rDS(on) DEVICES — INDUCTIVE LOAD

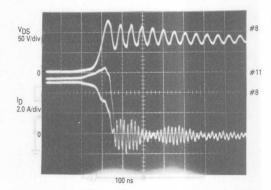


FIGURE 7-23 — ID TURN-OFF WAVEFORMS OF LOW AND HIGH rDS(on) DEVICES — INDUCTIVE LOAD

- 9 VDD
- 4. The circuit layout should be as symmetrical as possible with respect to the gate-drive and the source, gate, and drain parasitic inductances.

of the parasitic source inductance.

fall in paralleled devices due to the ballasting effect

5. In all applications, the gates should be decoupled with small resistors or ferrite beads to eliminate parasitic oscillations.

Drain-to-Source Diodes

The previous text on paralleling power MOSFETs has shown the effects of parameter matching (or unmatching) on the degree of current sharing when the FETs are operating in either switching or linear applications. However, it has not described the effects on the paralleled drainsource diodes when these diodes are used as clamp or free-wheeling diodes in practical applications. These diodes can be used in multi-MOSFET switching applications (see Chapter 12 on characterizing D-S Diodes) when the diode switching speeds are commensurate with the application. In a half bridge, as an example, the diode of one FET protects the drain-source of the second FET and, conversely, the diode of the second FET protects the first FET. Whatever the circuit configuration, the equivalent circuit reduces to that of a clamped inductive load, whereby the drain-source diode is effectively across the load inductance (Figure 7-24).

When power MOSFETs are paralleled in switching applications, the question arises as to how well their intrinsic diodes share the clamped current. To determine this, three MOSFETs were paralleled in the circuit shown in Figure 7-25. The test circuit (a complete schematic is shown in Figures 12-19 of Chapter 12) was duty cycle controlled to produce a continuous load current; thus, the commutated diode current indicated both the reverse recovery time trr and turn-on time ton. The individual and total diode currents, as well as the driver drain current, were monitored.

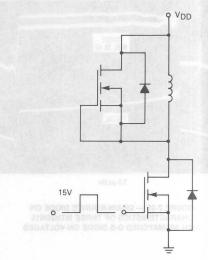


FIGURE 7-24 — INTRINSIC D-S DIODE **CLAMPING AN INDUCTIVE LOAD**

To obtain some indication of a worst case condition, a modest sample (20 pieces) of MTM20N15 were characterized for parameters that affect their paralleled performance. The forward on-voltage of the diodes at 10 A ranged from 1.05 to 1.20 volts, and trr varied from 0.25 to 0.32 µs. Devices with the widest mismatch in parameters were grouped and tested in the circuit shown in Figure

Testing indicated that current mismatches were small, even in devices with the greatest difference in D-S diode on-voltage. Figure 7-26 shows the current waveforms of

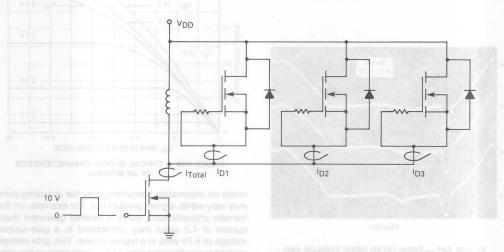


FIGURE 7-25 — TEST CIRCUIT TO OBSERVE **CURRENT SHARING OF PARALLELED D-S DIODES**

FIGURE 7-26 — DRAIN-SOURCE DIODE ON CHARACTERISTICS OF THREE MTM20N15 WITH MISMATCHED D-S DIODE ON-VOLTAGES

three paralleled diodes and the expected mild mismatch. Also shown is a representation of I_{TOTAL}, which is somewhat distorted due to the saturation of the current transformer that was used.

Current waveforms of devices with the widest variation in $t_{\rm rr}$ are shown in Figure 7-27. Again, even though the diodes are mismatched, the synchronized turn-on and turn-off transitions illustrate the high degree of current sharing that occurs as the load current is commutated between the freewheeling diodes and the drive transistor.

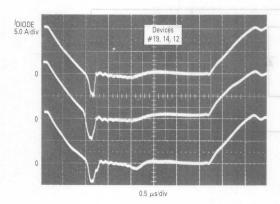


FIGURE 7-27 — PARALLELED DIODE TURN-ON AND TURN-OFF OF MTM15N20 WITH MISMATCHED tr

Paralleling Power MOSFETs in Linear Applications

Often lauded for their efficient high frequency switching capability, power MOSFETs are ideally suited for a myriad of switching applications. However, some of their other less renowned characteristics also make them attractive to designers of linear systems. Often the reason cited for their use is the inherent ruggedness of the MOSFET as evidenced by the lack of a second breakdown derating. Another characteristic that is appealing is the high input impedance that results in simplified gate-drive circuitry. Also, the transconductance is nearly linear over a wide operating range and its variation among devices in a given product line is small.

Although these benefits are significant, a method of predicting and stabilizing the operating point is necessary before linear operation can be successful. In the following sections a product line is characterized for the parameters pertinent to Q-point variation in the linear mode. The effects of a source resistor on the operating point and the small-signal transconductance are then discussed for single device operation. Finally, these concepts are extended to include the case of paralleled devices with special attention paid to the degree of current sharing.

Device Characteristics Important for Operating Point Stability

When developing a system that operates in the linear mode, it is often either desirable or imperative to accurately fix the system quiescent operating point (Q-point). The most pertinent graphs describing the operation of TMOS Power MOSFETs in the linear mode are those showing the output characteristics (Figure 7-28) and the transfer characteristics, or transconductance curves (Figure 7-29). However, since these are typical curves, they

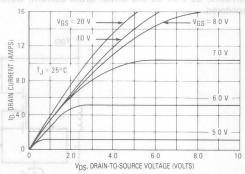


FIGURE 7-28 — TYPICAL OUTPUT CHARACTERISTICS
OF AN MTP8N20

relate no information concerning how the operating point may vary within a given product line. For example, on the transfer characteristics curve a desired quiescent drain current of 4.0 amps may correspond to a gate-source voltage of 5.75 volts in a typical device. This gate voltage applied to an atypical device of the same product line may result in a drain current that ranges from 2.5 to 4.5 A.

Matching device parameters is often proposed as a means of ensuring some minimum variation in the Q-point. This approach, especially using the threshold voltage, is not the optimum solution. The gate-threshold voltage is defined as the minimum gate-source voltage at which the MOSFET conducts some small drain current, usually specified as 1.0 mA. On the scale that the transfer characteristics are usually drawn, this 1.0 mA drain current is very small and the exact threshold voltage is indiscernable. It is not difficult to find two devices with nearly identical transfer characteristics that have thresholds that vary by nearly 2.0 volts. Conversely, devices with matched thresholds can have significantly different transfer curves. usually due to a gFS mismatch. Attempting to match devices by comparing transconductance or on-resistance also gives little assurance that the transfer curves will be

If component screening is desired, the most direct method is to actually compare each I_D versus V_{GS} curve. Since this is often impractical, one of two other courses may be taken. The criteria for matching could be the drain current at the gate voltage that is typical of the desired quiescent current. Referring back to the previous example, one may select devices on the basis of I_D at a V_{GS} of 5.75 volts. The other solution, which completely eliminates any device screening, involves the use of source resistors and is detailed in the next section.

similar

Junction temperature is another important variable that influences the quiescent operation point. Figure 6-25 shows that the gFS curve of the MOSFET can be divided into two regions. Below a VGS of 6.1 volts, an increase in TJ increases Ip. This is due to the negative temperature coefficient of VGS(th) dominating the positive coefficient of rpS(on). As TJ rises, the threshold voltage falls and Ip increases despite an increase in rpS(on).

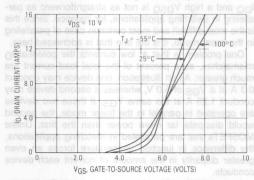


FIGURE 7-29 — TYPICAL TRANSCONDUCTANCE CURVES OF AN MTP8N20

At gate-to-source voltages greater than 6.1 volts, the temperature dependence of $r_{DS(on)}$ governs the change in I_D . Even though $V_{GS(th)}$ is falling as T_J rises, the effect of the increase in $r_{DS(on)}$ begins to dominate, causing I_D to decrease. The temperature dependence of I_D necessitates the consideration of the effect that T_J has on the Q-point, especially at low drain currents where the percentage change in I_D is high.

Using a Source Resistor to Stabilize the Q-Point

Operating point stability can be improved without preselecting devices by using a source resistor. The placement of such a resistor provides degenerative feedback to the gate by decreasing VGS by an amount proportional to the drain current (Figure 7-30). Equations for the small-signal transconductance and voltage gain with and without the source resistor are derived in Table 4.

Determining the effect of a source resistor on the operating point of a power MOSFET is a simple geometric exercise. The first step is to obtain, usually with a curve tracer, the transconductance curve of the device in question. With no source resistance (RS = 0 Ω), a vertical

FIGURE 7-30 — SOURCE RESISTOR SUPPLIES NEGATIVE
FEEDBACK TO THE GATE

TABLE 4 — Equations for the Small-Signal
Transconductance and Voltage Gain With and
Without a Source Resistor

	With No Source Resistor	With A Source Resistor
Small-Signal Transconductance	$9FS = \frac{\Delta ID}{\Delta VGS}$	$\begin{aligned} &\text{d.e.} & \frac{7 \Lambda QQ}{7 \Gamma P} = \frac{1 + RS}{7 \Gamma D} & \frac{1 + RS}{2} $
Small-Signal Voltage Gain	$A_{V} = \frac{7ID \cdot BF}{7AD \cdot BF}$ $= \frac{7ID \cdot BF}{7AD \cdot BF}$ $\therefore A^{V} = -BFS \cdot BF$	$A'_{V} = -g_{F}SR_{L}$ $= \frac{-R_{L}g_{F}S}{1+g_{F}S}R_{S}$ $\therefore A'_{V} = \frac{-R_{L}}{1/g_{F}S+R_{S}}$
Circuits	VDD RL VGG = VGS	VDD RL VGG + RS

Primed numbers indicate the effective values for the MOSFET and source resistor combination.

line through the gFS curve will indicate the drain current at a given V $_{GS}$. For instance, the device depicted in Figure 7-31 will conduct 0.375 A at a V $_{GS}$ of 4.7 volts.

through a given V_{GG} with a slope of $-1/R_S$. Figure 7-31 shows that for an R_S of 2.0 Ω and a V_{GG} of 5.45 V, the Q-point is fixed so that I_D is still 0.375 A. The effects of varying the gate-to-ground voltage can be determined by constructing parallel lines through the gate voltages of interest. Changing the slope of the line graphically models changes in R_S .

To use the technique of employing a source resistor to improve Q-point stability, the worst case variation in the gFS curves needs to be determined for the product line in question. For this study, 350 MTP8N18's from the same wafer lot were checked for the greatest difference in transconductance curves. The results are shown in Figure 7-32. With these curves, actually sizing RS and determining the gate voltage for a desired operating point (with a defined allowable variation) is a very simple geometric exercise.

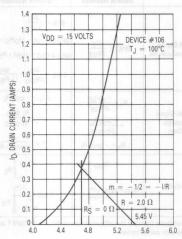
Assume that the desired conditions are as follows:

ID quiescent = 0.4 A

Allowable IDQ variation from 0.4 A is 0.05 A

 $T_J = 100^{\circ}C$

An RS load line drawn through points A and B and extending down to the gate voltage axis determines both the required magnitude of RS and the quiescent gate voltage. The figure could also be used to show the effects of swinging the gate voltage above and below the quiescent VGG. The dashed curves in Figure 7-32 represent the transfer characteristics at a junction temperature of 25°C. Obviously, the curves vary enough to influence the selection of RS if the device experiences large swings in TJ.



VGG, GATE-TO-GROUND VOLTAGE (VOLTS)

FIGURE 7-31 — GRAPHICAL METHOD OF PREDICTING THE EFFECT OF A SOURCE RESISTOR ON THE QUIESCENT OPERATING POINT

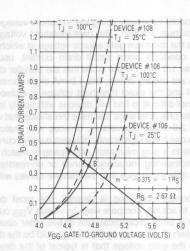


FIGURE 7-32 — USING A SOURCE RESISTOR
TO STABILIZE THE QUIESCENT OPERATING POINT

Paralleling MOSFETs in the Linear Mode

In many applications using MOSFETs in the linear mode, the quest is to obtain large swings in the load voltage and utilize as much of the maximum drain-to-source voltage rating as possible. With a large quiescent drain voltage, IDQ must be fairly small to keep the MOSFET power dissipation within manageable levels.

Unfortunately, paralleling in the linear mode at a low I_{DQ} and a high V_{DSQ} is not as straightforward as paralleling in switching applications, for instance. Since this is the most difficult and most common case of paralleling in the linear mode, it is the one that is addressed here.

One problem is that at low currents the potential I_D mismatches, as a percent of the total load current are much greater. As an illustration, one device may conduct 0.3 A at a V_{GS} of 5.0 V, whereas a second device may conduct 1.25 A at the same V_{GS} . If these two devices are operated in parallel in the linear mode, the second would dissipate far more power than the first. Unlike MOSFETs that are paralleled in switching applications, the difference in junction temperature forces an even greater disparity in the amount of current each device conducts.

As explained earlier, at low drain currents the temperature dependence of the drain current is dominated by the negative temperature coefficient of VGS(th) rather than the positive coefficient of rDS(on). Consequently, the device that is dissipating the most power will heat up, carry more current and dissipate even more power.

Although the situation appears to be hopeless — very wide variations in gFS curves causing even greater differences in power dissipation — the use of source resistors can minimize the differences and dramatically improve the chance of success.

not as great as expected. While the device that carried the most current ran hotter, it did so by only a couple of degrees (83 versus 85°C). A difference of 5 to 10°C was expected but did not materialize, most likely due to slight variations in the heat sinks. The MOSFETs were mounted on separate heat sinks, again to simulate a worst case condition. Close thermal coupling by placing units on the same heat sink is recommended to minimize variations in

To and Tu and therefore decrease any thermally induced

differences in ges curves.

temperatures were also monitored, but the difference was

In this study, the devices with widest variation in gFS curves were paralleled in the circuit shown in Figure 7-33. Individual source resistances of 3.3 Ω were chosen as a good compromise between a stable Q-point and the lower system gain are poorer efficiency attributable to an increase in RS. Table 5 establishes the equations for gfs and small signal voltage gain of paralleled MOSFETs with and without source resistors.

Using a source resistor to stabilize the operating point of devices with widely differing ges curves is also appli-

cable to improving current sharing among MOSFETs op-

erated in the linear mode. If the Q-points are closely matched, then the paralleled devices will, by definition.

carry nearly the same drain currents and incur approxi-

mately the same power dissipation.

Figure 7-34 shows the results of pairing the devices with the widest mismatch in gFS curves. Note how the drain currents can be predicted by relating the gFS curves (Figure 7-35) to the instantaneous gate voltage. Case

The benefits of device matching are shown in Figure 7-36. The nearly identical drain currents were obtained by matching devices by comparing the drain currents they would conduct at a VGS of 4.7 volts and a junction temperature of 25°C. The slight mismatch at higher drain currents is mainly due to a small difference in gFS curves at a TJ of 100°C. The case temperatures of these two devices were essentially identical. The 20 Ω gate resistors

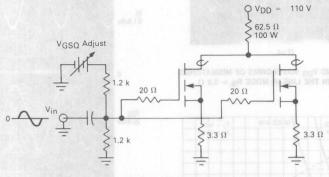


FIGURE 7-33 — CIRCUIT TO TEST CURRENT SHARING IN PARALLELED MOSFETS OPERATING IN THE LINEAR MODE

TABLE 5 — Equations for the Small-Signal Transconductance and Voltage Gain of Two Paralleled MOSFETs With and Without Individual Source Resistances.

ng MOSFETS	With No Source Resistors	With Individual Source Resistors, R _S
Small-Signal Transconductance	$\Delta I_{D1} = \frac{9FS1}{\Delta V_{GS}}, \ \Delta I_{D2} = \frac{9FS2}{\Delta V_{GS}}$ $\Delta I_{D1} + \Delta I_{D2} = \frac{9FS1 + 9FS2}{\Delta V_{GS}}$ $9FS1 + 9FS2 = \frac{\Delta I_{D1} + \Delta I_{D2}}{\Delta V_{GS}}$ $\therefore 9FST = 9FS1 + 9FS2$	$\begin{array}{ll} gFS1(\Delta V_{GS1}) = \Delta I_{D1}, gFS2(\Delta V_{GS2}) = \Delta I_{D2} \\ gFS1(\Delta V_{GG} - \Delta I_{D1} R_S) + gFS2(\Delta V_{GG} - \Delta I_{D2} R_S) = \\ \Delta I_{D1} + \Delta I_{D2} \\ gFS1(\Delta V_{GG}) + gFS2(\Delta V_{GG}) = \Delta I_{D1} (1 + gFS1 R_S) \\ + \Delta I_{D2} (1.0 + gFS2 R_S) \\ (gFS1 + gFS2)(\Delta V_{GG}) = (\Delta I_{D1} + \Delta I_{D2})(1.0 + gFS R_S), \\ where \overline{g}_{FS} = \frac{gFS1 + gFS2}{2} \\ \\ \therefore g'FST = \frac{\Delta I_T}{\Delta V_{GG}} \stackrel{:}{=} \frac{gFS1 + gFS2}{1.0 + \overline{g}_{FS} R_S} \end{array}$
Small-Signal Voltage Gain	$A_{V} = \frac{-\Delta V_{DS}}{\Delta V_{GS}}$ $= \frac{-\Delta I_{DT} R_{L}}{\Delta I_{DT/gFST}}$ $\therefore A_{VT} = -g_{FST} R_{L}$	$A'_{VT} = -g'_{FST} R_L$ $= \frac{-R_L(g_{FS1} + g_{FS2})}{1.0 + \bar{g}_{FS} R_S}$

Primed variables indicate the effective value for the MOSFET and source resistor combination Subscript "T" indicates the total value for all MOSFETs in parallel.

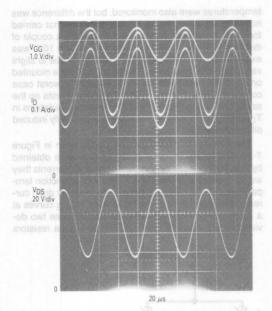


FIGURE 7-34 — V $_{\rm GG}$, I $_{\rm D}$ AND V $_{\rm DS}$ WAVEFORMS OF MISMATCHED MTP8N20 PARALLED IN THE LINEAR MODE R $_{\rm S}=3.3~\Omega$

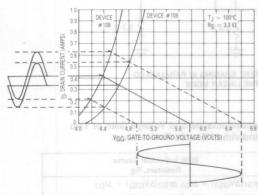


FIGURE 7-35 — TRANSFER CHARACTERISTICS AND RS LOADLINE OF MISMATCHED MTP8N18

in Figure 7-33 serve an important function. The high input impedance and high frequency capabilities of the MOSFET present the possibility of self-induced oscillations in paralleled devices. Inserting small resistances in series with each gate defuses the problem by degrading the Q of the LC network formed by the gate-and-drain inductances and the MOSFETs gate-to-drain capacitance. The magnitude of Rg necessary to allow trouble-free operation depends on the value of each of the circuit parasitics. The circuit in Figure 7-33 oscillated with series gate resistances of 10 $\Omega_{\rm c}$ but stabilized with 20 $\Omega_{\rm c}$ Increasing Rg results in a more stable circuit at the expense of lower bandwidth.

In conclusion, the same method used to stabilize the operating quiescent point of small signal MOSFETs can be easily extended to linear applications of power MOSFETs. After sampling a product line to obtain the widest expected variation in gFS curves, a simple graphical technique can be used to accurately predict the Q-point associated with a given source resistor and gate-to-ground voltage.

Since small variations in Q-point limit possible variations in drain current, successful paralleling is also achievable with this same method. The only additional consideration is the need to limit potential self-induced oscillations with individual gate suppression resistors.

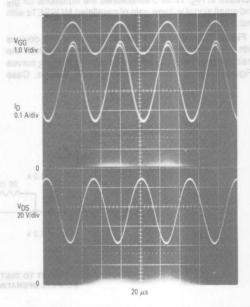


FIGURE 7-36 — $\rm V_{GG}$, $\rm I_{D}$ AND $\rm V_{DS}$ WAVEFORMS OF MATCHED MTP8N20 PARALLELED IN THE LINEAR MODE $\rm R_{S}=3.3~\Omega$

Applications of Paralleling MOSFETs

Paralleling Power MOSFETs in a Very Fast, High Voltage High Current Switch

There are many applications requiring an extremely fast high voltage, high current semiconductor switch, especially for device characterization, where the switch must be much faster than the device under test (DUT). Power MOSFETs serve this function extremely well, but they are presently limited in current capability. However, they can be readily paralleled to increase the current, without using current sharing ballast resistors, due to the inherent positive temperature coefficient of the drain-source ON-resistance rDS(on). For example, if the transconductance gFS of the FETs are unmatched, the FET with the highest gFS would tend to take initially the largest drain current, but due to the greater dissipation (ID2rDS(on)) and resulting temperature rise, rDS(on) would increase, thus, selflimiting the current. This process tends to equalize the drain currents of the respective devices.

A circuit for generating this fast pulse is shown in Figure 7-38. It uses 15 N-Channel power MOSFETs in parallel as the output power switch to achieve the system capability of 150 A of peak, pulsed current. The FETs used were unmatched TO-220 MTP5N40(2.7 V < VGS(th) < 3.9 V) with 400 V blocking capability V(BR)DSS, 5.0 A continuous drain current rating (10 A pulsed) and specified TDS(on) of 1.0 Ω max. The TO-220 devices lend themselves to efficient circuit layout and packaging (Figure 7-37).

The particular application for which this circuit was designed required the DUT to be referenced to ground (drain circuit); consequently, the switch is powered with a negative, high voltage supply $(-V_{SS})$ tied to the FETs sources. Thus, the ground referenced pulse generator output must be level translated to this negative supply. For fast switching, this translator must have the current drive capability for quickly charging the power MOSFETs input capacitances C_{ISS} and reverse transfer capacitance C_{TSS} . To accomplish this, two P-Channel MTP2P45's are

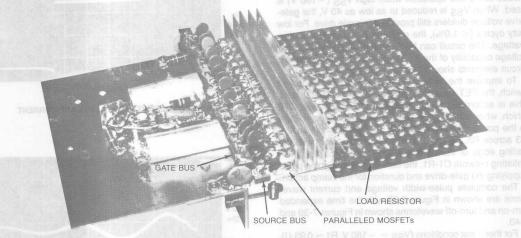


FIGURE 7-37 — BREADBOARD LAYOUT OF THE SWITCH ILLUSTRATING TIGHT PACKAGING CONCEPTS

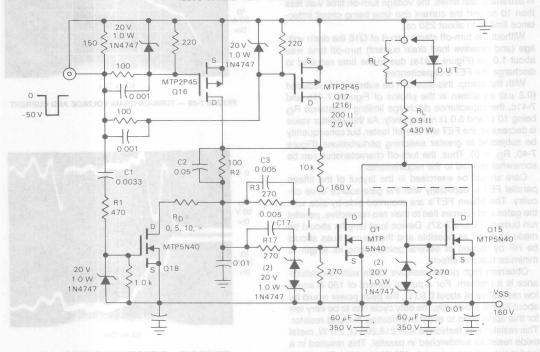


FIGURE 7-38 — PARALLELED POWER MOSFETs 150 A SWITCH

derived from a 50 V, 10 ns rise time pulse generator. A 20 V zener diode is used to protect the gate-source and still allows adequate gate-drive for rapid switching of the drain circuit. Connected to the drain is a current limiting resistor R2 (with speed-up capacitor C2) feeding the 15 respective gate circuits (only circuits 1 and 15 are shown); each circuit consists of a direct-coupled resistor, speed-up capacitor and protection zener diodes. The zener diodes come into operation when high VSS (-160 V) is used. When VSS is reduced to as low as 40 V, the gate-drive voltage dividers still provide adequate drive. For low duty cycles (< 1.0%), the resistors can be relatively low wattage. The circuit can be operated within the blocking voltage capability of the FETs (to 400 V), but the passive circuit elements should be scaled up accordingly.

To improve the turn-off switching times of the power switch, the FET capacitance must be quickly discharged.

configured as a parallel connected, series switch. These FETs are turned on by the negative going input pulse

To improve the turn-off switching times of the power switch, the FET capacitance must be quickly discharged. This is accomplished by the N-channel FET clamp Q18 which, when turned on, supplies the reverse gate voltage to the power switch through the voltage storing effect of C3 across R3. FET Q18 is turned on coincident with the trailing edge of the input pulse by means of the differentiating network C1-R1, the derived positive-going pulse supplying the gate-drive and duration for the clamp action.

The complete pulse-width voltage and current waveforms are shown in Figure 7-38 with the time expanded turn-on and turn-off waveforms shown in Figures 7-39 and 7-40.

For these test conditions (V_{SS} = -160 V, R1 ≈ 0.93 Ω), approximately 150 A at 140 V (21 kW peak) was switched in extremely fast times; the voltage turn-on time was less than 10 ns and the current rise time being circuit inductance limited to about 250 ns.

Without the turn-off clamp circuit of Q18 the drain voltage (and resistive load drain current) turn-off time was about 1.0 μ s (Figure 7-41a) due to the time required to discharge the FET's capacitances.

With the clamp, this time can be substantially reduced (0.2 $\mu s)$ as shown in the photos of Figures 7-41b and 7-41c, the capacitance discharge limiting resistance R_D being 10 Ω and 5.0 Ω respectively. As this resistor value is decreased, the FET will turn-off faster, but consequently be subjected to greater switching perturbations (Figure 7-40, $R_D=0$). Thus, the turn-off characteristics can be somewhat tailored to the requirements.

Care should be exercised in the layout of the fifteen parallel FET's, especially with the gate-source drive circuitry. The fifteen FET's are mounted side-by-side with the gates and sources tied to their two respective, parallel run busses (Figure 7-37). Device lead lengths should be made as short as possible and the source buss should be RF by-passed at several points along its length to minimize reactive effects.

Obtaining high power resistive loads with low inductance is a problem. For a pulsed current of 150 A and a low resistance of about 0.93 Ω , the peak power would be about 21 kW. Obviously, the duty cycle has to be very low for this application to avoid overheating the load resistor. This resistor was fashioned with 216,200 Ω , 2.0 W, metal oxide resistors sandwiched in parallel. This resulted in a load resistor of approximately 430 W capability. Therefore,

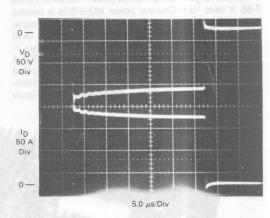


FIGURE 7-38 — SWITCHED VOLTAGE AND CURRENT

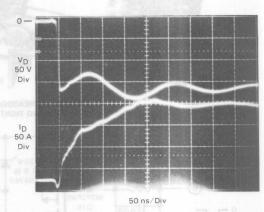


FIGURE 7-39 — TURN-ON DRAIN VOLTAGE AND CURRENT

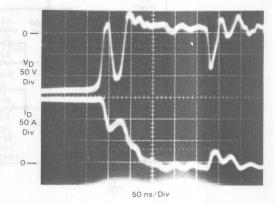


FIGURE 7-40 — TURN-OFF WITH CLAMP, $R_D = 0$

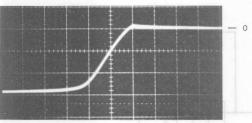


FIGURE 7-41a — TURN-OFF DRAIN VOLTAGE RD = ∞

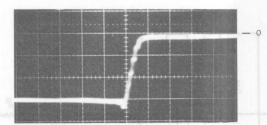
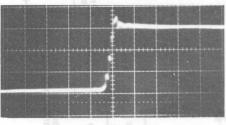


FIGURE 7-41b — TURN-OFF DRAIN VOLTAGE $R_D = 10 \Omega$



Vert. = 500 V/Div Horiz. = 500 ns/Div

FIGURE 7-41c — TURN-OFF DRAIN VOLTAGE $R_D = 5.0 \ \Omega$

duty cycles of less than 1.0% should be used to ensure operation within the load rating while still offering good oscilloscope viewing.

Fast, Complementary Power MOSFET Switch

Many present day semiconductors require test circuits that can supply large pulsed currents and fast voltage transitions.

In today's real world circuits, rectifiers are vital components in motor controls and in switching power supplies as the operating frequency and power level increases. Rectifier characteristics and selection can be critical for these applications.

Due to its fast switching speed, the complementary power FET switch, shown in Figure 7-42, is useful in measuring forward (t_{fr}) and reverse (t_{rr}) recovery times of fast recovery rectifiers, as well as for general uses requiring a complementary power signal.

The internal collector-emitter diode in power Darlington transistors and the drain-source diode in power FETs can be of great interest to the circuit designer. Rectifier operation is dependent on several conditions, two of which are the turn-off rate (di/dt) of forward current and the rate of rise (dv/dt) of the reapplied blocking voltage.

In some switching power supplies, a designed-in dead time is required between the switching transistors to avoid simultaneous conduction. The duration of the dead time and the dv/dt of the reapplied blocking voltage can be

critical, especially for some power MOSFETs. This complementary switch, with dv/dt adjustment and control of the dead time, can help determine the capability of power FETs in circuits when the above conditions are important.

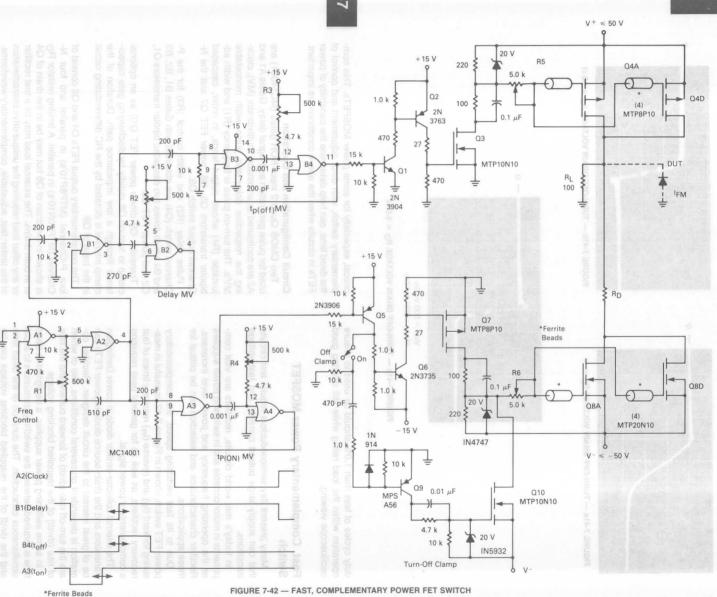
Circuit Configuration and Operation

Two CMOS Quad 2 input NOR gates (MC14001) are used for pulse generation and signal delay. Gates A1 and A2 are configured as an astable multivibrator (MV), clocking the respective delay and pulse width monostable MV's. The turn-on pulse is frequency (R1) and width adjustable (R4) whose output feeds, in order, cascaded bipolar transistors Q5, Q6, power FET Q7 and the N-Channel output switch Q8.

Pulse delay (R2) and width control (R3) for the P-Channel switch (Q4) are obtained with Gates B1, B2, B3 and B4 which drives two cascaded bipolar transistors Q1, Q2 and power FET Q3.

Transistor Q9 drives power FET Q10 as an optional clamp to turn-off Q8 rapidly by discharging gate capacitance through a low impedance path. Duration of the clamp interval is dictated by the RC differentiating circuit in the base of Q9.

The complementary output FETs Q4 and Q8 consist of four P-Channel (MTP8P10's) in parallel and four N-Channel (MTP20N10's) in parallel. A limiting resistor RD is shown in the drain of Q8 but may be in the drain of Q4 or in both drains. The external load may be a test rectifier or any other load requiring the unique drive characteristics of this tester: fast, adjustable, complementary waveforms.



The negative output switch Q8 (N-Channel) is capable of switching at least 100 A, whereas the positive switch Q4 (P-Channel) is limited to about 50 A due to the differences in the respective on-resistances. Additional devices can be paralleled for either switch for higher currents, if so required. Also, power FETs with higher VDSS ratings may be used.

Output Waveforms

The negative and positive switched output waveforms are shown in Figures 7-43a and 7-43b, with the positive voltage delayed about 2.0 μs , in Figure 7-43a. The external load resistor R_L is about 2.0 ohms, with the switched voltages of about \pm 42 volts.

In Figure 7-43a, the switched negative and positive voltages have very fast leading edges (about 10 ns) and slow

trailing edges (about 3.0 μ s and 1.0 μ s, respectively). Figure 7-43b shows the same switched voltages but with the clamp transistor (Q10) switched on. This discharges Q8 gates through a low impedance path and speeds up the trailing edge of the negative voltage to about 25 ns instead of 3.0 μ s.

In Figure 7-45, a MR821 fast recovery rectififer is shown as the load, with $I_{FM} = 40$ A, di/dt = 300 A/ μ s, and the dv/dt of the applied blocking voltage about 2500 V/ μ s.

Adjustment of dv/dt is accomplished with R5 for the positive switched voltage and with R6 for the negative voltage

Figure 7-44 shows the transition time of about 35 ns between the negative and positive voltages, with both the clamp on and with Q4 diverting current from Q8.

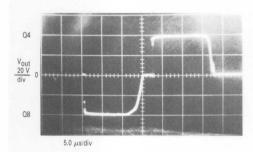


FIGURE 7-43a — FAST LEADING EDGE

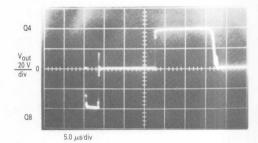


FIGURE 7-43b — FAST TRAILING EDGE, NEG. VOLTAGE, TURN-OFF CLAMP Q10 "ON"

FIGURE 7-43 — NEGATIVE AND POSITIVE SWITCHED OUTPUT VOLTAGE WITH RL - 2.0 $\Omega,$ V $^-$ AND V $^+\approx$ 42 V, DRAIN Q8

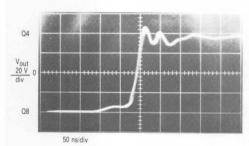


FIGURE 7-44 — NEGATIVE AND POSITIVE TRANSITION, DRAIN Q8, TURN-OFF CLAMP Q10 "ON"

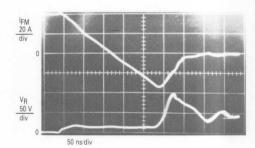
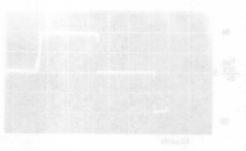
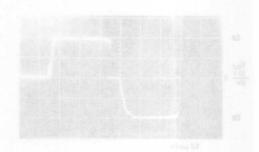
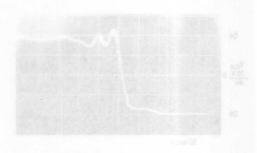


FIGURE 7-45 — REVERSE RECOVERY $(t_{\Gamma\Gamma})$ OF MR821 FAST RECOVERY RECTIFIER











Chapter 8: TMOS Applications 100 kHz Switch Mode Power Supply

Power FETs have proven themselves to be performance competitive and cost effective in flyback regulators operating at 100 kHz to 200 kHz.

The circuit described here proves the point. It is a 60 W 100 kHz FET switcher with four output voltages \pm 5.0 V and \pm 12 V. It operates from 120 Vac, has an efficiency of 75% and the total parts cost is approximately \$35.

Components unique to this high frequency design include the following:

- Motorola's MTP5N40 power FET. This 5.0 A, 400 V device has only one ohm of on-resistance and is driven directly from a linear IC. It not only switches in less than 50 ns but has enough RBSOA to eliminate the need for snubbers.
- Pulse Engineering's PE63133 power transformer.
 This is a continuous mode flyback transformer which is ideally suited to high frequency operation. Zener clamps are not required because the clamp winding is interleaved with primary halves. Regulation of the auxillary outputs is within ± 10% under varying conditions of line and load.
 - Motorola's MC34060 Switchmode control IC, 4N27 optoisolator, and MC1723 linear regulator. These devices are used in a practical demonstration of a low-cost, three-chip control system. The MC1723 is the error amplifier, the MC34060 is a fixed frequency PWM, and the 4N27 couples the feedback signal from the MC1723 to the MC34060.
 - Motorola's MBR1035 (TO-220) Schottky rectifier was used to rectify the +5.0 V output at half the cost of a comparable DO-4. Similar cost savings result from using the TO-220 fast recovery rectifiers, i.e., the MUR805 in the ± 12 V outputs.
 - Mepco/Electra's 3428 series of output capacitors.
 These high frequency electrolytics feature low ESR and high RMS current ratings. Only 50 to 70 mV (PP)

of ripple occurs at the outputs. Power loss is less than 0.5 W.

Circuit Design at a pulled vignile vid best

The goal of most low-power flyback designs is for reduced parts count (or size) and reduced cost. The 60 W 100 kHz switcher shown schematically in Figure 8-1, met these requirements. At 100 kHz, the transformer size and cost are reduced by about 30% compared with a 20 kHz design. Also, at 100 kHz, a FET can be driven directly from logic circuits (100 to 200 mA) and still switch very efficiently. This eliminates the need for drive interface circuits. The output caps used are about 50% smaller and they cost less as well. Finally, a relatively new three-chip control system is used. It replaces an expensive and performance limited drive transformer with a lower-cost optocoupler.

The FET is the control element for the flyback transformer and is directly driven from the MC34060 linear IC. A rather standard off line starter circuit is used to initially power the control circuit and this is also lower in cost than the filament transformer supply which is often used to power a single-chip system. The design procedure followed here was:

- 1. Design and test the power stage.
- 2. Add and stabilize the control loop.
- 3. Change from dc to ac power.

The FET waveforms obtained with the design are shown in Figure 8-2. The exceptional switching speed of the FET can be varified here (less than 50 ns) and ringing on the current waveform is due to the layout which includes a current-sense loop and noise pickup on the scope probe.

The input capacitor does not reduce in size like the outputs because it is needed for energy storage which still occurs at 60 Hz. Noise filters used here include a toroid from PE and the economical 41GS series of tan-

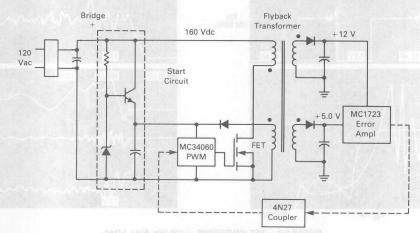


FIGURE 8-1 — REGULATOR BLOCK DIAGRAM

Chapter 8: TMOS Applications

talum capacitor from M/E. The 12 V output rectifiers were Motorola's MUR805 ultrafast recovery button rectifiers which are housed in a TO-220 package. They were ideally suited to this relatively high current (10–15 A peak) application because the correct amount of heat sinking was easily attained by simply bolting a fin to the tab.

The relatively new MBR1035 TO-220 Schottky rectifier is the best choice for rectifying the 5.0 V output. It is about half the cost of the equivalent DO-4 version, a 1N6095.

The overall efficiency of this regulator (including the control circuits) is 75%. As usual, most of the losses are associated with the power handling components as noted in Table 1.

TABLE 1 — Efficiency Data

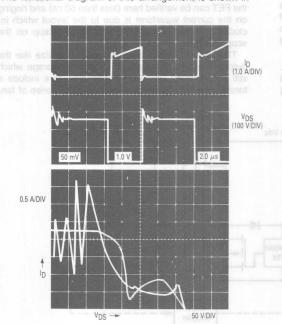
1. Input Power				
Vineend weny	svitslin 8	PPRMS	PA	PF
160 Vdc	0.6 A	96	96	100%
120 Vac	1.4 A	170	95*	56%
*Note using Clark	Hess wattme	ter.		
2. Output Power				
Winding	5.0	-5.0	+12.0	- 12.0
Load (ohms) Voltage	1.0	10.0	8.0	8.0 13.3
Voltage	5.1	5.1	13.2	13.3
Power			21.5	22.0
3. Efficiency				
Eff. = P_0/P_{in} = 1	72 W/95 W =	75%		
4. Estimated Los	sses			
FET	4.0 W	Fast Recove	ery (both)	8.0 W
Schottky	4.0 W	Misc.		5.0 W
Transformer	2.0 W			

The control loop contains three chips as noted earlier.
The functional diagram of this arrangement is shown in

Figure 8-3. The first chip is an MC1723 linear regulator. It is used here to provide a $5.0\,\mathrm{V}$ reference and an error amplifier. It is powered from the $+12\,\mathrm{V}$ output winding and receives feedback or control signal from the $+5.0\,\mathrm{V}$ output. The MC1723 drives the second chip, a 4N27 optocoupler. The coupler maintains isolation between the primary and secondary windings and couples the dc control signal to the input of the third chip, a MC34060. The MC34060 performs a fixed frequency pulse width modulator (PWM) function and is used to directly drive the FET power switch which is connected to the primary or energy storage winding.

The key regulating blocks are the 0 to 3.0 V sawtooth oscillator and the feedback comparator. As the feedback signal is raised from 0 to 3.0 V, it gradually narrows the on time of output pulse coming from the comparator. During start up, the feedback is missing and resistor divider network controls the second or dead-time comparator to ensure that on time cannot exceed 45%. This, and the soft start capacitor, prevents transformer saturation problems during start-up. Pull down of the gate voltage is accomplished as shown in Figure 8-3 with the addition of a low cost TO-92 PNP transistor (Q3). In this design, the MC34060 is started off line with the addition of a 200 V transistor (Q2) and 12 V zener as shown in Figure 8-4. It ultimately (at normal line voltage) runs off the 12 V auxiliary winding which back biases this transistor. Because it and the FET gate draw so little current from the line, about 20 mA, undervoltage inhibiting common to bipolar designs was not required here and this current becomes functional and runs safely when the input reaches 40 Vac.

The performance of this 100 kHz switcher is similar to most others. It is relatively easy to keep output ripple, both



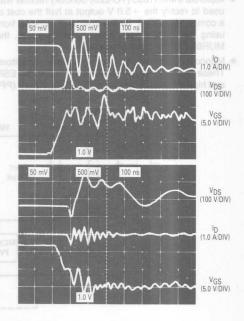
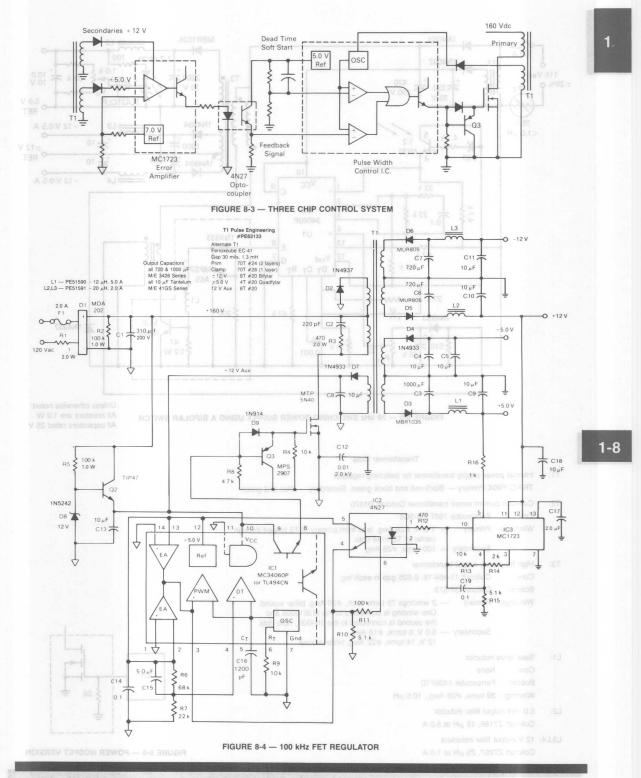


FIGURE 8-2 — FET WAVEFORMS — 120 Vac. FULL LOAD





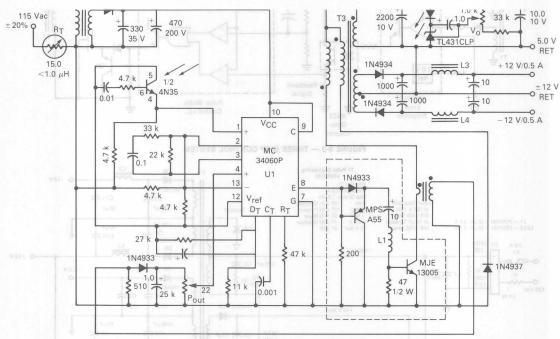


FIGURE 8-5 — 20 kHz SWITCHING POWER SUPPLY USING A BIPOLAR SWITCH

Unless otherwise noted: All resistors are 1/2 W All capacitors rated 25 V

Transformer Data

- T1: Internal power supply transformer for switching regulator TRAID F90X Primary — Black-red and black green. Secondary — Blue and green
- T2: Collector current sense transformer Coilcraft D1870

Core: Ferroxcube 768T183-3C8

Windings: Primary — 1 turn, #26 Awg. lead from primary of T3 looped through

center of T2, note dots. Secondary - 100 turns, #28 Awg.

High frequency output transformer

Core: Coilcraft 11-464-16, 0.025 gap in each leg.

Bobbin: Coilcraft 37-573

- 2 windings 75 turns each, #26 Awg, bifilar wound. Windings: Primary

One winding is connected to the MJE13005 and

the second is connected to the 1N4937, note dots.

Secondary - 5.0 V, 6 turns, #16 Awg.

12 V, 14 turns, #22 Awg, bifilar wound.

L1: Base drive inductor

Core: None

Bobbin: Ferroxcube 1408F1D

Winding: 39 turns, #28 Awg., 10.5 μH

L2: 5.0 Volt output filter inductor Coilcraft Z7156, 15 µH at 5.0 A

L3,L4: 12 V output filter inductors

Coilcraft Z7257, 25 µH at 1.0 A

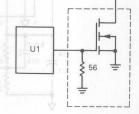


FIGURE 8-6 - POWER MOSFET VERSION

60 Hz and 100 kHz, below 100 mV on all outputs. (See Table 2.) Line regulation here was excellent, less than 0.1%, but load reg (2.0%) could have been better. Normally tight layouts and higher loop gain can get this down to 0.1 to 0.5% as well. Efficiency (75%) and cross regulation (\pm 10%) are also similar to other multiple output switcher designs.

TABLE 2 — Output Data

 Ripple Voltages (12) 	Vac, Full Loa	ad)		
Winding 100 k Ripple (PP) 60 Hz Ripple (PP) Noise Spikes (PP)	+ 5.0 60 mV 20 mV 2.0 V	-5.0 300 mV 50 mV 2.0 V	+ 12 70 mV 70 mV 2.0 V	50 mV 60 mV 2.0 V
2. +5.0 V Regulation	\$ 200 \$ 22	CTI		-
Line Load Voltage	100 Vac Full 5.10	100 Vac Half* 5.21	130 Vac Full 5.10	130 Vac Half 5.21

*Note: +5.0 V Load increased to 2.0 ohms and -12 V load removed. Load Reg. = $\Delta V_0/V_0$ = 0.11/5.1 = 2.2%. Line Reg. $\Delta V_0/V_0$ = 0.005/5.1 = 1.0%.

20 kHz Switcher

A less novel 20 kHz flyback switcher provides a good illustration of the interchangeability of FETs and bipolar transistors. The 35 watt supply shown in Figure 8-5 was originally designed around the MJE13005 bipolar output transistor. With the bipolar, crossover time and case temperature rise were measured with $V_{\rm in}$ at 160 Vdc and outputs fully loaded.

A view of the crossover waveforms is shown in Figure 8-7. At the full load case temperature of 71°C, the MJE13005 is turning on in a crossover time of slightly under one microsecond. (46°C case temperature rise).

providing a good relative measure of its efficiency as a switching element.

When an MTP4N50 FET is substituted for the bipolar transistor, the drive circuit is greatly simplified as illustrated in Figure 8-7. Now the MC34060 control circuit is capable of directly driving the FET, eliminating the complex base drive circuitry required for the bipolar. The end result is that the FET can be substituted for the bipolar by removing five components and changing one resistor value. Thus, the FET substitution results in a reduced components count.

Performance wise, the FET is the better choice, with a considerably improved crossover time, Figure 8-8, and a case temperature rise of only 18°C.

Automotive DC-DC Converter

In the previous example, FET drive circuitry was maximally simplified. The penalty for this simplification is that turn-on gate-source voltage, applied across a relatively low gate-source resistor, draws approximately as much drive power as a bipolar would. This example illustrates how the FET's low drive power requirements can be used advantageously. The circuit, shown in Figure 8-9, is a 25 watt DC-DC converter that is designed for automotive use. It uses the same control IC as the previous example. The significant difference is the addition of Q1, D3, & D6 to the drive loop. This arrangement provides a low impedance loop for fast turn-off, while drawing a negligible amount of current from the IC after the FET is turned-on.

The FET and this circuit work well together. Efficiency was measured at 78% with V_{in} at 13.6 volts, load regulation at 0.4%/Amp., and line regulation at 0.01%/volt. In general, the comparatively low rDS(on) of FETs with 100 V (or less) ratings makes the FET a particularly good choice for this type of application.

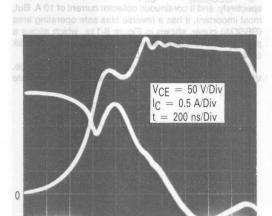


FIGURE 8-7 — BIPOLAR CROSSOVER TIME

The advantages of power MOSIFETs over bipolars nigh input impedance (low drive power), fast switching, freedom from second breakdown — have been cited many times and can clearly be shown when the two tech-

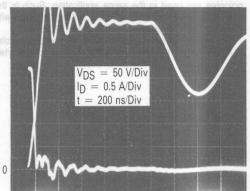
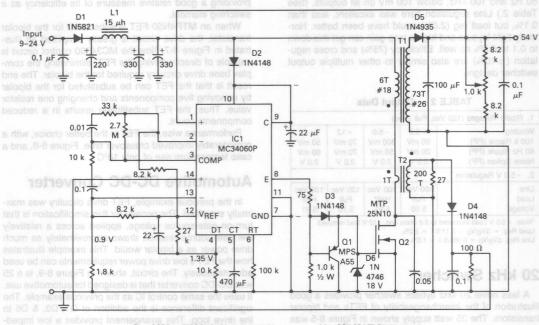


FIGURE 8-8 — FET CROSSOVER TIME



- T1: CORE = FERROXCUBE 3019-L00-3C8
 BOBBIN = FERROXCUBE 3019F-1D
 GAP = 0.015"
- L1: COILCRAFT Z7156, 15 μH L2: COILCRAFT Z7157, 25 μH
- el eggo drus entil tevt
- yanelolikili Jerflegol llew Mow T2::COILCRAFT D1871:CURRENT SENSE XFMR. IS 35V 031 Js $_{\rm HI}$ V dliw beni--upen bsol Jaflov 3.81 Js $_{\rm HI}$ V T3::V CORE = COILCRAFT.11:464-41 EE-19
 - BOBBIN = COILCRAFT 37-612-001 GAP = 0.0075"

FIGURE 8-9 — AUTOMOTIVE DC-DC CONVERTER

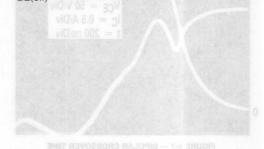
High Voltage Flyback Converter

The advantages of power MOSFETs over bipolars — high input impedance (low drive power), fast switching, freedom from second breakdown — have been cited many times and can clearly be shown when the two technologies are used in the same application. Such is the case when a HV flyback converter, initially designed with a bipolar, was redesigned for the power MOSFET.

The first design used a Switchmode high-voltage bipolar MJ8505 output transistor in a PWM flyback converter,

Figure 8-10c. This transistor has breakdown voltage ratings VCEO(sus) and VCEV of 800 V and 1400 V, respectively, and a continuous collector current of 10 A. But, most important, it has a reverse bias safe operating area (RBSOA) curve, shown in Figure 8-11a, which allows a peak flyback voltage of about 700 V, generated by a peak collector current in the 3.0 to 4.0 A range.

To achieve this RBSOA capability an off-bias voltage, $V_{BE(off)}$, of about -5.0~V is required. Also, since there



is a trade-off of β with high-voltage transistors ($\beta_{min}=7.5$ at $I_{C}=1.5$ A), a low forced beta β_{F} of about 2.5 ($I_{BI}\approx1.5$ A) was chosen to ensure device saturation. To produce clean, monotonic, relatively fast clamped inductive turn-off waveforms, the Baker Clamp network of diodes (D2–D4) is suggested. Consequently, a power amplifier consisting of an I_{BI} forward base current circuit (transistors Q1 and Q2) and an off-bias circuit (transistors

Q3 and Q4) is required to interface the low level PWM with the MJ8505. The PWM (U1), for this example, need only provide a +5.0 V pulse to the power Amp with about 20 mA sourcing and sinking capability.

If, however, the output device is a comparably rated power MOSFET, MTM2N90 the drive circuitry can be greatly simplified, with the resulting savings in cost and improved reliability. Moreover, the faster switching

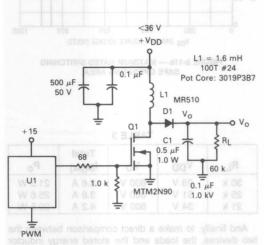


FIGURE 8-10a — SINGLE MOSFET OUTPUT

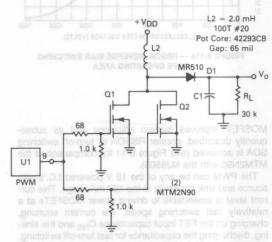


FIGURE 8-10b — TWO PARALLEL MOSFET OUTPUT

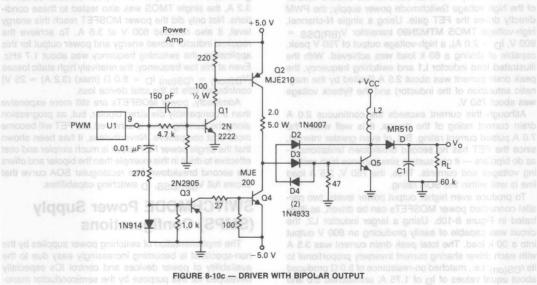


FIGURE 8-10 — HIGH VOLTAGE FLYBACK CONVERTER WITH POWER MOSFET & BIPOLAR OUTPUTS

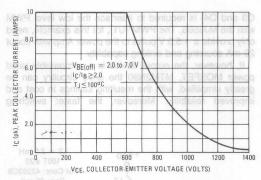
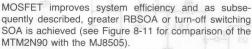


FIGURE 8-11a — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



The PWM can be any of the 15 V powered I.C.'s with source and sink capability in the 100 mA range. This current level is amendable to driving power MOSFETs at a relatively fast switching speed, the current sourcing, charging up the FET input capacitance $C_{\rm iSS}$ and the sinking, discharging the capacitance for fast turn-off switching. Also, the near 15 V PWM output ensures that the FET is well turned on.

This is exactly what was done for the second version of the high voltage Switchmode power supply; the PWM directly drives the FET gate. Using a single N-channel, high-voltage TMOS MTM2N90 transistor $V_{(BR)DSS} = 900 \text{ V}, I_D = 2.0 \text{ A})$, a high-voltage output of 750 V peak, capable of driving a 60 k load was achieved. With the illustrated load inductor L1 and switching frequency, the peak drain current was about 2.5 A (limited by the magnetic saturation of the inductor) and the flyback voltage was about 750 V.

Atlhough this current exceeds the continuous 2.0 A drain current rating of the device, it is well within the 7.0 A pulsed current rating. But, of even greater interest, since the FET has no second breakdown limitations—as do bipolars—it can sustain simultaneous high switching voltages and currents. Thus, the 750 V, 2.5 A load line is well within the SOA rating.

To produce even higher output power levels, two parallel connected power MOSFETs can be driven, as illustrated in Figure 8-10b. Using a larger inductor L2, the circuit was capable of easily producing an 800 V output into a 30 k load. The total peak drain current was 3.5 A with each driver sharing current inversely proportional to its rDS(on): i.e., matched on-resistance of 5.0 Ω produced about equal values of ID of 1.75 A, unmatched 5.0 and 8.0 Ω , about 2.1 A and 1.4 A respectively. Reducing the load resistance even further, resulted in greater power output, with the individual device drain current being well within spec limits, as shown in Table 3:

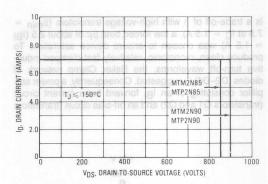


FIGURE 8-11b — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

TABLE 3

R _L V _{DD}		Vo	Total ID(pk)	Po	
30 k	28 V	800 V	3.6 A	21.3 W	
25 k	31 V	800 V	3.8 A	25.6 W	
21 k	34 V	800 V	4.2 A	30.5 W	

And finally, to make a direct comparison between the two devices, the loads and the stored energy inductor should be the same. Since the bipolar originally was tested with the larger inductor and a 30 k load to produce as great as a 700 V output from a peak collector current of 3.2 A, the single TMOS was also tested to these conditions. Not only did the power MOSFET reach this energy level, it also reached 800 V at 3.6 A. To achieve the required inductor stored energy and power output for this application, the switching frequency was about 1.7 kHz. Even at this low frequency, the relatively high static losses $[VDS(on)] = rDS(on) \cdot D = 8.0 \Omega \, (\text{max}) \, (3.2 \, \text{A}) \approx 25 \, \text{V}]$ contributed little to the total device loss.

Admittedly, power MOSFETs are still more expensive than a comparably die sized bipolar, but, as progression along the learning curve is achieved, the FET will become more cost competitive. Nevertheless, it has been shown that the single power FET circuit is much simpler and cost effective to drive in this example than the bipolar and offers the second breakdown free rectangular SOA curve that allows full V_{(BR)DSS}, ID switching capabilities.

SWITCHMODE Power Supply (SMPS) Configurations

The implementation of switching power supplies by the non-specialist is becoming increasingly easy due to the availability of power devices and control ICs especially developed for this purpose by the semiconductor manufacturer.

This section is meant to help in the preliminary selection of the devices required for the implementation of the listed switching power supplies.

Flyback Switching Power Supplies: 50 W to 250 W

- Input line variation: V_{in} + 10%, 20%
- Converter efficiency: $\eta = 80\%$
- Output regulation by duty cycle (δ) variation: $\delta_{\text{max}} = -0.4$
- Maximum MOSFET working current:

$$I_{W} = \frac{2.0 \text{ P}_{out}}{\eta \cdot \delta_{max} \cdot \sqrt{\text{in}} (\text{min}) \cdot \sqrt{2.0}} = \frac{5.5 \text{ P}_{out}}{V_{in}}$$

- Maximum FET working voltage: No. 2011 Bugnt & VDSW = 2.0 Vin(max) √2.0 offer refreshood
- Minimum FET drain-source voltage: per JuduO
 VDS ≥ 1.2 VDSW
 8.0 = xsm⁶

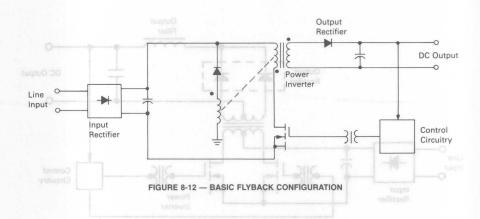


TABLE 4 — Flyback Semiconductor Selection Chart

Output Power	50	W	100 W		175 W		250 W	
Input Line Voltage, Vin	120 V	220 V	120 V	220 V	120 V	220 V	120 V	
50 V 20 V 20 V	250 W	or 240 V	W-00	or 240 V		or 240 V	to)/ eai.l tuant	
MOSFET Requirements Max Working Current, I _W Max Working Voltage, V _{DSW}	2.25 A 380 V	1.2 A 750 V	4.0 A 380 V	2.5 A 750 V	8.0 A 380 V	4.4 A 750 V	11.4 A 380 V	
Power MOSFETs Recommended Metal (TO-204AA) (TO-3) Plastic (TO-220AB) Plastic (TO-218AC)	MTM4N45 MTP4N45	MTM2N90 MTP2N90	MTM4N45 MTP4N45	MTM2N90 MTP2N90	MTM7N45 — MTH7N45	MTM4N90	MTM15N45	
Input Rectifiers Max Working Current, IDC Recommended Types	0.4 A MDA104A	0.25 A MDA106A	0.4 A MDA206	0.5 A MDA210	2.35 A MDA970	1.25 A MDA210	4.6 A MDA3506	
Output Rectifiers Recommended types for Output Voltage of: 5.0 V 10 V 20 V 50 V 100 V	MBR3 MUR3 MUR1 MUR1	035PT 010PT 615CT 615CT MUR840A	MBR3 MUR3 MUR1 MUR1	035PT 010PT 615CT 615CT 840A	MUR10 MUR3 MUR1	2035CT 0010CT 015PT 615CT 840A	MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	MUR1615C MUR840A See Table	MC3423,	MC3424; Colifier: SING	vervoltage GLE TL431;		438, LM358	Recommende	

Push-Pull Switching Power Supplies: 100 W to 500 W

- Input line variation: Vin + 10%, 20%
- Converter efficiency: $\eta = 80\%$
- Output regulation by duty cycle (δ) variation: M = δmax = 0.8
- Maximum MOSFET working current:

$$I_{W} = \frac{P_{out}}{\eta \cdot \delta_{max} \cdot V_{in(min)} \cdot \sqrt{2.0}} = \frac{1.4 P_{out}}{V_{in}}$$

- Maximum FET working voltage:
 VDSW = 2.0 Vin(max) √2.0
- Minimum FET drain-source voltage: NDS ≥ 1.2 VDSW
- Working frequency: f = 20 to 200 kHz

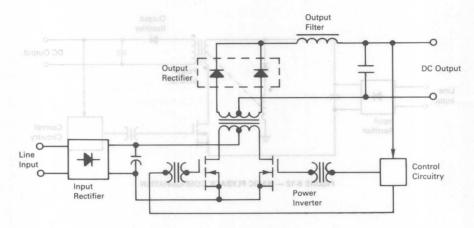


FIGURE 8-13 — BASIC PUSH-PULL CONFIGURATION

1-8

TABLE 5 — Push-Pull Semiconductor Selection Chart

Output Power	10 100	O W	250 W		500 W	
Input Line Voltage, V _{in}	120 V	220 V 240 V	120 V	220 V 240 V	120 V stnementupe	220 V 240 V
MOSFET Requirements Max Working Current, I _W Max Working Voltage, V _{DSW}	1.2 A 380 V	0.6 A 750 V	2.9 A 380 V	1.6 A 750 V	5.7 A 380 V	3.1 A 750 V
Power MOSFETs Recommended Metal (TO-204AA) (TO-3) Plastic (TO-220AB) Plastic (TO-218AC)	MTM2N50 MTP2N45	MTM2N90 MTP2N90	MTM4N4 MTP4N4		MTM7N45 MTH7N45	MTM4N90
Input Rectifiers Max Working Current, IDC Recommended Types	0.9 A MDA206	0.5 A MDA210	2.35 A MDA970	and the second s	4.6 A MDA3506	2.5 A MDA3510
Output Rectifiers: Recommended types for output voltages of: 5.0 V 10 V 20 V 50 V 100 V	MBR3035PT MBR3045PT MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	WIGHE FLAST:	Ampliner: Sir	Se	e Table 4		

Half-Bridge Switching Power Supplies: 100 W to 500 W

- Input line variation: Vin + 10%, 20%
- Converter efficiency: $\eta = 80\%$
- Output regulation by duty cycle (δ) variation: $\delta_{\text{max}} = 0.8$
- Maximum MOSFET working current: $I_{W} = \frac{2.0 \; P_{Out}}{\eta \cdot \delta_{max} \cdot V_{in}(min) \cdot \sqrt{2.0}} = \frac{2.8 \; P_{Out}}{V_{in}}$
- Maximum FET working voltage; when bugnles $V_{DSW} = V_{in(max)} \cdot \sqrt{2.0}$
- Minimum FET drain-source voltage: V_{DS} ≥ 1.2 • V_{DSW}
- Working frequency: f = 20 to 200 kHz

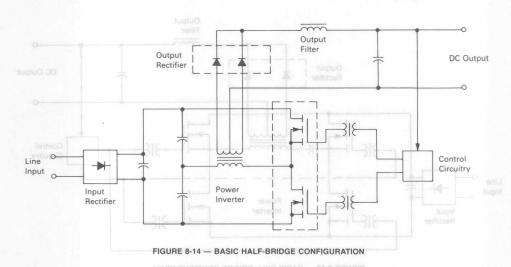


TABLE 6 — Half-Bridge Semiconductor Selection Chart

Output Power		007 100	W	350	W	tewo9 Juc500	W					
Input Voltage, Vin	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V					
MOSFET Requirements Max Working Current, I _V Max Working Voltage, V	v A T A	2.3 A 190 V	1.25 A 380 V	5.7 A 190 V	3.1 A 380 V	11.5 A 190 V	6.25 A 380 V					
Power MOSFETs Recomm Metal (TO-204AA) (TO-3 Plastic (TO-220AB) Plastic (TO-218AC)		MTM5N35 MTP3N40	MTM2N45 MTP2N45	MTM8N40 — MTH8N40	MTM4N45 MTP4N45	MTM10N25 MTP10N25	MTM7N45 — MTH7N45					
Input Rectifiers Max Working Current, IDC A 8 8 Recommended Types		0.9 A MDA206	0.5 A MDA210	2.3 A MDA970-5	1.25 A MDA210	4.6 A MDA3506	2.5 A MDA3510					
Output Rectifiers: Recommended types for output voltage of: TOO OOTHUM TOO OOTHUM TOO OOTHUM TOO OOTHUM TOO OOTHUM TOO OOTHUM	5.0 V 10 V 20 V 50 V 100 V	MBR3035PT MBR3045PT MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A						
Recommended Control Cir	rcuits	151 556		See T	able 4	See Table 4						

- Output regulation by duty cycle (δ) variation: $\delta_{\text{max}} = 0.8$

• Maximum MOSFET working current:
$$I_{W} = \frac{P_{out}}{\eta \cdot \delta_{max} \cdot V_{in(min)} \cdot \sqrt{2.0}} = \frac{1.4 P_{out}}{V_{in}}$$

- Maximum MOSFET working voltage: $V_{DSW} = V_{in}(max) \cdot \sqrt{2.0}$
- Minimum FET drain-source voltage: V_{DS} ≥ 1.2 · V_{DSW}
- Working frequency: f = 20 to 200 kHz

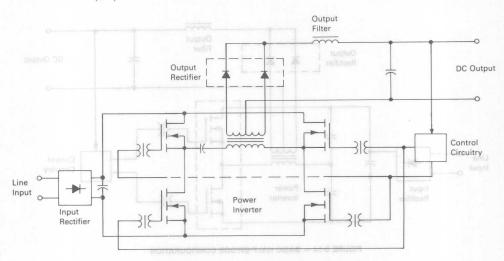


FIGURE 8-15 — BASIC FULL-BRIDGE CONFIGURATION

TABLE 7 — Full Bridge Semiconductor Selection Chart

Output Power	W	028 500) W	750	W	100	0 W
Input Voltage, Vin	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements Max Working Current, I Max Working Voltage, \		5.7 A 190 V	3.1 A 380 V	8.6 A 190 V	4.7 A 380 V	11.5 A 190 V	6.25 A 380 V
Power MOSFETs Recommended (TO-204AA) (TO-Plastic (TO-220AB) Plastic (TO-218AC)		MTM8N20 MTP8N20	MTM4N45 MTP4N45	MTM10N25 MTP10N25	MTM7N45 MTP4N45 MTH7N45	MTM15N20 MTP12N20 MTH15N20	MTM7N45 — MTH7N45
Input Rectifiers Max Working Current, I Recommended Types	1.25 A OC	4.6 A MDA3506	2.5 A MDA3510	7.0 A	3.8 A OO	9.25 A	5.0 A
Output Rectifiers: Recommended types for output voltages of: TOOTOGERUM TRADEGRUM	mended types put voltages of: 5.0 V MBR20035CT 10 V MUR10010CT 20 V MUR10015CT 50 V MUR3015PT		MUR10010CT* MUR10015CT MUR3015PT*		MBR30035CT* MUR10010CT* MUR10015CT* MUR10015CT MUR3040PT		
Recommended Control Ci	ircuits	SHUW	OPPROV	See T	able 4		

*More than one device per leg, matched.

Motor Controls

Power MOSFETs are interesting devices for motor drive applications. The advantages and disadvantages are similar to those discussed for switching power supplies. With motor drives, however, there is more of a distinction. Whereas FETs are not yet a match for bipolar Darlingtons in off-line multiple horsepower drives, they are an excellent choice for fractional horsepower drives and drives that are operated off busses less than 100 V.

Three examples are illustrated. They include a stepping motor drive, a high efficiency H bridge, and a one-transistor PM motor speed control.

Using Power MOSFETs in Stepping Motor Control

Stepping motors are used extensively in electromechanical positioning systems. Applications range from printers to tape drivers, floppy disk drives, numerically controlled machinery and other digitally controlled positioning systems. The task of the stepping motor controller is to drive the rotation generating sequential current flows in the field winding of the motor on command from an external device.

The use of TMOS Power MOSFETs and CMOS logic simplifies the drive circuitry while allowing considerable flexibility of control. This section describes several types of stepping motor control circuits including an 88.0% efficient switching drive. Stepping motor logic sequencing, power requirements and dynamics are briefly examined.

DRIVE TECHNIQUES LOS ent. Inemelganoo at to ebolb

Stepping Motor Characteristics

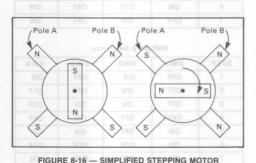
A basic understanding of stepping motors is desirable. A permanent magnet stepping motor consists of a series of permanent magnets distributed radially on a rotor shaft surrounded by electromagnets attached to the stationary housing. Energizing the electromagnets with the proper polarities generates a magnetic field pattern to which the

motor magnets try to align producing torque. A simplified representation of a stepping motor is shown in Figure 8-16. Initially, Poles A and B are both energized with north up, drawing the rotor's south pole to the up position. Reversing the polarity of Pole A draws the rotor 90° clockwise to its final position; this is known as a full step. If pole A had been turned off instead of reversed, the rotor would have rotated only 45° clockwise to line up with the field created by Pole B; this is known as a half step. Stepping motors obtain small angle step increments by using large numbers of poles. Stator pole reversal can be accomplished by reversing the current flow direction in the winding or by using alternate halves of a center-tapped winding.

An external block diagram of a center-tapped stepping motor plus control switches, inductive clamp diodes, resistive current limiting and power supply is shown in Figure 8-17. Pole A, for instance, can be energized to one polarity by turning Switch 1 on and Switch 2 off; the opposite polarity is generated by turning Switch 1 off and Switch 2 on.

It follows that the proper magnetic polarity sequence for stepping can be generated by controlling Switches 1–4. Clamp diodes prevent the voltage across the inductive winding from flying up and destroying the switches as they are turned off. The required switching sequences for full and half step operation are shown in Figure 8-18. Reversing the sequences of Figure 8-18 will reverse the direction of motor rotation.

Rapid stepping requires high di/dt in the motor windings. Since di/dt is a function of supply voltage, a high supply voltage is desirable. The average winding current is limited by the motor manufacturer's specification. As an example, Superior Electric's SLO-SYN model M093-FC07 has a current rating of 3.5 amps/winding with 1.23 Ω / winding resistance and 7.94 mH/winding inductance. The recommended power supply is 24 volts; currents are limited to the maximum rating by a 6.5 Ω , 100 W resistor/ winding. This yields a dc current of about 3.0 A and an L/R time constant of 1.0 ms. Higher supply voltages and



*Colors are for Superior Electric SLO-SYN dc Stepping Motors

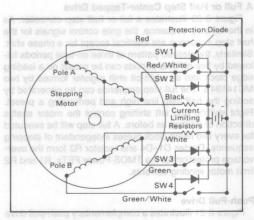


FIGURE 8-17 — SIMPLIFIED STEPPING MOTOR AND CONTROL BLOCK DIAGRAM*

the resulting larger current limiting resistor will decrease L/R and increase the obtainable stepping rate.

Depending on rotor inertia, torque requirements and winding currents, a stepping motor may exhibit oscillatory behavior including vibration, lost steps and/or stalling near self-resonant stepping frequencies. Oscillatory behavior may be lessened or eliminated by adjusting winding currents, by adjusting interial and/or torque loading or by the use of mechanical dampers.

A Full Step Center-Tapped Drive

Figure 8-19 illustrates a full step center-tapped stepping motor controller using one CMOS 4-bit presettable shift register to drive four N-Channel TMOS Power FETs. Examining the full-step sequence of Figure 8-18, shows that the sequences for the various gate signals are the same except for a phase shift. Therefore, the desired control sequence of two on-time periods followed by two off-time periods may be preset into the 4-bit shift register (MC14194) of Figure 8-19. The required phasings are obtained by tapping the appropriate shift register outputs.

Clockwise stepping is obtained by right shifting the MC14194; left shifting yields counterclockwise stepping. Control signals S0 and S1 plus a clock line control stepping. On power-up, the MC14194 requires a preset obtained by setting S0, S1 = 1,1 and supplying a leading edge clock; this puts the logic in a known state. The remainder of the control functions are illustrated in the control table of Figure 8-19; stepping occurs in a leading edge clock. Diodes 1-4 prevent the inductive turn-off spike from avalanching the TMOS Power FETs. Resistor R3 creates a back voltage which halts winding current rapidly on turnoff. R3 is selected to limit the voltage spike to the TMOS S-D voltage rating. TMOS power FETs switch extremely fast, and the turn-on delay of the diodes may not be short enough to prevent S-D avalanche. A small capacitor (0.01 to 0.1 μ F) placed across the motor winding will usually lower dv/dt sufficiently to prevent S-D avalanche. Resistors R1 and R2 limit motor winding currents.

A Full or Half Step Center-Tapped Drive

Figure 8-20 illustrates a full or half step controller. As in the full step sequence, the gate control signals for the half step sequence are identical except for a phase shift. Similarly, the desired pattern of three on-time periods followed by five off-time periods can be preset on a leading edge clock into an eight-bit shift register formed by two MC14194's. The full step sequence can be generated by setting the half step line high and performing a preset. Right shifting and left shifting control the motor shaft's direction of rotation as before. A full step will be executed for every two rising clock pulses independent of stepping sequence. Diodes D1–D4 and resistor R3 form the overvoltage protection for the TMOS Power FETs. R1 and R2 limit motor winding currents.

Push-Pull Drive

Figure 8-21 illustrates a complementary push-pull drive for a non-center tapped stepping motor driven from a 24 volt motor supply and a 15 volt logic supply. One of two winding drive sections plus the complete control logic is shown in Figure 8-21. The total drive consists of four N-Channel and four P-Channel TMOS Power FETs arranged in two push-pull drives per winding (the M093-FC07 center tap leads were floated, inductance/full winding = 31.76 μ H, resistance/full winding = 2.46 Ω and rated current = 2.0 amps/winding).

Phasing signals are obtained with the shift register technique described earlier. The circuit of Figure 8-21 will provide a full or half step sequence as clocked into the two CMOS shift registers during a preset (a full step only controller can be implemented with one 4-bit CMOS shift register). Gate signals for the N-Channel FETs are taken directly from the CMOS registers. Gate signals for the P-Channel FETs are translated and referenced to the motor power rail through Q9-Q10.

Sufficient capacitance across the sources of the bridge FETs must be used to limit P-Channel gate-source voltage transients to below the pass frequency of the collector resistor and the P-Channel gate capacitance. During switching transients, it is possible that both FETs in a given complementary pair could briefly be on at once. This condition could short power to ground through the complementary pair. To avoid exceeding peak drain current rating, the gate-drive on the P-Channel FET is restricted to 10 V.

TMOS Power FETs are constructed with internal source-to-drain diodes. The circuit of Figure 8-21 uses these diodes to shunt turn-off transient currents from the ground plane to the power rail; thus, a given FET is protected from winding turn-off energy by the source-drain diode of its complement. The source-drain diode, how-

Full-Step Sequence

STEP	SW1	SW2	SW3	SW4	
ng ¹ orti i	OFF	ON	OFF	ON	
102 W 01	OFF	ONDE	I ON I	OFF	
3	ON	OFF	ON	OFF	
4	ON	OFF	OFF	ON	
1 OFF		ON	OFF	ON	

Half-Step Sequence

STEP	SW1	SW2	SW3	SW4	
1/	OFF	ON	OFF	ON	
2 2	OFF //	ON OFF		OFF	
3	OFF	ON	ON	OFF	
4	OFF	OFF	ON	OFF	
5	ON	OFF	ON	OFF	
6	ON	OFF	OFF	OFF	
7 HOTO	ON	OFF	OFF	ON	
8	OFF OFF		OFF	ON	
1	OFF ON		OFF	ON	

FIGURE 8-18 — STEPPING SEQUENCES**

^{**}Clockwise Rotation as Viewed from the Nameplate End of the Motor

ever, requires about 300 ns of turn-on time. A 0.1 μ F capacitor is placed across each winding so that the windings dv/dt is low enough to allow for diode turn-on without avalanching the FETs. Winding currents are limited by the 9.0 ohm 5.0 watt resistors.

Switched Current Limiting and almora notice?

The circuit of Figure 8-21 uses resistive current limiting. With 2.0 amps flowing in each winding, 4.0 amps will be drawn off of the 24 volt supply yielding 96 watts of draw with only 25% of that power being delivered to the motor. Some form of switched current limiting is clearly desirable. Figure 8-22 illustrates a simple switching scheme.

Starting with zero current flow, let the desired current flow be left to right through the motor winding. Let the referenced voltage V_{ref} be 0.2 volts. Assuming $R_{\text{H}} > > R_{\text{ref}}$, the positive comparator inputs will be approximately 0.2 volts. With no current flow, the sense resistors will have no voltage across them and the comparators will have high outputs; this enables the C1 and C2 inputs to drive the P-Channel Power FETs. The proper C1, C2 input

for left to right current flow is 1,0. This turns the upper left P-Channel and the lower right N-Channel on placing the full power supply across the motor winding. Current I1 increases with di/dt = V/L. When I1 increases to 2.0 amps, the voltage across the lower right 0.1 sensing resistor will be 0.2 volts, and the lower right comparator will go low after a short filter delay shutting off the upper left P-Channel FET. The current through the motor winding begins to decay around the I2 current path.

When the comparator went low, it shifted its positive input reference down by about 70 mV. 12 decays until the voltage across the 0.1 sense resistor falls below the hysteresis determined level; at that point, the comparator will go high turning on the upper left P-Channel FET and recharging the winding current along the 11 current path. The winding current within the C1, C2 control envelope increases to the reference level and oscillates around that level at a value set by RH, R_{ref} and the logic supply voltage. The frequency of oscillation is set by V/L, the hysteresis value and the current path resistances.

The circuit of Figure 8-22 places a negative voltage on

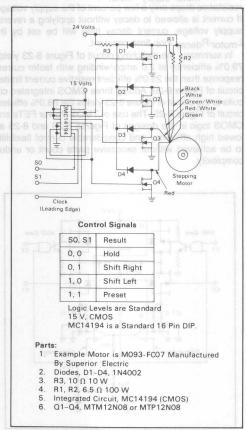


FIGURE 8-19 — CENTER-TAPPED S-8 ERUDIA

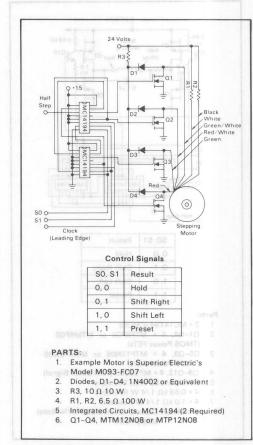


FIGURE 8-20 — HALF- OR FULL-STEP DRIVE

the negative input terminal of the comparators during the 12 current path. This is not detrimental to the comparator provided that the terminal current doesn't exceed a few milliamps.

The complete logic circuit plus one of two required winding drive sections for a push-pull stepping motor with switched current limiting is shown in Figure 8-23. Figure 8-24 is the corresponding parts list for the complete circuit. The circuit of Figure 8-23 is limited to 8.0 amps continuous with a motor power supply voltage of about 70 volts by the specified P-Channel TMOS Power FETs. Thus, the controller can handle up to 560 watts delivered to each winding. Changes in RH, R_{ref} and the sensing resistor may be desirable for motors other than the example motor. For low inductance motors driven from high voltage supplies with low levels of hysteresis, faster components in the switched feedback loop may be required.

Utilizing Synchronous Rectification and application

The circuit of Figure 8-23 required 26.4 watts to maintain 2.0 amps/winding with 78.8% of the drawn power

MC14194 MC14194 15 V O-SO. S1 Result 0,0 Hold 0.1 Shift Right 1.0 Shift Left 1, 1 Preset Parts: 1. 2 × MC14194 (CMOS) Q1-Q4, 4 × MTP8P08 or MTM8P08 (TMOS Power FETs) Q5-Q8, 4 × MTP12N08 or MTM12N08 (TMOS Power FETs) Q9-Q12, 4 × MPS8099 (NPN Small Signal) 5. 2 × 9 Ohm 50 Watt Resistors 6. 4 × 0.68 k0 1/4 W Resistors 7. $4 \times 1.0 \text{ k}\Omega$ 1/4 W Resistors Example Motor: Superior Electric SLO-SYN Model M093-F007

FIGURE 8-21 — HALF- OR FULL-STEP RESISTIVE CURRENT LIMITED DRIVE FOR STEPPING MOTORS WITHOUT CENTER-TAP

delivered to the M093-FC07. Calculations indicated that greater than 50.0% of the control circuit power consumption was due to the S-D diode drop during the I2 current loop (Figure 8-22). This drop could be lowered by operating the lower N-Channel Power FETs as synchronous rectifiers. The additional logic required for synchronous rectification amounts to three CMOS integrated circuits. A complete logic circuit plus one of the two required winding drive sections is shown in Figure 8-25. Essentially, the lower N-Channel is turned on when the upper complementary P-Channel is turned off by the comparator or when the N-Channel control signal is high. The circuit of Figure 8-25 yielded 88.4% efficiency at 2.0 amps/winding.

Further Possibilities and algorith trips of fiel ad woll

Shaping of the applied current waveform is often desirable. If a large stepping torque followed by a low holding torque is desired, the required current waveform can be applied to the positive comparator input. Within the comparator hysteresis and the circuit's current response speed, the current in the motor will follow the comparator reference. The di/dt circuit response is limited by approximately V_{motor} supply/L_{motor}, provided that the series resistance drops only a few percent of the supply voltage. If current is allowed to decay without applying a reverse supply voltage, current decay time will be set by the L_{motor}/R_{decay} loop time constant.

In summary, the switching circuit of Figure 8-23 yields 79.0% efficiency at 2.0 amps/winding with faster current response than the 25.0% efficient resistive current limited circuit of Figure 8-20. Adding three CMOS integrated circuits to the circuit of Figure 8-23 yields the 88.0% efficient circuit of Figure 8-25. The use of TMOS Power FETs and CMOS logic in the designs of Figures 8-23 and 8-25 allowed high efficiency and considerable control flexibility to be achieved without excessive parts count or undue complexity.

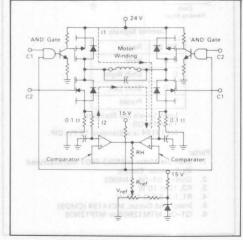


FIGURE 8-22 — COMPARATOR SWITCHED CURRENT LIMITING



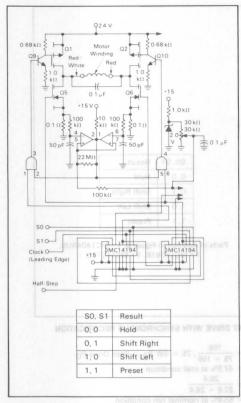


FIGURE 8-23 — HALF- OR FULL-STEP SWITCHED CURRENT DRIVE FOR STEPPING MOTORS WITHOUT CENTER-TAP

H Bridge Performance Comparisons

Power MOSFETs are excellent candidates for low voltage H Bridges. In this example, MOSFETs are compared with two other popular alternatives, bipolar discretes and bipolar Darlingtons. Circuits were designed for all three types of output power devices. Each circuit design is optimized for the output device used.

General "H" Switch Design Considerations:

- . P.M. DC Motor, 2.0 A run, 15 A stall/start.
- 12 V protected bus, 32 V max peak, 14 V nominal.
- "H" switch input, 2.0 mA max sink requirement.
- Discrete driver stages (for comparison of designs).
- Maximum ambient temperature of 100°C, maximum junction temperature = 150°C.
- Off the shelf type output power devices using maximum data sheet limits to calculate drive requirements and forward "on" voltage levels. The power output devices were chosen such that die sizes for the three types are approximately equal.

Integrated Circuits

- 1. 2 × MC14194B, CMOS 4-Bit Shift Register
- 2. 1 × MC14081B, CMOS Quad "AND" Gate
- 3. 1 × LM339N, Quad Comparator

TMOS Power FETs

- 1. Q1-Q4, 4 × MTP8P08 or MTM8P08, P-Channel Power FET
- Q5–Q8, 4× MTP12N08 or MTM12N08, N-Channel Power FET

Transisto

1. Q9-Q12, 4 × MPS8099, NPN Small Signal Transistors

Resistors

- 1. 4 × 0.1 Ω 2.0 W
- 2. 4 × 680 Ω 1/4 W
- 3. $5 \times 1.0 \text{ k}\Omega \text{ } 1/4 \text{ W}$ 4. $2 \times 10 \text{ k}\Omega \text{ } 1/4 \text{ W}$
- 5. $1 \times 30 \text{ k}\Omega 1/4 \text{ W}$
- 6. 1 × 30 kΩ Adjustable, 1/4 W
- 7 6 × 100 kΩ 1/4 W
- 8. 2 × 22 MΩ 1/8 W

Zener Diode

1. 1 × IN, 2 V Reference

Capacitors

- 1. 3 × 0.1 μF 100 V
- 2. 4 × 50 pF 50 V

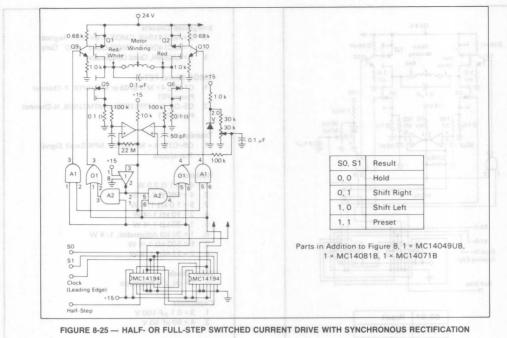
FIGURE 8-24 — PARTS LIST FOR CIRCUIT OF FIGURE 8-23

Discrete Bipolar "H" Switch

TIP35 and TIP36 power transistors were selected for their low cost and high current capacity. The high current-gain specification for these units results in base drive requirement of 1.5 amperes to switch a 15-ampere load current. It may be that base drive can be reduced by 30 percent if the units are screened for high-current hfe, but for this design comparison, only "off-the-shelf" standard devices with the regular data-sheet specifications are under consideration.

The bipolar "H" switch design requires medium size driver transistors and large-wattage voltage-dropping resistors in the base-drive circuit. A buffer stage is also required. The control lines are shown tied to a SPDT center off switch. In an actual circuit, this switch would be a logic array or a microcontroller output network. A protective counter-EMF voltage clamp is provided by the back-to-back Zener rectifiers. The Darlington and TMOS units have built-in clamp diodes and for many applications would not require the zeners. Capacitor and resistor snubbing networks may be required with all three types output devices

As indicated in the performance table, the bipolar design is not very practical because of the large base drive requirement. Of the three power devices, it is the least efficient by a wide margin. In most situations, FETs or Darlingtons are a better choice.



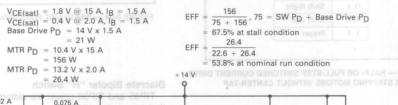


FIGURE 8-23 - HALF- OR FULL-STEP SWITCHED CURRENT DRIVY 1+ 0.002 A 0.075 A _____2.0 k ≥ **≥** 180 Ω **\$** 2.0 k 180 Ω TIP36 TIP36 6.2 k 8.0 Ω 20 W 160 Ω ≶ **₹**160 Ω 2.0 W 2.0 W MPSU01A MPSU01A ₹10 k | 0 .20 10 k € MOTOR 15 A Pk 2.0 A NOM. e PM. DC TIP35 Ferrite requirement. Of the three power devices, it is the least voltage levels 2The power

FIGURE 8-26 — "H" SWITCH BIPOLAR CONTROL CIRCUIT

Discrete Darlington "H" Switch

Motorola MJ4030 and MJ4033 power TO-204 (TO-3) Darlingtons were chosen for the Darlington version of the H bridge. As the chart shows, the drive-power requirements are substantially reduced from the bipolar power design. The tradeoff is that the forward "on" voltage is raised to such a high level that this particular motor will no longer be within its terminal voltage specification during stall or start-up. Also, the Darlington's dissipation will require a larger heat sink than the bipolar design. The Darlington does provide internal clamp diodes.

The Darlington "H" switch design works best in highvoltage, low-current load control circuits where the Darlington's high saturation power loss is not significant.

Power TMOS "H" Switch

An MTP25N05 Power FET was chosen for this design. Since the die size falls somewhat shy of the bipolar and Darlington device die sizes, an adjustment was made in the conduction loss calculation. Actual V_{DS}(on) measurements were scaled according to the area ratio in order to arrive at the numbers presented here. As the comparison chart reveals, the TMOS design is clearly superior to the bipolar and Darlington designs. Its only technical drawback is the 34 volt bias supply requirement. This supply only has to source approximately 200 microam-

peres for this dc control, and can be derived from a single voltage pump-up circuit using TMOS gates and voltage doubling networks.

Test Measurement Calculations

The following equations were used to determine the circuit performance values for this example.

 MOTOR POWER CONSUMPTION — The applied voltage across the motor load-terminals multiplied times the normal motor current.

$$PD(MTR) = 1.0 \times (V_{BATT} - 2.0 \times V_{F(on)})$$

 $I = 2.0$ AMPS RUN MODE $I = 15$ AMPS STALL MODE

VF(on) = VCE(sat) or VDS per data sheet

- 2. OUTPUT DEVICE POWER DISSIPATION $P_{D(sw)} = (I \times V_{F(on)}) \times 2.0$
- 3. "H" SWITCH CONTROL EFFICIENCY

$$\begin{aligned} &\mathsf{EFF} = \frac{\mathsf{Power\ Out}}{\mathsf{Power\ In}} \\ &\mathsf{Power\ Out} = \mathsf{PD}(\mathsf{MTR}) \\ &\mathsf{Power\ In} = \mathsf{PD}(\mathsf{sw}) + \mathsf{PD}(\mathsf{MTR}) \end{aligned}$$

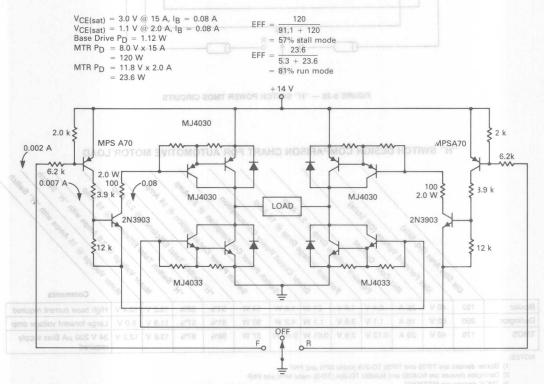


FIGURE 8-27 — "H" SWITCH DARLINGTON CIRCUIT

27.5 EFF = $\frac{1}{0.48 + 27.5}$

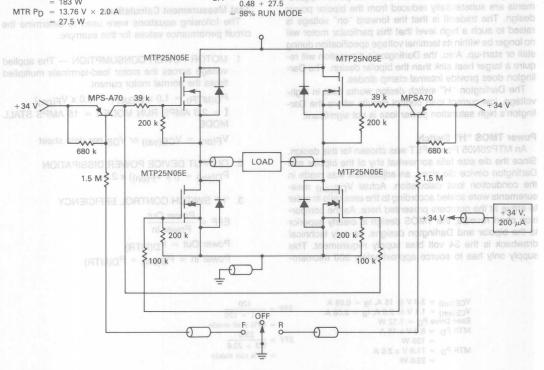


FIGURE 8-28 — "H" SWITCH POWER TMOS CIRCUITS

"H" SWITCH DESIGN COMPARISON CHART FOR AUTOMOTIVE MOTOR LOAD 15 AMP Forked July & Brown Land Shield Chellin Power Consumption Moduly of Market & 2.0 knows with it Heat Formed Jorges Och States Swed Powel Consumption .H. Switch Told Huberton ... the switch Took the broken Die Site Bed Sch. Comments Bipolar 192 40 V 25 A 0.4 V 1.8 V 21 W 1.6 W 54 W 54% 68% 13.2 V 10.4 V High base current required 11.8 V 60 V 1.1 V 3.0 V 1.1 W 4.2 W 90 W 81% 8.0 V Large forward voltage drop Darlington 200 16 A 57% **TMOS** 176 40 V 20 A 0.12 V 0.9 V 0.01 W 0.48 W 27 W 98% 87% 13.8 V 12.2 V 34 V 200 μA Bias supply

NOTES

1-8

- 1) Bipolar devices are TIP35 and TIP36 TO-218 plastic NPN and PNP
- 2) Darlington devices are MJ4030 and MJ4033 TO-204 (TO-3) metal NPN and PNP.
- 3) TMOS devices are MTP25N05.
- 4) Figures shown above are the worst case data sheet condition for the parameter calculated.

Bidirectional Control of Fractional Horsepower Motors

By using power MOSFETs in Figure 8-29b's circuit, fractional-horsepower motors can be driven bidirectionally with only a small percentage of the base-drive power that bipolars require. Moreover, by sensing the motor's back EMF and delaying drive-voltage reversal, the circuit reduces the peak currents encountered during motor reversal. This feature allows the use of lower current MOSFETs than an instantaneous-reversal method would dictate.

A basic H switch, Figure 8-29a reverses the motor's supply voltage for bidirectional control. In Figure 8-29b's circuit, two pairs of N-channel MOSFETs serve as the CW (clockwise) and CCW (counterclockwise) switches. A flyback-type dc/dc inverter, composed of a CMOS hex inverter and a small signal MOSFET, drives the FET switches. The 3-inverter oscillator operates at 240 kHz; the three remaining inverter's average output tracks the power-supply input, ensuring adequate gate-bias voltage even for input-supply voltages as low as 6.0 V.

The Darlington transistors sense the motor's counter EMF (via the 20 V snubber zeners that become forward biased when the motor's back EMF appears) and shunt the drive-reversal signal to ground until the back EMF decays. The transistors will hold the gate-drive line low until the counter EMF drops below the base-to-emitter threshold voltage. This action causes the circuit to wait until the motor nearly stops rotating before applying reverse voltage. If faster response times are needed, the Darlingtons can be eliminated while connecting the 1.0 $\mathrm{M}\Omega$ base resistors to ground — this change, however, would necessitate higher current MOSFETs because of the large peak-reversal currents that would ensue.

Figure 8-30 shows the dramatic difference in the peak currents that occur with and without the back-EMF-sensing feature. With the sensing circuit disabled (a), the currents exceed 50 A; the resulting MOSFET dissipation is approximately 140 W. Enabling the circuit (b) reduces the currents to approximately 30 A and the MOSFETs' dissipation to about 14 W. A 16 V zener diode limits the input voltage to the flyback inverter in case the supply

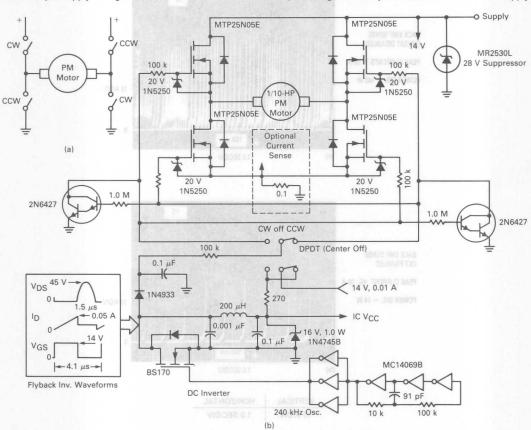


FIGURE 8-29 — DRIVE FRACTIONAL-HORSEPOWER MOTORS EFFICIENTLY WITH THIS POWER-MOSFET H-BRIDGE CIRCUIT. IT DISSIPATES MUCH LESS POWER THAN A BIPOLAR-TRANSISTOR

DRIVER — MOREOVER, IT ALLOWS THE USE OF LOW-CURRENT MOSFETS BY DELAYING REVERSAL VOLTAGE UNTIL THE MOTOR COASTS TO A STOP.

rises higher than 16 V; the transient suppressor protects the MOSFETs from supply spikes greater than 28 V.

In this design, the MOSFETs require heat sinking to keep their junction temperatures less than 150°C in worst-case conditions (that could occur, for example, with a 16 V supply, 100°C ambient temperature and a stalled motor). As an option, a current-sensing circuit can be added to gate-off the power FETs after detecting a stall condition.

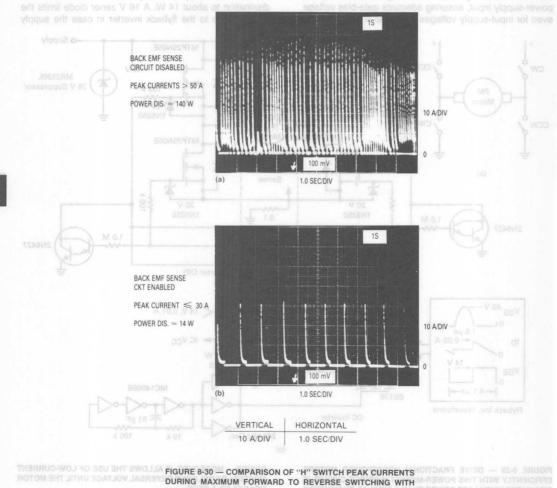
PWM Motor Speed Control

FETs can be used to considerable advantage for simplifying permanent-magnet motor speed control. The circuit shown in Figure 8-31 provides efficient pulse-width

modulated control with a minimum number of components. The key feature is direct drive of the power FET from a CMOS control IC. The result is a control system with minimized parts count.

The control system is based upon the MC14528B dual monostable multivibrator. One-half of the monostable is connected in an astable mode, producing a pulse oscillator. The remaining half is then used as a one-shot, with its adjustable pulse-width determining the duty cycle and, therefore, motor speed.

In addition to its simplicity, the circuit of Figure 8-31 is notable for its low standby power drain. The combination CMOS control and TMOS power gives a very low quiescent current drain that is desirable in battery operated applications.



MOTOROLA TMOS POWER MOSFET DATA

MANUAL TOGGLE SWITCH

Horizontal Deflection Circuits

Power MOSFETs can be a good alternative to bipolars in high resolution CRT sweep circuits. The most obvious advantage is simplicity. However, MOSFET horizontal outputs also offer significant benefits in terms of increased reliability and faster switching times.

Drive simplification with the MOSFET is even more significant than in the preceding switching power supply examples. In most cases, a base-drive transformer is eliminated, as well as di/dt wave shaping networks.

The reliability issue is a little more complex, and relates to differences in SOA characteristics. It is normal design practice to exceed bipolar collector-emitter breakdown ratings during the retrace pulse transition. This is permissible if the base-emitter voltage is held negative during the retrace period. If, however, a positive noise pulse occurs during the retrace period, the bipolar base-emitter junction can become forward biased when collector-emitter voltage is greater than VCEO(sus). The bipolar's safe operating area is then violated, creating a substantial risk of failure. MOSFETs, on the other hand, will handle this type of stress quite readily, since their FBSOA capability extends beyond peak retrace voltage. Therefore, increased reliability with the MOSFET horizontal output is directly related to the probability of noise occurring in the drive circuitry.

Speed is also an important issue. At a 30 kHz scan rate, $1.0~\mu s$ of bipolar storage-time delay represents 3% of the horizontal line period, or a loss of 30 lines of data in a field of 1024 lines. In addition, bipolar storage time is not a fixed constant, but changes from device to device and with temperature. A horizontal phase locked loop can

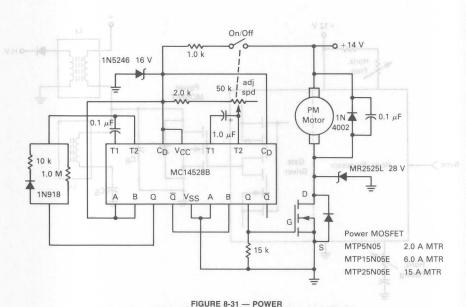
be added to compensate for the storage-time delays in the horizontal output stage. The active video data time may also be cut back, accordingly, to allow for internal horizontal timing delay.

Based upon these considerations, effective use of the bipolar transistor at high scan frequencies requires a complex base drive circuit, custom selection of the bipolar device for minimum storage-time variation, and an accurate phase locked loop to compensate for saturation time delays. Power MOSFETs, on the other hand, can be driven from a CMOS IC, do not require critical parameter screening, exhibit minimal turn-off delay, and do not require a phase locked loop for correcting device-induced timing errors.

Design Example

The power MOSFET, until recently, could not handle much current at voltages above 500 V. Recent technology developments have pushed this limit up to the 1000 V range with increased current ratings. Therefore, a power MOSFET can now be selected for computer CRT display systems with power supply requirements ranging from 12 V to 75 V.

The standard horizontal raster scan system is used in this design. That is, the horizontal yoke and flyback transformer are both switched by one output device. It should be pointed out that the power MOSFET has been switched up to 120 kHz scan rates, but due to other device constraints, the CRT anode high voltage network's performance is very marginal at this high frequency rate. Even a scan frequency of 30 kHz is pushing the limits of the high-voltage rectifier and associated components.



MOTOROLA TMOS POWER MOSFET DATA

METEVE TO MOSFET MOTOR SPEED CONTROL CIRCUIT

The design concept is shown in the block diagram of Figure 8-32. The horizontal drive signal can be supplied by a free running synchronous clocked oscillator or by external computer logic. The safest method is to use a free running synchronous oscillator to insure the horizontal frequency is held within safe limits. There are several horizontal processor linear integrated circuits containing a phase detector, oscillator and predriver available. A partial list includes SGS TDA1180 and Motorola MC1391. None of these devices are presently designed to drive a MOSFET power unit directly; so some type of an interface or buffer circuit is required. Three power MOSFET drive circuits are shown in Figure 8-33. These circuits perform adequately in the horizontal system described here.

Circuit Description

The design presented in Figure 8-34 eliminates the driver transformer, driver transistor, and associated passive components that would normally be found in a bipolar design. A MLM311 comparator is used to invert and levelshift the incoming positive going synchronous pulse. The comparator output is ac coupled to the MC1391 horizontal processor which consists of a phase comparator and voltage controlled oscillator with adjustable duty cycle. The phase comparator of the MC1391 is connected to the incoming conditioned horizontal synchronous pulse and the output of the MC1391's internal oscillator. An error voltage is applied to the oscillator timing control voltage to lock in the external synchronous pulse and the oscillator. The duty cycle of the MC1391 oscillator output is set to provide a 63% "ON" time to the power MOSFET gate.

Essentially, the prime requirement for driving the power MOSFET for this horizontal scan output design is to insure sufficient gate on-voltage and low enough impedance for a fast turn-off transition. Since the power MOSFET has a high gate input impedance, the gate voltage requirement is easily met, with little wasted power. The off transition requires that the power MOSFET's internal 1000 pF gate capacitance be discharged very quickly. This is accomplished by using a single hex inverter IC, with all the gates wired in parallel. As mentioned before, other devices can be used to drive the MOSFET. The CMOS inverter was chosen to show that CMOS technology is sufficient to drive the MOSFET.

The system described above provides excellent performance. The gate-drive voltage of the power MOSFET was purposely pulsed during the peak retrace drain voltage pulse to simulate destructive transients due to anomalies such as arcing.

It was found that a controlled drain-to-source current occurred, with no catastrophic failures, as long as the total power dissipation was held within the limits of the power FET's safe operating area ratings. Figure 8-34 shows the waveforms associated with the retrace pulse test. Since the MOSFET is a high input impedance device, it is important to insure the gate of the power MOSFET is at a low impedance during the retrace period. The gate should not be driven negative, to minimize the possibility of voltage spikes causing gate avalanche. The gate cannot withstand an avalanche condition of any measurable current intensity and survive. Since the power MOSFET device selected for this design exhibits at least a 2.0 volt threshold, a negative gate-drive is not important.

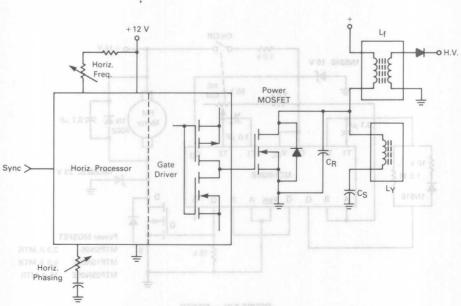


FIGURE 8-32 — POWER MOSFET HORIZONTAL OUTPUT SYSTEM

Figure 8-35 shows a comparison of the key horizontal output circuit waveform patterns between a bipolar and MOSFET design. Note the large reduction in the horizontal output drive power and lack of storage time in the MOSFET design.

Fast High-Current MOSFET Driver

A totem-pole MOSFET driver circuit shines when highcurrent, fast-transition pulses must be generated from lowvoltage sources. Its MOSFETs sidestep a number of problems that their bipolar counterparts present in the same circuit.

High-speed transistors and high-current transistors intended for PWM applications have created a need for high-current, fast-drive circuits. Transistors that demand 20 to 35 A of reverse base current for rapid turn-off and can be driven by as little as 5.0 V of off-voltage are a common requirement. Bipolar devices switch in nanoseconds but are limited to 5.0 to 10 A when driven from low-voltage collector supplies. With higher current capability,

such transistors require power transistors as drivers and, when driven by a low-voltage source, sacrifice switching speed

Yet a third possible solution — paralleling fast, lowcurrent transistors — presents two problems: current sharing and physical layout.

The MOSFET driver circuit in Figure 8-36 uses two N-channel devices with positive and negative polarities. Fast transitions are possible, even when a low-voltage source is used. The circuit returns to 0 V between pulses, an important feature when driving high-power Darlington transistors with base-bias resistors and speed-up diodes. In this case, excessive heating would otherwise occur during the off-time interval.

Small size, simple configuration, and minimum component count join with ease of operation to make this driver circuit very useful for applications in variable-frequency switched-mode power supplies, and inverters.

In operation, a single-polarity, negative-going pulse from a pulse generator is applied to the input. The pulse, whose width can vary anywhere from 5.0 μ s to 3.0 ms, turns on PNP predriver transistors Q2 for the positive-polarity output.

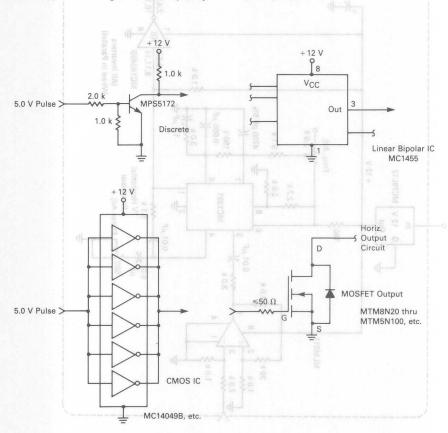
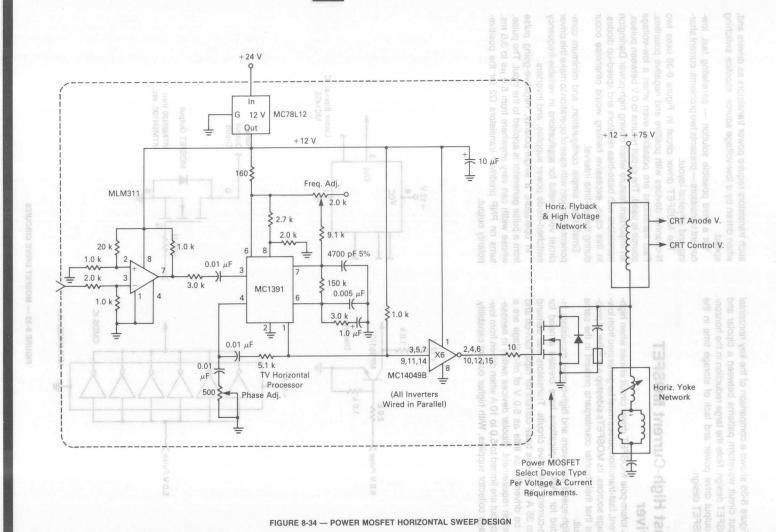
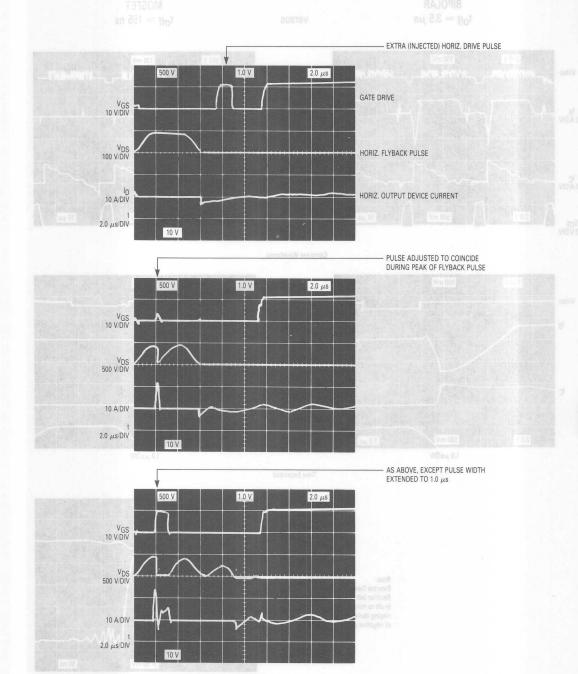


FIGURE 8-33 — MOSFET DRIVE CIRCUITS







2M904 FIGURE 8-35 — HORIZONTAL DEFLECTION RETRACE PULSE TEST WAVEFORMS

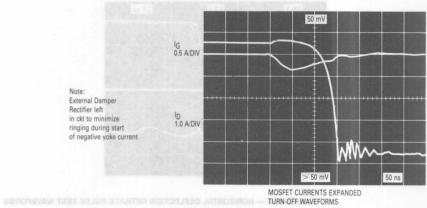


FIGURE 8-36 — BIPOLAR versus MOSFET

Resistor R_b, inserted in series with the drain lead of Q2 and the supply, sets the positive drive level. The resistor should be selected for a drive of 10 V or greater as well as the amount of desired current.

After the required on-time of the positive output current, the pulse generator returns to zero. Then, the RC differentiator network applies a positive voltage to the gate of MOSFET Q3, which supplies the negative polarity output. The values shown can be changed to lengthen the du-

ration of the negative drive. The negative voltage remains for about 10 μs and then returns to zero, completing a single cycle.

The circuit can be used with FETs by replacing R_b with a short and the positive and negative voltages applied to the devices' gates. For controlled gate-impedance drive, resistors can be inserted in series with the gates. Similarly, a resistor added in series with the base of the bipolar transistor results in controlled base-current drive.

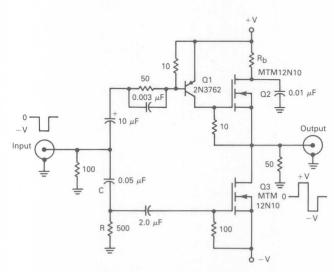


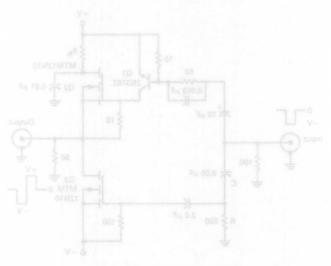
FIGURE 8-37 — MOSFET DRIVER CIRCUIT

Resistor R_D, inserted in series with the drain lead of Q2 and the supply, sets the positive drive level. The resistor should be selected for a drive of 10 V or greater as well as the amount of desired current.

After the required on-time of the positive output current, the pulse generator returns to zero. Then, the RC differentiator network applies a positive voltage to the gate of MOSFET Q3, which supplies the negative polarity output. The values shown can be changed to lengthen the du-

ration of the negative drive. The negative voilage remains for about 10 µs and then returns to zero, completing a single cycle.

The circuit can be used with FETs by replacing B_b with a short and the positive and negative voltages applied to the devices' gates. For controlled gate-impedance drive, resistors can be inserted in series with the gates. Similarly, a resistor added in series with the base of the bipolar ransistor results in controlled base-current drive.



PIGURE 6-37 -- MOSFET DRIVER CIRCUIT

Chapter 9: Spin-Off Technologies of TMOS

SENSEFETS THE STATE OF STATE O

Some of the more exciting developments in discrete power semiconductors are arising from power IC concepts. Integrated circuit design engineers, with fine geometries and ratioing techniques as standard tools of the trade, are applying these concepts to discrete power semi-conductor design with great success. One notable example is SENSEFETs.

By splitting drain current into power and sense components, these new devices feature a "lossless" current sensing technique for discrete designs. The intention of this chapter is to explore the concept, device characteristics, and the state-of-the-art performance that SENSE-FETs can provide.

Lossless Current Sensing Manager V alsow

"Lossless" current sensing is a technique that arises from integrated circuit ratioing concepts. It is based upon the tendency of individual source cells in a monolithic power MOSFET to match. Therefore, if one or two out of several thousand cells are returned to a separate sense or mirror connection, a ratio between load current and sense current is developed.

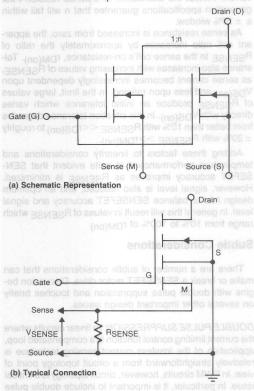
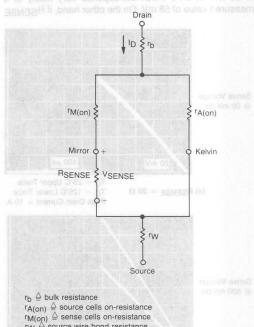


FIGURE 9-1 — FUNCTIONAL REPRESENTATION

This concept is illustrated in Figure 9-1a, where sense current and load current are related by the ratio 1:n, provided that the sense terminal and the source terminal are returned to the same potential. When a sense resistor is placed between these two terminals, the ratio is disturbed somewhat, but remains quite predictable for low values of RSENSE. A shorthand symbol for the SENSEFET, and a connection for RSENSE are shown in Figure 9-1b.

The circuit model and equations shown in Figure 9-2 describe SENSEFET behavior during fully switched on operation. From the equations, one can easily calculate the sense resistance required for a given sense voltage. Although any value of sense resistance can be used, two considerations are worth noting: (1) as RSENSE increases, VSENSE asymptotically approaches a maximum voltage magnitude equal to Ip *rA(on), and (2) sense voltage accuracy over the operating temperature range severely degrades with increasing sense resistance. From a practical point of view, relatively good accuracy is maintained when RSENSE < rM(on)/2.



rw ≜ source wire bond resistance
RSENSE ≜ external sense resistance

(1) $r_{M(on)} = n r_{A(on)}$ where $n \triangleq geometric current mirror ratio$

(2) VSENSE = ID · rA(on) · RSENSE / [RSENSE + rM(on)] (3) RSENSE = VSENSE · rM(on) / [ID · rA(on) - VSENSE]

(4) $ID = VSENSE \cdot (RSENSE + rM(on)) / rA(on) \cdot RSENSE$

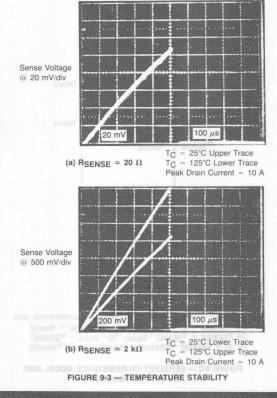
FIGURE 9-2 — SENSEFET ON-RESISTANCE MODEL AND ASSOCIATED EQUATIONS

reduced with respect to current in power section cells. Therefore, there is a debiasing effect which alters the 1:n sense ratio as a function of RSENSE. Similar to switch-mode operation, moderate values of sense resistance alter the sense ratio in a predictable way, resulting in a useful measurement.

Accuracy and not lodiny a branche A BENESH to

Accuracy for a current sensing technique can be looked at in a number of different ways. Of most concern in switching applications are the linearity, temperature coefficient, and unit to unit variations that occur when the power device is fully switched on. These parameters are illustrated for the MTP10N10M, a 10 A/100 V SENSEFET.

LINEARITY: At any given drain current, a corresponding sense voltage can be chosen by scaling RSENSE. As drain current, ID, changes from this baseline, linearity measures the accuracy with which the VSENSE/ID ratio holds at other currents. For example, at 10 A a 20 \(\Omega\$ sense resistor typically sets VSENSE at 116 mV for the MTP10N10M. A linear response would suggest a reading of 58 mV at 5 A, which corresponds very nicely to a measured value of 58 mV. On the other hand, if RSENSE



surement with lower values of RSENSE.

TEMPERATURE COEFFICIENT: A graphic representation of temperature stability is shown in Figure 9-3. For this figure drain current is ramped from 0 to 10 A. The photos are double exposures with one shot taken at 25°C and the other at 125°C. As with linearity, the best results are obtained with a sense resistor that is small with respect to the sense cell's on resistance, $r_{DM(on)}$. With 20 Ω , temperature tracking is essentially within a trace width, and the two values diverge by only 4% at 10 A. As RSFNSF is increased, temperature coefficient becomes less dependent upon matching and more a function of the power device's on voltage. In the limit where RSFNSF is very large, sense voltage approximates the power device's V_{DS(on)} and tracks its temperature coefficient. This tendency is guite evident in Figure 9-3b, where at RSFNSF = 2 k the two measurements diverge by 45% for a 100°C change in temperature.

TOLERANCE: The parameter that describes tolerance for a SENSEFET is the cell ratio, n. It is defined for RSENSE = 0 and measures the ratio of source current to sense current without the attenuation of a sense resistor. First generation specifications guarantee that n will fall within a $\pm 10\%$ window.

As sense resistance is increased from zero, the apparent cell ratio increases by approximately the ratio of RSENSE to the sense cell's on-resistance, $r_{DM(on)}$. Tolerance also increases with increasing values of RSENSE, as sense current becomes increasingly dependent upon $V_{DS(on)}$ and less upon ratioing. In the limit, large values of RSENSE produce an initial tolerance which varies directly with $V_{DS(on)}$. In this situation tolerance degrades from better than 10% with RSENSE $<< r_{DS(on)}$ to roughly $\pm\,20\%$ with RSENSE $>> r_{DM(on)}$.

Adding these factors to linearity considerations and temperature performance it is quite evident that SEN-SEFET accuracy improves as RSENSE is minimized. However, signal level is also reduced, and an optimum design has to balance SENSEFET accuracy and signal level. In general this will result in values of RSENSE which range from 10% to 100% of rDM(on)

Subtle Considerations

There are a number of subtle considerations that can make or break a SENSEFET motor drive. Discussion begins with double pulse suppression and touches briefly on several other important design issues.

DOUBLE PULSE SUPPRESSION: In linear circuits where the current limiting control function is a compensated loop, application of the lossless current sensing technique is relatively straightforward from a circuit topology point of view. In PWM circuits, however, circuit topology is a critical issue. In particular, it is important to include double pulse suppression in the PWM drive loop. In other words, once

the current limit trip point is reached, it is important to disable the power device for the remainder of the clock interval

If the current limit loop is allowed to oscillate at its natural frequency, the primary objective of protecting the power transistor can be jeopardized. Without double pulse suppression, the loop will often oscillate faster than gate drive will switch the power device with reasonable switching losses. When this happens it is very easy for power dissipation to rapidly exceed acceptable levels and for an otherwise foolproof protection scheme to fail from over dissipation.

DIODE CLEARING: In bi-directional and brushless motor drives where freewheeling diodes are commutated, diode recovery currents can be an issue. For example, suppose that a P-channel MOSFET in the top half of a bridge has motor current flowing through its freewheeling diode. If a SENSEFET on the bottom half of this leg is then turned on rapidly there will be a substantial current spike. This spike consists of the motor current plus the freewheeling diode's reverse recovery current, and can easily be three or four times maximum run current.

SENSEFETs are high-speed devices that easily transmit a corresponding peak sense voltage to the drive's current limiting circuitry. Therefore, it may be necessary to keep switching peaks from inadvertently tripping current limit circuitry.

There are several relatively straightforward methods for doing this. In SMARTMOS circuits, for example, a low value of RSENSE is generally used in combination with a sense amplifier. The sense amplifier does a good job responding to the PWM repetition rate but, due to its rolloff characteristics, largely ignores switching spikes. Similarly, a low pass filter between RSENSE and the drive's current limit input will do the same job. Approaching the problem from a different angle, digital techniques can also be used to blank the current limit loop during reverse recovery time

COMMUTATING ERROR: If a PWM signal is instead applied to the upper half of the same bridge, a more difficult situation is created. In this case, suppose that motor current is flowing through the SENSEFET's freewheeling diode when the upper switch turns on rapidly. This time it is the SENSEFET's drain source diode that gets cleared, and this clearing process produces a high level error signal. In other words, during reverse recovery time, the SENSEFET's output can easily exceed its steady state maximum value by more than an order of magnitude. This voltage is in the right direction to trip current limit circuitry, and is large enough to be difficult to filter out. For this reason, circuit topologies which avoid pulse width modulating both upper and lower halves of the bridge are usually preferred. Where this constraint is not desirable, digital blanking of current limit circuitry during reverse recovery time can be used.

SENSE AMP SATURATION: When a sense amplifier is used to boost a low level SENSEFET signal for further processing it is necessary to pay close attention to the amplifier's saturation voltage specification. For example, in CMOS systems the MC14574 quad comparator does a good job of working directly with SENSEFET signals. If

instead the companion MC14573 operational amplifier is chosen to boost signal level, its output voltage range can pose a serious limitation. With the operational amplifier, there will be a dead zone that corresponds to its specified 1.05 volt minimum output voltage. In this dead zone the SENSEFET's output voltage does not affect the amplified output voltage until the latter exceeds 1.05 volts.

For this reason, minimum output voltage is a key specification for SENSEFET interfacing, assuming that single supply operation is desired. The MC34074 is an excellent choice in this regard, with a typical minimum output voltage of 100 mV, and specified maximum of 200 mV.

GROUND LOOPS: Lossless current sensing is a technique that looks for 100 mV signals in a loop that may carry tens or even hundreds of amps. The potential for ground loop error in this kind of a situation is a first order design consideration. In particular, current flowing from the SENSEFET's source into a non-zero ground impedance can easily create voltage drops which are significant with respect to a 100 mV measurement.

For this reason, a Kelvin source connection is provided. Its use is relatively straightforward, and illustrated in Figure 9-4. The key consideration is to tie the current limit circuitry's voltage reference to the SENSEFET's Kelvin terminal. This connection eliminates the errors that can be developed by high currents flowing in power ground.

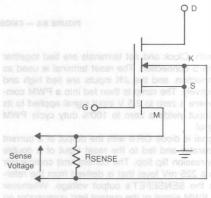


FIGURE 9-4 — KELVIN CONNECTION

Motor Drive set and to grantiged ent is set at golf gill Application Example (2000) The entit airli

An example of how SENSEFETs fit into a PWM motor drive is illustrated in Figure 9-5. This is a CMOS/Power MOS system based upon the MC14574 quad comparator, MC14027B dual J-K flip flop, MC14049UB inverter buffer, and MTP10N10M SENSEFET.

This system establishes a 2.5 V reference with a TL431, and uses this voltage to limit the peak of a 2.5 V ramp. This ramp is generated by charging timing capacitor CT until its voltage reaches 2.5 V, then tripping an R-S latch and turning on a small MOSFET until it has been discharged to approximately 250 mV. At this point the latch is reset, the B5170 MOSFET is turned off, and the cycle repeats. The MC14027B J-K in this case is configured as

FIGURE 9-5 — CMOS/SENSEFET MOTOR DRIVE allugio SOMTRAMS of self priod

an R-S latch. Clock and set terminals are tied together forming the S connection. The reset terminal is used as the R connection, and the J/K inputs are tied high and low respectively. The ramp is then fed into a PWM comparator, where a zero to 2.5 V input signal applied to its inverting input yields a zero to 100% duty cycle PWM output signal.

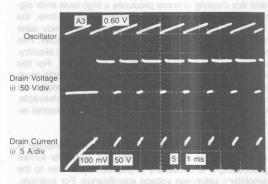
This signal is diode OR'd with the output of a current limit comparator and fed to the reset input of a double pulse suppression flip flop. The current limit comparator compares a 225 mV level that is derived from the reference with the SENSEFET's output voltage. Whenever either the PWM signal or the current limit comparator go high, this second flip flop is reset, thereby turning off the SENSEFET. The SENSEFET then remains off until the flip flop is set at the beginning of the next clock cycle.

This time the MC14027B J-K is configured as a reset dominant R-S latch. The connections are straightforward. The clock terminal serves as the "S" input and the reset terminal for the "R" connection. K and set terminals are grounded, J is tied high.

With the values shown, clock frequency is approximately 20 kHz and peak motor current is limited to 9 A. The MC14049 is quite adequate for providing gate drive at this frequency. Rise and fall times for the MTP10N10M are under 100 ns.

At lower PWM frequencies it is advisable to insert some resistance in series with the SENSEFET's gate in order to reduce switching noise. A 470 Ω series resistor produced the relatively clean waveforms in Figure 9-6, where the PWM rep rate has been set to approximately 1 kHz.

In this figure the ramp waveform at C_T is shown in the upper trace, SENSEFET drain current in the lower trace, and drain source voltage in the middle. Beginning with the second horizontal division a 2.5 V step function has been applied to the drive's input. The waveforms show an orderly startup, operating a 1/2 HP motor from an 80 V bus. The double pulse suppression technique syncs current limiting to the oscillator and provides for a safe, well controlled startup. When the double pulse suppression feature is removed, the MTP10N10M will fail almost instantaneously under the same starting conditions.



each to be some FIGURE 9-6 — STARTUP WAVEFORMS

Switching Power Supply Application Example

In order to work well with SENSEFETs, current-mode control circuitry has to accept relatively low values of sense voltage. First generation current-mode control IC's will accept the SENSEFETs output voltage during regulation but often are found lacking under short circuit conditions where current limit thresholds can be a volt or more for the most popular types.

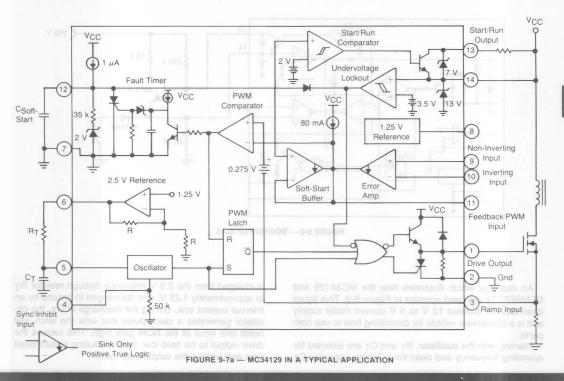
A new current-mode control IC, the MC34129, has an architecture which works quite well with SENSEFET output voltages, and provides a number of other second generation features. An illustration of the circuit and a timing diagram are provided in Figure 9-7.

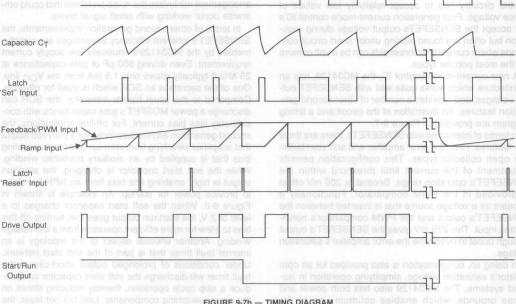
In terms of interfacing with SENSEFETs, there are three key features. First, the error amplifier and soft start buffer are open collector types. This configuration permits adjustment of the current limit threshold within the SENSEFET's operating range. Second, a 200 mV offset is provided in the PWM comparator. Functionally it appears as a voltage source that is inserted between the SENSEFET's output and the PWM comparator's noninverting input. This 275 mV gives the SENSEFET's output enough boost to overcome the error amplifier's saturation voltage.

In doing so, compensation is also provided for an opto isolator's saturation voltage, simplifying operation in isolated systems. The MC34129 also has both power and sense grounds, which enables optimum use of the SENSEFET's Kelvin source connection. As the application example in Figure 9-4 shows, the signal ground can

be connected to the Kelvin terminal while the power ground is connected to the SENSEFET's source. This arrangement minimizes the noise problems that could otherwise occur working with small signal levels.

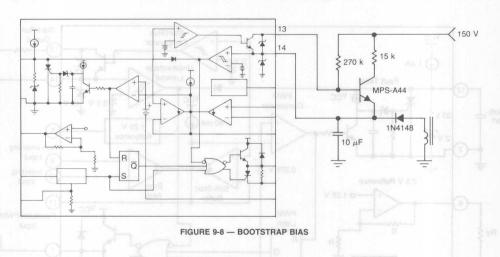
In terms of other second generation improvements, the SENSEFET's inherent efficiency advantages are complemented by the MC34129's unusually low supply current requirement. Even driving 500 pF of gate capacitance at 25 kHz it typically draws only 1.5 mA from the VCC line. One of the secrets is an SCR which is used for off-drive. Compared to the usual bipolar transistor, the SCR can discharge a power MOSFET's gate capacitance with considerably less bias current. For off-line applications, the second generation architecture includes a start-run output that simplifies switching from start-up bias to an operating bias that is supplied by an auxiliary bootstrap winding. While the soft start capacitor is charging, the start/run output is high, enabling line bias from an NPN transistor to provide power for startup. An example is shown in Figure 9-8. When the soft start capacitor charges to a level of 2 V, the start/run output goes low, turning off this bias to allow for more efficient operation from a low voltage winding. Another unusual aspect of the topology is an internal fault timer that is part of the soft start network. Under conditions of prolonged output short-circuit, the fault timer will discharge the soft start capacitor and produce a skip cycle operation, thereby reducing stress on the power switching components. Last but not least, the MC34129 also includes a sync/inhibit input which allows synchronization of the oscillator to an external signal.





ent tasel for fud tase almenogmos philidally Figure 9-7b — TIMING DIAGRAM

FIGURE 9-7 — MC34129



An example which illustrates how the MC34129 and SENSEFETs are used appears in Figure 9-9. This figure describes an isolated 12 V to 5 V current mode supply and is a convenient vehicle for describing how to use both parts.

Starting with the oscillator, RT and CT are selected for operating frequency and dead time. Timing capacitor CT is charged from the 2.5 V reference through resistor RT to approximately 1.25 V, and discharged to ground by an internal current sink. During the discharge of CT, the oscillator generates a clock pulse that sets the latch and holds one input of the NOR gate high. This causes the drive output to be held low, thus producing output dead time and limiting the output duty cycle.

1-9

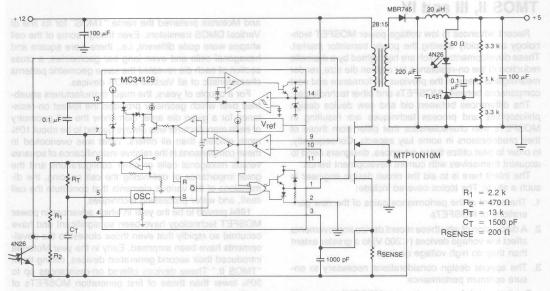


FIGURE 9-9 — MC34129/SENSEFET POWER SUPPLY 19WOOD TO VEVIUS 19110 IS JANUARY

The amount of dead time can be programmed by values chosen for R_T and C_T . Note that many combinations of R_T and C_T will give the same oscillator frequency, however, only one combination will yield a specific dead time at a given frequency. The values shown produce an operating frequency of 28 kHz and a maximum on-time slightly less than 50%.

The ramp voltage, V_{Ramp}, is generated by R_{SENSE} and fed into the PWM comparator's noninverting input at pin 3. The ramp's magnitude is determined by the value of R_{SENSE} and the amount of primary current that is switched. As a first order approximation:

$$V_{Ramp} \cong \frac{RSENSE \cdot IP \cdot rDS(on)}{rDM(on) + RSENSE}$$

where Ip represents primary current, rDS(on) is the SENSEFET's drain-source on resistance, rDM(on) is the sense section's on resistance, and RSENSE is identified in Figure 9-9. As a general rule of thumb, best results are obtained when RSENSE is chosen to produce at least a 100 mV signal at normal operating currents and also be no larger than rDM(on). Knowing the relationship between VSENSE and Ip, maximum short circuit current can be set with voltage divider R1, R2. The output voltage from this divider is coupled through a unity gain follower to set the upper trip point on the PWM comparator. To calculate the trip point, 275 mV of offset is added to the SENSEFET's output voltage.

The regulation loop may be closed with an opto isolator which pulls down the voltage at pin 9, thereby reducing maximum primary current and also duty cycle. This configuration is advantageous in that it saves components. R1 and R2 are used to both limit peak current and provide a connection for the opto isolator.

Soft start is provided in a rather straightforward manner by connecting a capacitor between pins 12 and 7. A 1 μA internal current source charges this capacitor, producing a voltage ramp on pin 12 during startup. The output is held low until the voltage at pin 12 exceeds the PWM comparator's 200 mV offset. As the soft start capacitor is charged further, maximum allowable duty cycle ramps up with the capacitor voltage until the limit imposed by R1 and R2 takes over.

For the example in Figure 9-9, the MTP10N10M SENSEFET has nominal values of $r_{DM(on)}$ and $r_{DS(on)}$ which are 288 Ω and 160 m Ω , respectively. Sense voltage with 288 Ω of RSENSE is therefore approximately 60 mV per amp of primary current. With R1 and R2 setting the upper trip point at 470 mV, peak current is limited to something just shy of 3 A, given the 275 mV offset. At startup, the 0.1 μF capacitor holds the output off for 20 ms, and allows full duty cycle after approximately 40 ms.

TMOS II, III and IV

Recent advances in low voltage power MOSFET technology are rapidly altering the power transistor market. These developments, which are highlighted by a dramatic reduction in the on-resistance for a given die size, render meaningless many of the previous performance and cost comparisons between MOSFETs and other technologies.

The differences between old and new device design philosophies and process techniques are resulting in MOSFETs with characteristics that differ from those of their predecessors in some key aspects. Consequently, in order to best utilize these advances, designers need to acquaint themselves with current development trends.

The intent here is to aid the circuit design engineer in such a study. The topics covered include:

- The extent of the performance gains of the new generations of MOSFETs
- A discussion of why these recent device improvements affect low voltage devices (<200 V) to a greater extent than they do high voltage devices
- 3. The special design considerations necessary to ensure optimum performance.

But first, a brief survey of power MOSFET history will help the reader understand why such remarkable performance improvements are possible.

A Brief History of Power MOSFETs

The history of power MOSFET development began less than a decade ago when device engineers started moving away from the conventional small-signal MOSFET structure, i.e., devices with all contacts on the surface of the die, long channel lengths and high on-resistance. Their inefficiency mandated the use of large die, which made the devices too expensive to compete with the bipolar transistor.

Lateral DMOS structures were the first devices that could reasonably be referred to as power MOSFETs. However, long channel lengths and poor silicon utilization still kept on-resistances and prices high. Other approaches soon followed.

A second breakthrough came with the advent of vertical current conduction. The first structures that allowed current to flow from the back of the die (the drain) to the source metallization on the top surface of the die were the V-groove devices, sometimes referred to as VMOS transistors. Although their development was an important step toward more efficient use of silicon, process and performance problems associated with the V-groove itself foretold its early demise. Most of the major manufacturers, including Motorola, once pursued this technology but have since abandoned it and have opted for the latest step in the progression toward more efficient silicon utilization.

By 1981, most manufacturers were persuaded that the Vertical DMOS technology was the most promising option. Its planar structure signaled simpler wafer processing, and its relatively short channel lengths promised low onresistances. Each company coined trademarks to refer to their special cell geometry and processing techniques. For example, International Rectifier developed the "HEXFET," Siemens introduced the "SIPMOS" transistor,

and Motorola preferred the name "TMOS" for its line of Vertical DMOS transistors. Even though some of the cell shapes were quite different, i.e., there were square and hexagonal cells and even long bar geometries, a cross section of each die revealed the same geometric patterns characteristic of all Vertical DMOS devices.

For a couple of years, the major manufacturers squabbled over which geometry provided the lowest on-resistance for a given die area. Somehow the cell geometry of each manufacturer was always quoted to be about 10% more efficient than all others. What was overlooked in these comparisons is the relative insignificance of squares versus hexagonal cells or other configurations and the great importance of optimizing the cell spacing, the dimensions of the various elements that constitute the cell itself, and wafer processing techniques.

1984 proved to be the year in which advances in power MOSFET technology have been so significant and have occurred so rapidly that even those closest to the developments have been surprised. Early in the year Motorola introduced their second generation devices, calling them "TMOS II." These devices offered on-resistances up to 30% lower than those of first generation MOSFETs of similar die size. Low voltage devices were the benefactors of most of the improvements. Adjustments to improve cell spacing, cell size, and in some cases cell geometry, were the features that distinguished TMOS II from TMOS I.

The final salvo of 1984 was fired in the fall when Motorola introduced the TMOS III line. Again a product introduction swept away preconceived notions of the limitations of power MOSFETs by making available devices with the lowest per unit area on-resistance in the industry. In an extension of the TMOS II design philosophy, cell packing densities rose from about 600K to 1 M for TMOS III. Diffusion profiles were optimized as was the resistivity of the silicon wafers used to build the devices. The combination of the increased packing density and the "short channel process" netted devices with on-resistances of about 1/4 that of the original TMOS.

There is an industry-wide trend toward smaller, more efficient, and less costly power MOSFET die. This fore-shadows the rapid extinction of all the original low voltage chip designs. Such pervasive change makes mandatory a familiarization with the benefits and limitations of the newest devices.

In the span of just a few months, the performance standards of power MOSFETs have been revised to the point that the difference between the old and new is almost difficult to appreciate. This raises the two questions, "How were such dramatic improvements possible?" and "Why are the improvements limited to low voltage devices?" Their answers can be found with the aid of Figure 9-10, which shows the components of rDS(on) within a low or high voltage cell. In high voltage devices the resistivity of the n-epi layer must be large to stand off a maximum drain-to-source rating of 400 V, for example. Based on the percentage of the total on-resistance that each component claims, the resistance of the n-epi is by far the most costly in terms of on-state efficiency. To significantly improve the conductivity of high voltage devices, therefore, the resistance of the drain, rp, must be reduced. (This is exactly the thrust of the GEMFET technology.)

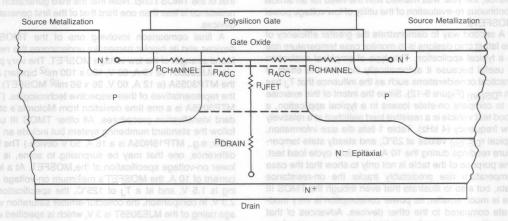


FIGURE 9-10 — THE COMPONENTS OF ON-RESISTANCE IN A HIGH- OR LOW-VOLTAGE MOSFET ARE CHANNEL RESISTANCE (RCHANNEL), DRAIN RESISTANCE (RDRAIN), JFET RESISTANCE (RJFET), AND RESISTANCE OF THE ACCUMULATION REGION (RACC). LOWER ON -RESISTANCE VALUES ARE EASIER TO ACHIEVE IN LOW-VOLTAGE DEVICES, WHERE CHANNEL RESISTANCE MAKES UP ABOUT 70% OF THE TOTAL RESISTANCE IN A POWER-MOSFET CELL.

The lower maximum V_{DS} rating of low voltage devices allows using an n-epi with a much lower resistivity. Although there is no clear definition of what constitutes a "high" or "low" voltage device, at a maximum V_{DS} rating of about 200 volts, the significance of the drain resistance begins to dwindle and the importance of the channel resistance, the resistance of the accumulation region, and the JFET resistance begins to dominate. Especially for MOSFETs with voltage ratings less than 100 V, efforts directed at reducing these resistances pay big dividends.

These dramatic changes in the silicon area necessary to provide a given on-resistance are a bonanza for power MOSFET users. Designers now have the pleasant task of deciding how to use the device improvements. They may, for instance, choose to greatly minimize on-state losses by replacing first or second generation devices with second or third generation units that have the same die size. With the conductivity of a given chip size increasing nearly fourfold in some cases, designers can drastically reduce heat-sinking requirements and greatly improve system efficiency.

The second option open to the designer is to select replacements on the basis of their on-resistance or current ratings. This entails using a device with a much smaller die. Since much of the cost of a power transistor is associated with processing of silicon wafers, the use of smaller chips means lower component cost.

Comparison of On-Resistance

In 1986, TMOS IV was introduced with a series of products called E-FETs. This product had all the advantages of TMOS III products but ruggedness was added.

Much has already been said about greater conductivity per unit area of silicon being the strength of the newest generation of power MOSFETs. But an appreciation of just how far device designers have furthered their art in this respect comes only after a review of some of the rDS(on) versus die size data.

One very enlightening illustration (Figure 9-11) allows easy comparison of the typical on-resistance associated with a TMOS I, II, III and IV chip. The original TMOS MTP15N05 requires 150 x 150 mil² of silicon to yield a typical 135 $M\Omega$ on-resistance. With TMOS II technology, on-resistances are pushed down to 125 $m\Omega$, with only 115 x 115 mil², about a 40% savings in silicon. Even with a 60% reduction in the original TMOS die area, TMOS III technology makes possible the added bonus of a 30% drop in rDS(on).

Almost as impressive as the performance gains is the rapid pace at which these changes are occurring. At the beginning of 1984, few realized that such dramatic improvements were possible, and virtually no one predicted the introduction of radically superior devices. Since each new generation delivered much greater perfor-

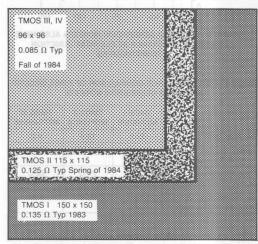


FIGURE 9-11 — FOR A GIVEN DIE SIZE, ON-RESISTANCE HAS

the latest chip designs is to monitor case temperature rise in a typical application. This type of empirical evaluation is useful because it automatically includes the effect of practical considerations such as the influence that Ti has on rps(on) (Figure 9-12). Since the intent of this exercise is to compare on-state losses in a typical application, a good test vehicle is a resistive load switched at a relatively low frequency (4 kHz). Table 1 lists die size information, typical rDS(on) values at 25°C, and steady state temperature readings during the 10 A, 14% duty cycle load test. The purpose of the table is not only to show that the case temperature rise predictably tracks the on-resistance data, but also to illustrate that even though the TMOS III die is much smaller, its power consumption is very moderate compared to the other devices. Advances of that proportion are normally restricted to the discovery of entirely new technologies and are not usually associated with improvements in existing techniques.

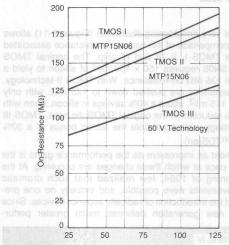


FIGURE 9-12 — THIRD GENERATION MOSFETS ALSO HAVE LOWER ON-RESISTANCE AT ELEVATED JUNCTION TEMPERATURES

TABLE 1 — ON-RESISTANCE COMPARISON OF FIRST, SECOND AND THIRD GENERATION MOSFETs

	TMOS I MTP15N06	TMOS II MTP15N06	TMOS III MTP14N06A		
Die Area (kmil ²)	22.5	12.5	9.2		
Typical rDS(on) @ 10 A, TJ = 25°C	135 ΜΩ	125 ΜΩ	85 MΩ		
Case Temperature During 10 A Test	74°C	71°C	66°C		
Normalized r _{DS} (on) Die Area = 22.5 kmil ²	1.0	0.54	0.26		

The last row of Table 1 offers another means of comparing device technologies. Those entries show the onresistance of each device with all die sizes normalized to

devices and its bipolar namesake underscores the newly found strength of the low voltage MOSFET. The very popular MJE3055T (a 10 A, 60 V, 100 x 100 mil² bipolar) and the MTP3055A (a 12 A, 60 V, 96 x 96 mil² MOSFET) are the representatives of their respective technologies. (The MTP3055A is a one time deviation from Motorola's standard identification procedures. All other TMOS III units follow the standard numbering system but include an "A" suffix, e.g., MTP16N05A is a 16 A, 50 V device.) The first difference, one that may be surprising to some, is the lower on-voltage specification of the MOSFET. At a load current of 10 A, the MOSFET's maximum on-voltage rating is 1.5 V, and at a T_J of 125°C, the specification is 2.3 V. In comparison, the collector-emitter saturation voltage rating of the MJE3055T is 3 V, which is specified with a base drive of 3.3 A.

The other advantages of the MOSFET are numerous and familiar to most. They are greater speed, more extensive forward biased and switching safe operating areas, simpler and much more efficient drive, higher pulsed current rating, and greater ease of paralleling.

Several other parameters of power MOSFETs vary from generation to generation. Most notable are lower overall capacitance and junction-to-case thermal impedance. Because a change in either can alter circuit operation, performance comparisons between MOSFETs of different generations should address the effect of both these characteristics on design practices.

An added bonus; faster switching

Switching speeds, gate-charge requirements, and input capacitance — all closely related parameters — are improving. Although the switching-speed comparison is not quite as straightforward as the on-resistance comparison, the end result is good news for those concerned about switching losses and gate-drive efficiencies. For example, the switching speed of the MTP14N05A, a TMOS III device, is about 35% faster than that of the TMOS I version of the MTP15N05.

Changes in device design actually increase parasitic capacitance per unit of silicon area — about 35% for the same die size from TMOS I to TMOS III. However, because input capacitance ($C_{\rm iSS}$) is directly proportional to die size, die-size reductions of as much as 75% more than offset the effect of the greater parasitic capacitance per unit of area. Clearly then, the capacitance, switching speeds, and gate charge for a given current rating are much improved. Of the three parameters, the gate-charge requirements tend to be the spec that most clearly defines the device's switching speed, for it is independent of gate-drive impedance.

It's difficult to predict switching speeds using values of input capacitance (specified at a V_{DS} of 25 V) or curves that relate capacitance to V_{DS} or V_{GD} . The results could also be wrong. The simplest and most accurate way to compare potential switching speeds is to use gate-charge waveforms. If the gate drive is a constant-current source, you can use the expression Q = It to relate charge to switching time.

Figure 9-13 shows the gate charge waveforms of the MTP14N06A and the similarly rated TMOS I and II MTP15N06. Properly interpreted, the curves contain much information regarding potential switching speeds and input capacitances. The curves can be divided into three regions, each of which corresponds to a specific interval of the turn-on transition. The first interval consists of the initial ramp of the gate-to-source voltage. During this period the input capacitance is charging, but there are no significant changes in the drain current or drain-to-source voltage. Since IG is constant in gate charge test circuits, the slope of the curve is inversely proportional to $C_{\rm iSS}$ (i = C dv/dt). Note that the slope of the TMOS III curve in this region is the steepest, indicating relative ease of charging and lowest input capacitance.

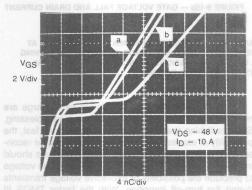


FIGURE 9-13 — GATE CHARGE REQUIREMENTS OF THE TMOS III MTP14N06A (a) AND THE TMOS II MTP15N06 (b) ARE MUCH IMPROVED OVER THAT OF THE TMOS I VERSION OF THE MTP15N06 (c)

During the second interval, the one in which the rise of the V_{GS} waveform falters and is stalled at a plateau, the drain voltage falls from the supply voltage to V_{DS}(on). Such a large change in V_{DS} brings a large swing in V_{GD} and requires substantial charging of C_{rss} (or C_{gd}, the Miller capacitance). Therefore, the amount of time spent,

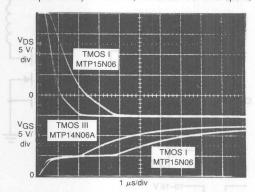


FIGURE 9-14a — GATE VOLTAGE RISE AND DRAIN-TO-SOURCE VOLTAGE FALL DURING TURN-ON.

or the amount of charge required, when moving through this region depends on the magnitudes of C_{rss} and the supply voltage. Here again, the TMOS III device delivers the best performance, needing only about 7 nC of gate charge compared to 8 and 11 nC for the TMOS II and I units.

Although switching is completed in Region 2, C_{iSS} continues charging until the gate-to-source voltage reaches the desired $V_{GS(on)}$. As in the first region, the slope of the waveform in this third region indicates the size of the input capacitance. Interestingly, all waveforms are now rising more gradually than they did in the first region. The magnitude of C_{iSS} , which is a function of the gate-to-drain voltage, is much higher now that the device is in the onstate, V_{DS} is relatively low and V_{GD} is positive.

Since the concept of required gate charge is based on a constant current gate drive, it applies directly to only those few gate drive topologies that can be modeled as constant current sources. Nevertheless, gate charge information does allow easy prediction of relative switching speeds, regardless of the type of gate drive.

As an example, consider driving a power MOSFET directly from a standard CMOS logic gate. The CMOS-MOSFET combination is especially important due to its simplicity and reduced parts cost. Based on the gate charge data in Figure 9-13, the drain voltage fall time of the MTP14N06A should be about 60% of that of the MTP15N06 — its TMOS I counterpart. That is indeed the case as shown in the turn-on and turn-off waveforms in Figures 9-14 a and b. The marked difference in transition times is directly attributable to the variation in gate charge requirements. The fact that TMOS III devices switch almost twice as fast as earlier units makes the use of a standard CMOS gate as a MOSFET driver more feasible.

This near doubling of switching speeds renews the possibility of using a standard CMOS gate as a MOSFET driver. Of course, although direct drive approaches are enticing, their associated switching losses limit operating frequency. A couple of assumptions and some recommendations from CMOS applications engineers allow a rough calculation of the operating frequency limits.

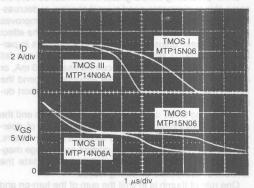


FIGURE 9-14b — GATE VOLTAGE FALL AND DRAIN CURRENT FALL DURING TURN-OFF.

FIGURE 9-14 — IN A COMPARISON OF FIRST AND THIRD GENERATION MOSFETS OF SIMILAR CURRENT RATINGS, TMOS III OUTCLASSES ITS PREDECESSOR BY SWITCHING NEARLY TWICE AS FAST WHEN DRIVEN BY A SINGLE CMOS GATE. IN THIS CASE A 1.5 k Ω SERIES GATE RESISTOR HOLDS PEAK GATE CHARGING CURRENT TO LESS THAN 10 ma.

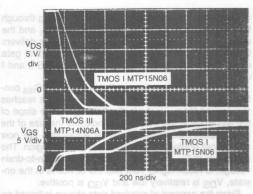


FIGURE 9-15a — GATE VOLTAGE RISE AND DRAIN-TO-SOURCE VOLTAGE FALL DURING TURN-ON.

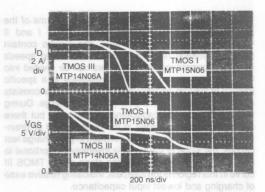


FIGURE 9-15b — GATE VOLTAGE FALL AND DRAIN CURRENT FALL DURING TURN-OFF.

FIGURE 9-15 — THE NEWEST MOSFETS, BECAUSE OF THEIR REDUCED GATE CHARGE REQUIREMENTS, CAN OPERATE AT HIGHER FREQUENCIES WHEN GATE DRIVE CURRENT IS LIMITED. HERE THREE PARALLELED CMOS INVERTERS ARE DRIVING THE MOSFET GATE THROUGH A SERIES RESISTANCE OF $100~\Omega$. EVEN AT FREQUENCIES APPROACHING 20~kHz, TOTAL TMOS III SWITCHING TIME IS ONLY 1% OF THE ENTIRE PERIOD.

To a large extent, switching speeds are strongly dependent on how hard one is willing to push the capabilities of the CMOS gate. The recommended maximum continuous output current is 10 mA per pin. Since these devices are not designed to drive highly capacitive loads such as a MOSFET gate, their pulsed current ratings are not specified.

Rigid adherence to the continuous specification results in the switching speeds shown in Figure 9-14. In this case, the TMOS I and TMOS III devices are driven from a single inverter of an MC14572, a hex gate IC. A 1.5 k series resistance between the output of the IC and the gate of the MOSFET limits peak charging and discharging to less than the 10 mA specification. Since the RMS value of the TMOS III gate current at 20 kHz is less than one milliampere, decreasing the magnitude of the series gate resistance is tempting.

Either paralleling CMOS gates, which must be from the same chip to guarantee good current sharing, or decreasing the value of the series gate resistance improves switching times. Figures 9-15 a and b illustrate the effect of both of these adjustments. With three inverters in parallel and a 100 Ω series resistance, transition times fall well below the 1 μ s. Peak gate current rises to 40 mA, or about 13 mA per gate. This brief excursion beyond the 10 mA specification is harmless because of its short duration (<300 ns).

Translating these current and voltage fall times and the associated switching losses into an upper limit of operating frequency is a subjective exercise. Many factors, including available heatsinking, current and voltage magnitudes, on-state losses and duty cycle, dictate the amount of acceptable switching losses.

One rule of thumb is to limit the sum of the turn-on and turn-off transition times to less than 1% of the period. Using this criterion, the TMOS I device driven from a single CMOS inverter is limited to 1.3 kHz and the TMOS III equivalent is bounded by 2.4 kHz. With the three gates in parallel, 9 and 17 kHz are the upper limits.

Although faster switching and lower gate charge are normally desirable traits, they can be a mixed blessing. Since switching speeds may be almost twice as fast, the possibility of excessive voltage transients must be reconsidered. The design of all power MOSFET circuits should include rigorous monitoring of the drain-to-source voltage to preclude the possibility of excessive voltage transients during the turn-off transition. With the faster TMOS III devices this concern becomes more critical. Speeding the response time of the overvoltage protection circuitry may be needed if the device is switched more rapidly. When greater speeds are unnecessary, a higher gate drive impedance in the form of a resistance in series with the gate slows the switching transitions and simplifies the design of overvoltage protection circuitry.

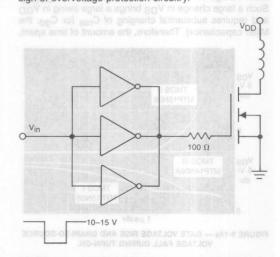


FIGURE 9-15c — THREE STANDARD CMOS INVERTERS OF AN MC14572 DRIVING A MOSFET GATE WITHOUT THE AID OF A BUFFER STAGE.

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Thermal considerations are important

It's also important that you understand the thermal implications of the smaller die sizes of third-generation MOS-FETs. A lower rDS(on) value per unit area increases the power-handling capability of a given die size, but the ability to dissipate power is still tied to the thermal resistance of the device. The newer, smaller devices — sometimes less than a third the size of their predecessors — have less area in contact with their cases, which increases their thermal resistance and decreases the power they can dissipate. It's therefore not a good idea to select replacements for first-generation MOSFETs solely on the basis of on-resistance and drain-to-source breakdown voltage.

Because junction temperatures directly affect long-term reliability, the T_J value is an important indicator of a transistor's exposure to stress. Where junction temperature is such a major concern, the junction-to-case thermal impedance also becomes critical. In fact, when it comes to minimizing junction temperature, the magnitude of the thermal impedance is almost as important as the value of on-resistance. The following example shows why.

Assume that Device A is a first generation MOSFET that is being replaced with Device B, a third generation unit. With the RMS value of the drain current held constant in each instance, a requirement of Device B is that its operating junction temperature must be less than or equal to that of Device A.

If
$$T_{J1} = T_{J2}$$

then $P_{D1}(R_{\theta JC1} + R_{\theta CA}) = P_{D2}(R_{\theta JC2} + R_{\theta CA})$
or $I_{RMS}^2 I_{DS}(on) 1(R_{\theta JC1} + R_{\theta CA}) = I_{RMS}^2 I_{DS}(on) 2(R_{\theta JC2} + R_{\theta CA})$

If, for a moment, $R_{\theta}CA$ is assumed to be zero, the equation simplifies to: Albim salug of all disonges (sele

$$(rDS(on) \times R_{\theta}JC)_1 = (rDS(on) \times R_{\theta}JC)_2$$

This equation states that if the case temperatures are held constant, which is assured when $R_{\theta CA} = 0$ (infinite heat sink); then equating the product of the thermal resistance and the on-resistance guarantees that the junction temperatures will be the same. Therefore, this product, referred to as the "resistance product," is a useful tool for comparing devices from different technologies or

The best way to elaborate on the concept of the resistance product is with a numerical example. Table 2 contains the ratings of Motorola's IRF531 and the MTP14N06A. On the basis of their similar resistance products, they might be considered to be direct replacements.

TABLE 2 — CHARACTERISTICS OF DEVICES WITH SIMILAR RESISTANCE PRODUCT RATINGS

	Device A	Device B		
Device Type	IRF531	MTP14N06A		
Technology	TMOS I	TMOS III		
rDS(on)	0.18 Ω	0.10 Ω		
$R_{\theta JC}$	1.67°C/W	3.12°C/W		
PD(max)	75 W	40 W		
Resistance Product	0.30°C/A ²	0.31°C/A ²		

Let I_{RMS} = 10 A and R_{θ CA} = 3°C/W

Then
$$P_{D1} = (100 \text{ A}^2 \times 0.18 \ \Omega)$$
 $P_{D2} = (100 \text{ A}^2 \times 0.10 \ \Omega)$

$$\begin{array}{lll} \Delta T_{JC1} = P_{D1} R_{\theta JC1} & \Delta T_{JC2} = P_{D2} R_{\theta JC2} \\ = 18 \ W \ x \ 1.67 ^{\circ} C/W & = 30 ^{\circ} C & = 31 ^{\circ} C \end{array}$$

As expected, the junction to case temperature rise in each instance is nearly the same because the resistance products are so closely matched. But here the similarity ends due to the greater efficiency of the smaller chip. Depending on the magnitude of the case to ambient thermal resistance, the case to ambient temperature differential, T_{CA} , might vary considerably. When $R_{\theta CA} =$ 3.0°C/W, then

$$\Delta T_{CA1} = 3.0^{\circ} \text{C/W} \times 18 \text{ W} \text{ and } \Delta T_{CA2} = 3.0^{\circ} \text{C/W} \times 10 \text{ W}$$

= 54°C = 30°C

For
$$T_A = 25^{\circ}C$$
,
 $T_{J1} = \Delta T_{JC1} + \Delta T_{CA1} + T_A$ and $T_{J2} = \Delta T_{JC2} + \Delta T_{CA2} + T_A$
 $= 30 + 54 + 25^{\circ}C$ $= 31 + 30 + 25^{\circ}C$
 $= 109^{\circ}C$ $= 86^{\circ}C$

= 86°C

As the numbers illustrate, a constant resistance product does not always guarantee identical junction temperatures — it only forces the same ΔT_{JC} . In fact, if the case to ambient thermal resistance is high, junction temperatures may be quite different. However, the product can still be used as a comfort factor when designing in the newer power MOSFET generations. If the resistance product is held constant, the on-resistance of the more efficient device must be lower even though its junction to case thermal impedance is higher. Therefore, the newer device will dissipate less power for a given load current by virtue of its lower on-resistance. The lower power dissipation then results in a smaller case to ambient temperature differential and a lower junction temperature.

The preceding analysis ignores how T_J affects onresistance, a very important consideration. The interdependence of the magnitude of rDS(on), TJ and power dissipation makes the resistance product an inexact tool. Also, the concept of the resistance product is based on the steady state thermal resistance and is, therefore, not appropriate for transient analysis. In spite of these inadequacies, the concept is useful for first order approximations, and it does illuminate some of the considerations that must be thought through to safely utilize the advantages of the new technology. For a more detailed thermal analysis, Motorola's AN569, "Transient Thermal Resistance — General Data and Its Use" is an excellent guide.

Fortunately for the designer, die size, steady state and transient thermal impedance, on-resistance, maximum allowable junction temperature and package limitations are all factored in when a device's maximum pulsed and continuous current ratings are assigned. Consequently, the MTP16N05A (which is a 16 A, 50 V device of the TMOS III vintage) is almost always a drop in replacement for any other 16 A, 50 V power MOSFET. The lower maximum on-resistance specification compensates for the smaller die and increased junction-to-case thermal impedance. Linear applications are an exception to this rule since the main concern in those circuits is power dissipation capability. Die area and thermal impedance must remain unchanged in those cases since improvements in onresistance often do not reduce power dissipation.

preciated. The new efficiency and economy of the low voltage MOSFETs foreshadows their dominance of that section of the power transistor market.

The automotive industry is among those likely to welcome a means of cost effectively controlling large continuous and pulsed currents. Specific applications involve the control of the many small motors found under the dash and hood and in the doors, the replacement of mechanical relays, and the switching of many lamps and solenoids. Interestingly, automakers often have little use for the MOSFET's most proclaimed attribute, its tremendous switching speed. Instead, they are impressed by its low on-voltages, extensive SOA, and modest gate drive requirements.

The use of MOSFETs for synchronous rectification is an example of an application that deserves reconsideration. Previously, MOSFETs had trouble competing with Schottky diodes, for example, because the MOSFET required much more silicon area to deliver the same performance. With the precipitous drop in per unit area onresistance, the MOSFET is now much more competitive (Figure 9-16).

Several other applications come to mind, for example, solid state relays, hammer drivers for printers, telecommunications equipment, and output stages for programmable controllers. But the application primed for the introduction of such a switch is the brushless DC motor controller. As the cost of the semiconductor control circuitry continues to fall, the benefits of the electronically commutated motor — high efficiencies, linear speed/torque characteristics, long service life, the potential for speed control, etc. — will become more affordable.

binary to decimal decoder) and the six OR gates provide the proper logic sequence to control the output transistors. The relatively low commutation frequency is strictly a function of the motor speed, because the Hall effect sensors ultimately determine the firing sequence.

For simplicity, a P-channel MOSFET, an MTP5P20, was used as the power switch in the upper legs of the bridge. With a few drive circuit modifications, a PNP bipolar or even an NPN Darlington could also fill that socket. The most qualified candidate to serve as the low side switch is one of the third generation MOSFETs, again a 96 x 96 mil^2 chip. This device has a drain-to-source voltage rating of 200 V and a typical rDS(on) of only $0.3~\Omega$. A continuous motor load current of about 2 A causes negligible power dissipation in this device.

In the open loop system shown in Figure 9-17, motor speed is unregulated and is a function of the motor characteristics, the type of load and the magnitude of the DC supply voltage. Changing the supply voltage or using pulse width modulation allows regulation of motor speed. In this case, the best place for a speed control network is between the OR gates and the hex buffer.

There are three ways to control the effective motor voltage with pulse width modulation. The designer may PWM only the bottom three transistors, or only the top devices. The third option, pulse width modulation of both the upper and lower devices, also controls motor speed. The simplest approach is to pulse width modulate MOSFETs in the lower legs of the bridge. In that position, the MOSFET shows off several of its most advantageous attributes. It is fast, cost effective, efficient and very easy to drive.

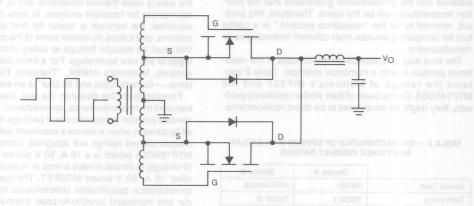


FIGURE 9-16 — USING POWER MOSFETS AS "SYNCHRONOUS RECTIFIERS" IN THE OUTPUT STAGE OF A SMPS CAN REDUCE RECTIFICATION LOSSES. WHEREAS MOSFETS ONCE REQUIRED TOO MUCH SILICON TO RIVAL THE SCHOTTKY DIODE NORMALLY USED, THE NEWEST MOSFETS ARE MUCH MORE COMPETITIVE.

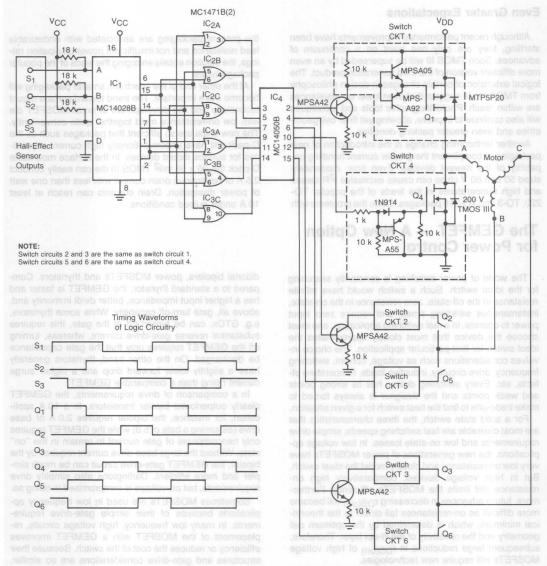


FIGURE 9-17 — TO SIMPLIFY THE DESIGN OF THIS BLOWER-MOTOR CONTROL CIRCUIT, THE UPPER LEGS OF THE BRIDGE EMPLOY A P-CHANNEL MOSFET FOR THE POWER SWITCH

Pulse width modulation of only the lower devices also circumvents one other potential problem. Even in these third generation devices, the MOSFET's diode is still sensitive to high dv/dt's (in the range of 1 volt per nanosecond) during its reverse recovery time. Use of a bipolar, in parallel with a discrete diode, is a tidy solution. The discrete

diode doesn't mind the commutation stresses imposed by the fast switching MOSFETs. Also, rapid turn-on of the bipolars is unnecessary because their switching frequency, which is tied to the motor speed, is much lower. Therefore, the MOSFET's intrinsic diode need not endure the rigors of very high dv/dt.

Even Greater Expectations

Although recent performance improvements have been startling, they are only one point on a continuum of advances. Soon TMOS III will be superseded by an even more efficient version of the third generation product. The logical extension of certain changes in design philosophy from TMOS I to III suggest that even lower on-resistances are within reach. Photolithographic tools and techniques will also continue to improve, allowing yet finer cell geometries and even greater packing densities.

Another forthcoming change is the introduction of new packaging to compliment the greater current handling capability of the newest devices. Even now, moderately sized 50 and 60 V chips can cause excessive I²R losses and high temperatures in the leads of the popular TO-220, TO-3 and TO-218 packages. Since the problems with

The GEMFET — A New Option for Power Control

The world of power switching is constantly searching for the ideal switch. Such a switch would have infinite resistance in the off-state, zero resistance in the on-state, instantaneous switching times, and require zero input power to operate. In a real switching application, one must choose the device that most closely approximates the ideal switch for that particular application. The choice involves considerations such as voltage, current, switching frequency, drive circuitry, inductive loads, temperature effects, etc. Every switching device has its strong points and weak points and the designer is always forced to make trade-offs to find the best switch for a given situation.

For a solid state switch, the three characteristics that are most desirable are fast switching speeds, simple drive requirements and low on-state losses. In low voltage applications, the new generations of power MOSFETs have very low on-resistance and closely model the ideal switch. But in high voltage devices, comparatively high onresistance still limits the MOSFETs efficiency. Furthermore, future advances in decreasing rDS(on) will become more difficult as on-resistances fall closer to the theoretical minimum, which is determined by the optimum cell geometry and the resistivity of the N-epi layer. Therefore, subsequent large reductions in rDS(on) of high voltage MOSFETs will require new technologies.

The GEMFET (Gain Enhanced MOSFET), also called an insulated gate bipolar transistor (IGBT), is the result of one such technological advance. It is a relatively new high voltage power semiconductor device with a combination of characteristics previously unavailable to the designer of power circuitry. Closely related to the power MOSFET in structure, this new device has forward voltage drop comparable to bipolars while maintaining the high input impedance and fast turn-on associated with the isolated gate of the MOSFET. Although turn-on speeds are very fast, current fall times of approximately 4.0 μs are quite slow, and may restrict the use of at least the first generation of these devices to lower frequency applications.

At switching frequencies below about 10 kHz, however, the GEMFET is an attractive alternative to the more trathe present packaging are associated with undesirable lead resistance and not insufficient power dissipation ratings, the solution entails enlarging the leads of the popular package types.

At the other end of the spectrum, smaller packaging will become more important. The trend toward surface mount technology and the development of small MOSFET die with low on-resistance meld together quite conveniently. The new chips are so efficient that packages such as the D-pack will have unconventionally high current capabilities for surface mount devices. In the surface mountable D-pack the 96 x 96 mil² TMOS III die can easily conduct 2.5 A of continuous drain current with less than one watt of power dissipation. Drain currents can reach at least 10 A under pulsed conditions.

ditional bipolars, power MOSFETs and thyristors. Compared to a standard thyristor, the GEMFET is faster and has a higher input impedance, better dv/dt immunity and, above all, gate turn-off capability. While some thyristors, e.g. GTOs, can be turned off at the gate, this requires substantial reverse gate-drive current, whereas, turning off the GEMFET requires only that the gate capacitance be discharged. On the other hand, thyristors generally have a slightly lower forward drop and a higher surge current rating than a comparable GEMFET.

In a comparison of drive requirements, the GEMFET clearly outperforms bipolar transistors. In a 10 A application, for instance, the bipolar requires 2.0 A of base drive (assuming a beta of 5.0) while the GEMFET requires only nanoamperes of gate current to remain in the "on" state. Without the large base-drive current required by the bipolar, the GEMFET gate-drive circuit can be much simpler and more efficient. Darlingtons also simplify drive requirements, but on-voltage is compromised in doing so.

Sometimes MOSFETs are used in low frequency applications because of their simple gate-drive requirements. In many low frequency, high voltage circuits, replacement of the MOSFET with a GEMFET improves efficiency or reduces the cost of the switch. Because their structures and gate-drive considerations are so similar, the change usually entails no significant circuit modifications. Substitution of a GEMFET with approximately the same die area dramatically improves on-state efficiency and current ratings.

If cost is a major concern, another option is to replace the power MOSFET with a GEMFET that has a smaller die area. The result can be a device with a similar current rating and comparable on-state losses. Except at higher frequencies, the cost/performance tradeoffs are substantially in favor of the GEMFET.

The GEMFET is suitable for high current, high voltage, low frequency applications because of its low forward drop and relatively long turn-off time. Appropriate applications for the GEMFET include motor drive circuits, automotive switches, programmable controllers, robotics, home appliances, machine tools, etc.

The GEMFET is very similar to the double-diffused power MOSFET. Simply by varying starting materials and by altering certain process steps, a GEMFET may be produced from a power MOSFET mask set. Figure 9-18 illustrates that the two structures are identical except for the P+ layer adjacent to the drain metalization. Additional current carriers in the form of holes are injected from the P+ substrate into the normally high resistivity N-epi layer and markedly reduce the on-voltage. The resulting four layer structure (P-N-P-N) allows current densities much greater than those attainable in power MOSFETs and comparable to those of bipolars.

Like the power MOSFET, the gate of the GEMFET is electrically isolated from the rest of the chip by a thin layer of SiO₂. Accordingly, the GEMFET is also a high input impedance device and exhibits the associated advantages of modest gate-drive requirements and excellent gate-drive efficiencies. The uniqueness of the GEMFET is that low on-voltages as well as high input impedances are now available in high voltage power semiconductors.

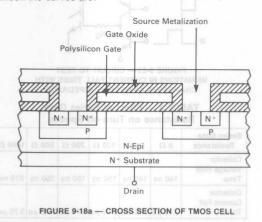
The symbols and equivalent circuits of the GEMFET and MOSFET are shown in Figure 9-19. Because of its four layer structure, the GEMFET lacks the parasitic drain-source diode common to nearly all power MOSFETs.

Device Characteristics

Output Characteristics

In the forward conduction mode, the GEMFET closely resembles a power MOSFET. The equivalent circuit is best modeled as shown in Figure 9-19 in which a low voltage, low rpS(on), N-Channel MOSFET is driving a PNP transistor in a compound configuration. The PNP device not only helps lower the effective rpS(on), but also enhances the device gain (transconductance) at high drain currents. Except at excessive drain currents or junction temperatures, the NPN device is considered to be a parasitic and does not influence circuit operation.

The output characteristics of a popular power MOSFET (MTP4N50) and a GEMFET (MGP20N50) of identical die dimensions and similar breakdown voltages are shown in Figures 9-20a and 9-20b. The two major differences between the curves are:



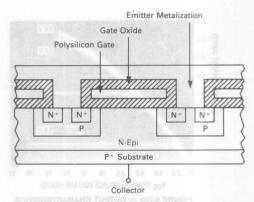


FIGURE 9-18b — CROSS SECTION OF GEMFET CELL

- The GEMFET has a much lower on-resistance at currents greater than 2.0 A.
- 2 Before the GEMFET can conduct current, the P-N junction formed by the P+ substrate and the N-epi layer must be forward biased. Consequently, the GEMFET curves are offset from the origin by a diode drop, similar to SCRs or Darlingtons.

Figure 9-21 indicates that at 25°C the 20 A, 500 V MGP20N50 gives no hint of a propensity to latch at currents up to 62 A, which is much larger than the pulsed current rating of the MOSFET.

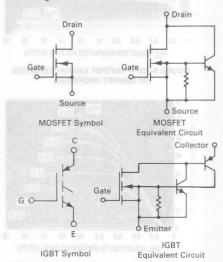


FIGURE 9-19 — MOSFET AND GEMFET SYMBOLS AND EQUIVALENT CIRCUITS

Switching Speeds

Presently, the feature that limits the GEMFET from serving a very wide range of applications is its relatively slow turn-off speed. While turn-on is fairly rapid, current fall times at turn-off can exceed 4.0 μ s.

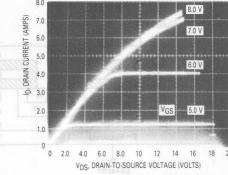


FIGURE 9-20a — OUTPUT CHARACTERISTICS
OF POWER MOSFET (MTP4N50)

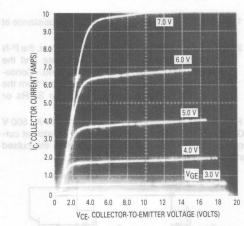


FIGURE 9-20b — OUTPUT CHARACTERISTICS OF GEMFET (MGP20N50)

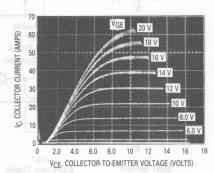


FIGURE 9-21 — OUTPUT CHARACTERISTICS OF GEMFET AT HIGH DRAIN CURRENTS

The turn-off of the GEMFET is rather slow because many minority carriers are stored in the N-epi region. When the gate is initially brought below threshold, the N-epi contains a very large concentration of electrons, consequently, there will be significant electron injection into the P+ substrate and a corresponding hole current into N-epi.

As the electron concentration in the N-region decreases, the electron injection decreases, leaving the rest of the holes and electrons to recombine. The turn-off of the GEMFET should then have two phases: the injection phase where the drain current falls very quickly; and a recombination phase where the drain current decreases more slowly. Figure 9-22 shows the clamped inductive turn-off waveforms of the MGP20N50.

Although turn-off speeds are not impressive, this is the first generation of these devices and improvements in switching speeds can be expected. For GEMFETs, there is an rCE(on) — switching speed trade-off. Theoretically, turn-off times can be decreased without large increases in rDS(on) by controlling carrier lifetimes or by other proprietary methods.

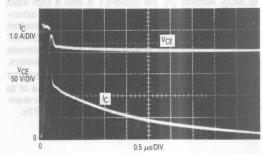


FIGURE 9-22 — CLAMPED INDUCTIVE TURN-OFF OF GEMFET

Even though MOSFETs are championed for their simple gate-drive requirements, at high operating frequencies sizable peak gate currents must be supplied to ensure rapid switching. Since this first generation GEMFET is, by comparison, much slower, the gate drive-impedance can be fairly high without affecting turn-off speeds. In the circuit shown in Figure 9-23, R_G was varied from 0 to 1.0 k Ω , but the current fall time essentially remained constant at 3.75 μ s (Table 3).

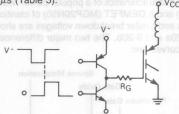


FIGURE 9-23 — CIRCUIT TO TEST VARIATIONS IN CURRENT FALL TIMES WITH CHANGES IN GATE DRIVE IMPEDANCE

TABLE 3 — Effect of Series Gate Resistance on Turn-off Speeds

Series Gate Resistance	0 Ω	50 Ω	100 Ω	200 Ω	500 Ω	1000 Ω
Collector Voltage Rise Time		140 ns	150 ns	180 ns	350 ns	810 ns
Collector Current Fall Time	3.75 μs					

Comparison of On-State Losses

The most pronounced advantage of the GEMFET over the power MOSFET is its lower on-resistance. The VDS(on) of a high voltage MOSFET is fairly large and rises with increasing junction temperature and drain current. Conversely, the VCE(on) of a GEMFET decreases with increasing TJ and is not greatly affected by Ic. Figure 9-24 compares the on-voltages of the two technologies at various drain currents and at a TJ of 25°C and 100°C. Since the MOSFET does not have the GEMFET's offset voltage in its output characteristics, at low currents the MOSFET on-voltage is slightly lower. However, as the illustration suggests, at high currents and temperatures the difference is dramatic. For comparison, a bipolar transistor was also included in Figure 9-24. Its on-voltage is

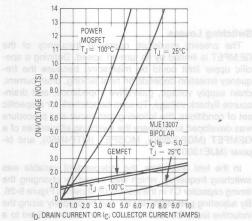


FIGURE 9-24 — ON-VOLTAGE versus DRAIN OR COLLECTOR
CURRENT FOR A GEMFET, MOSFET AND BIPOLAR OF
EQUIVALENT DIE SIZE

a function of the transistor's high current beta and the magnitude of the base current.

On-state efficiencies are not solely determined by onvoltages. Gate or base-drive currents are also contributing factors. Its high input impedance allows the GEMFET to rival the on-state efficiency of the bipolar transistor, even though its on-voltages are comparable to those of SCRs (one diode drop in addition to a bipolar saturation voltage). The bipolar device chosen for this comparison had a forced beta so low (about 5) at the desired collector current that the base current losses were important.

To illustrate the variation in the on-state efficiencies of each technology, a bipolar transistor, MOSFET and GEMFET were used as the switching element in an open loop PWM dc motor control circuit. The bipolar (MJE13007) was a 156 x 156 mil chip rated at 8.0 A, 400 volts. The 20 A, 500 volt GEMFET (MGM20N50) and the 4.0 A, 500 volt MOSFET (MTP4N50) had areas equivalent to a die size of 150 x 150 mil. To keep switching losses to a minimum, the frequency was held constant at about 90 Hz as the duty cycle was varied from 9% to 71%. Since

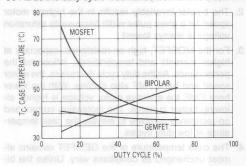


FIGURE 9-25 — ON-STATE EFFICIENCY COMPARISON — PULSE WIDTH MODULATION OF DC MOTOR

TABLE 4 — On-State Efficiency Testing: Pulse Width Modulation of DC Motor

	Pulse Width (ms)	Duty Cycle %	or ID(max) (A)	Case Temp (°C)	Power Dissipation (W)	On Voltage (Volts)	V _{DS} or V _{CE(pk)} (Volts)	Relative Power Out (Speed)	Relative Power In
GEMFET		5	1 1					The state of the s	
(MTM20N50)	8.0	71	0.75	37.2	0.69	1.0	1.75	78	2.0
	6.0	54	1.0	37.4	0.70	1:1	2.0	77	2.0
	4.0	36	1.6	38.5	0.75	1.1	2.5	73	2.0
	2.0	18	2.75	39	0.79	1.5	4.0	64	2.0
	1.0	9.0	4.50	40.9	0.86	2.0	6.5	49	2.0
TMOS	(2)			-	/				. 1 En l
(MTP4N50)	8.0	71	0.75	38.6	0.76	1.0	1.75	78	2.0
in the second	6.0	54	0.80	42.1	0.91	1.3	2.25	77	2.0
	4.0	36	1.25	49.4	1.22	2.0	3.25	70	2.0
	2.0	18	2.25	62	1.77	4.5	6.50	48	2.0
	1.0	9.0	3.50	77.4	2.44	7.5	11.00	18	2.0
BIPOLAR			1	1/2					
(MJE13007)	8.0	71	0.80	49.7	1.24	0.1	0.8	82	140
	6.0	54	1.1	45.7	1.06	0.2	1.0	81	104
	4.0	36	1.5	40.7	0.85	0.2	1.5	78	72
	2.0	18	2.75	34.8	0.59	0.3	3.0	70	36
	1.0	9.0	4.5	32.6	0.50	0.5	5.0	59	20

T = 11.2 ms $T_A = 21.2^{\circ}C$ $f \approx 90 \text{ Hz}$ $V_{DD} \approx 14 \text{ V}$ $R_{\theta HS} = 23^{\circ}C/W$

a motor is a nonlinear load and conditions such as motor speed and back EMF change with pulse width, the results of the comparison (Table 4 and Figure 9-25) should be carefully interpreted.

The "relative power out" referred to in Table 4 is simply a measurement proportional to the motor speed and is inversely related to the saturation voltage. If the onvoltage is high, the potential across the motor is diminished and the speed is decreased. The "relative power in," a measure of forward base (or gate) current, is useful for comparing the required base or gate power necessary to control a five ampere load.

The following generalizations can be drawn from Table 4 and Figure 9-25:

- 1. Even though its on-voltage is very low, the bipolar loss not the most efficient device at high duty cycles. The power consumed by the device due to its large base current is great enough to be reflected in an increase in case temperature. Because of the bipolar's low beta, the case temperature and power dissipation closely track the relative power in.
 - The bipolar invariably results in the highest motor speed for a given pulse width because its saturation voltage is always lowest.
 - 3. For the MOSFET, high on-resistance, especially at higher currents and temperatures, influences the performance. As the duty cycle decreases, the motor speed and back EMF also decline. With the lower back EMF, the effective motor voltage is higher, allowing higher currents. The increasing current and on-resistance combine to elevate the case temperature at low duty cycles.
 - 4. The case temperature of the GEMFET remains almost unchanged as conditions vary. Unlike the bi-

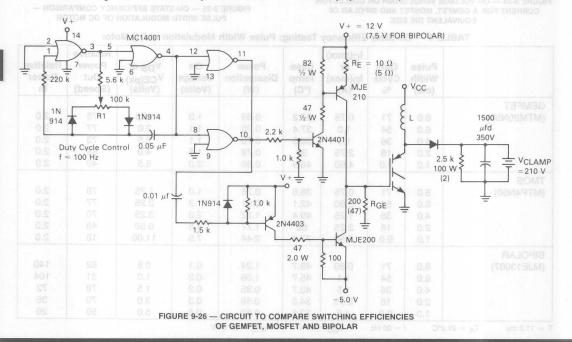
polar, its input power is very small and does not significantly affect the power dissipation at high duty cycles. At lower duty cycles and higher currents, the GEMFET on-voltage is much lower than the MOSFET's. Again, the result is cooler case temperatures.

While the GEMFET looks quite respectable in this comparison, the peak current chosen influences the relative efficiencies. If the motor supply voltage had been increased to obtain larger peak currents, the comparison would have been even more in favor of the GEMFET. The MOSFET would have performed more poorly due to its ID-rDS(on) relationship, and the bipolar's base drive losses, due to forced betas' less than 5.0, would further reduce its efficiencies at large pulse widths.

Switching Losses

The present maximum operating frequency of the GEMFET is limited by its turn-off speed. Defining a specific upper limit could be misleading because the frequency limitation depends on heat sinking, drain current, drain supply voltage, gate-drive impedance, and drain-source flyback voltage. To set a benchmark for a specific set of conditions, the following test circuit and procedure was developed to compare the switching efficiencies of a GEMFET (MGP20N50), MOSFET (MTP4N50), and bipolar (MJE13007).

In the test procedure, the independent variable was switching frequency, which was varied by changing the timing capacitor C1 in the test circuit shown in Figure 9-26. By adjusting potentiometer R1 and by properly sizing the inductive load, the load current waveform was fixed to a 25% duty cycle and a peak of 5.0 A.





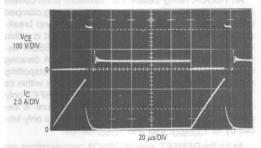


FIGURE 9-27a — CLAMPED INDUCTIVE SWITCHING WAVEFORMS AT 7.0 kHz — GEMFET

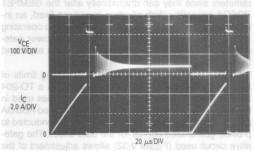


FIGURE 9-27c — CLAMPED INDUCTIVE SWITCHING
WAVEFORMS AT 7.0 kHz — BIPOLAR

For the MJE13007, the forced beta of 5.0 required a base current of 1.0 A. Turn-off of all three types of devices was initiated by clamping the base (or gate) to -5.0 volts. The oscillograms in Figure 9-27 show the drain (or collector) current and drain-source (or collector-emitter) voltage of each device at 7.0 kHz.

Again, the test results were quite predictable, and the case temperature versus frequency for this specific case is plotted in Figure 9-28. The efficiency of the heat sink, in this instance a 41/2" x 41/2" x 1/8" copper plate (R $_{\theta}CA=5^{\circ}C/W$), markedly influences the temperature rise results. A larger or smaller heat sink would have decreased, or increased, the noted temperature differences. The testing was restricted to lower frequencies because above 40 kHz secondary effects began to influence and distort the comparison.

The GEMFET switching losses rose rapidly with frequency, illustrating its high-frequency limitations. By comparison, the bipolar's case temperature increased only slightly while the MOSFET proved its high frequency capability with virtually no case temperature rise.

Thermal Resistance, RaJC

As expected, GEMFETs and power MOSFETs produced from the same mask set have very similar junction-to-case thermal resistances. $R_{\theta JC}$ of a power MOSFET can be determined by testing for variations in one of the following temperature sensitive parameters, or TSPs:

- 1. Drain-source diode on-voltage
- 2. Gate-source threshold voltage
- 3. Drain-source on-resistance

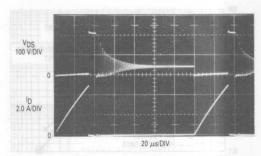


FIGURE 9-27b — CLAMPED INDUCTIVE SWITCHING WAVEFORMS AT 7.0 kHz — MOSFET

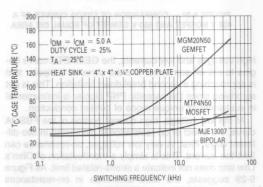


FIGURE 9-28 — COMPARISON OF CASE TEMPERATURE VERSUS FREQUENCY FOR A GEMFET, MOSFET AND BIPOLAR

All previous thermal resistance testing of the TMOS power MOSFET was based on the temperature dependence of the on-voltage of its drain-source diode. For the MTP4N50, the results were typically about 0.79°C/W. Because the GEMFET has no parasitic diode, this method was inappropriate for the MGP20N50. Instead, RaJC of the GEMFET was determined by using a second circuit that detects variations in the gate-source threshold voltage due to changes in T.J. Before testing the GEMFET, correlation between the two test methods was obtained by comparing the results of testing the MOSFET in each circuit. By testing for variations in threshold voltage, the RAJC of the MTP4N50 and the MGP20N50 were both typically 0.67°C/W. This suggests that the two methods are in fairly close agreement and that the thermal resistances of a MOSFET and GEMFET of equal die area are essentially the same.

Safe Operating Areas

Important ratings of any solid state switching element are its Safe Operating Areas. For the GEMFET, these include its Forward Biased SOA, or FBSOA, and Reverse Biased SOA, or RBSOA. Since non-destructive fixtures were used to determine both of these SOA limitations, an entire curve could be drawn with each device tested. With this capability, device trends readily became apparent.

Figure 9-29 shows the dc FBSOA limits of an MTP5N40 and an MGP20N50. Even though the curves are quite similar, at either end there are significant differences. At

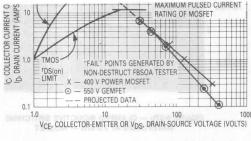


FIGURE 9-29 — COMPARISON OF FBSOA CURVES OF A 400 V MOSFET AND 550 V GEMFET OF EQUAL DIE AREA

high voltages and low currents, the GEMFET's curve begins to roll off somewhat like the curve of a bipolar that is approaching a second breakdown limitation. This is not surprising since the parasitic PNP bipolar is instrumental in sustaining its unique mode of current conduction.

At the low voltage, high current portion of the FBSOA curve, the effect of on-resistance is evidenced in two different ways. First, at very low voltages, on-resistance can limit the current. This is simply a manifestation of Ohm's Law and does not indicate a stress-related limit. As Figure 9-29 suggests, the wide difference in on-resistances between MOSFET and GEMFET is reflected in the on-resistance limit of their respective FBSOA curves. Second, a lower on-resistance also increases a device's peak-current rating by virtue of its more efficient current conduction. This limit is stress related and also is illustrated for both devices in Figure 9-29.

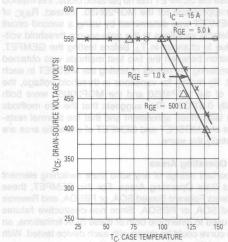


FIGURE 9-30 — EFFECT OF GATE DRIVE IMPEDANCE AND CASE TEMPERATURE ON GEMFET RBSOA

its pulsed power dissipation capability, an RBSOA derating curve is in order. In essence, an RBSOA derating indicates that a device may fail due to localized hotspotting even though its average junction temperature is within its $T_{J(max)}$ rating. Second breakdown of the MOSFET only occurs when its maximum junction temperature is exceeded. Therefore, operation of the MOSFET is only limited by its $T_{J(max)}$, I_{DM} and V_{DSS} ratings.

As for the GEMFET, special RBSOA considerations are necessary to ensure optimum reliability. Junction temperature and turn-off speed are especially noteworthy parameters since they can dramatically alter the GEMFET RBSOA capability. With all other conditions fixed, an increase in T_J can lessen the reverse-biased safe operating area if the drain current is high. At turnoff, lower gate-drive impedances are also more stressful, as explained below.

Figures 9-30 and 9-31 outline the operating limits of typical MGM20N50 (20 A, 500 V GEMFET in a TO-204 Package). The figures are typical of the devices used in this evaluation and do not represent a guaranteed RBSOA rating. A more thorough evaluation is being conducted to provide guaranteed curves for the data sheet. The gate-drive circuit used (Figure 9-32) allows adjustment of the gate-drive output impedance at turn-off simply by varying RGE.

To generate each "fail" point, a resistor, collector current and temperature were selected, then the magnitude of the clamp voltage was increased until the device either dissipated the coil's energy in avalanche or entered second breakdown. If the test device experienced a rapid collapse of its collector-emitter voltage (which is charac-

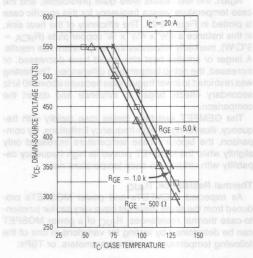


FIGURE 9-31 — EFFECT OF GATE DRIVE IMPEDANCE AND CASE TEMPERATURE ON GEMFET RBSOA



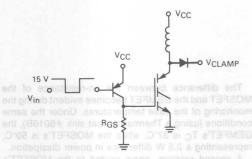


FIGURE 9-32 — GEMFET RBSOA GATE DRIVE CIRCUIT

teristic of second breakdown), the non-destruct fixture rapidly (150 ns) removed energy from the DUT before its die suffered damage.

Interestingly, the failure mechanism is not simply power related, i.e., slower switching speeds and greater crossover times tend to increase its RBSOA. This is clearly shown in the turn-off waveforms of Figures 9-33a and 9-33b. Even though the device enjoys lower switching losses with an RGE of 51 $\Omega_{\rm r}$, its RBSOA is lessened. This phenomena may be due to a very rapid MOSFET turn-off that places a dv/dt stress on the PNP bipolar.

If the GEMFET is turned off more slowly, the MOSFET carries a greater portion of the load current and lessens the strain on the bipolar during this critical portion of the switching cycle.

The GEMFET is poised to alter the options available to power circuit designers. While its slow turn-off speeds limit its potential applications at this point, the GEMFET's low rCE(on) and high input impedance make it the technology of choice for many applications requiring low frequency switching.

An Application of the GEMFET

An ideal example of a GEMFET application would highlight its three strongest features. It would require a switch with high blocking voltage capability, a large current rating and simple drive requirements. The switching element in an automotive electronic ignition control system is one of many such applications in which the GEMFET deserves consideration as an alternative to the switches currently in use. Presently, high voltage Darlingtons are the most commonly used switch in automotive ignition systems. The advantage of using a GEMFET as its replacement is the elimination of the Darlington's base drive circuitry. Since the required switching frequency is below 1.0 kHz, the GEMFET's high input impedance and low drive requirements make it ideally suited to be driven directly from CMOS logic.

When the transistor - whether it be a Darlington, GEM-FET, or Power MOSFET — turns on, the primary current ramps up to 3.0 to 7.0 A (6.0 A peak for this exercise). At turn-off, the inductive kick, or flyback voltage, is allowed to rise as high as practical to produce the very high transformer secondary voltages (20 kV) required to generate a spark. In the present systems that employ high voltage Darlingtons, voltage is often clamped to about 400 V by a zener placed from collector to base. As soon as the collector-base voltage exceeds the nominal zener voltage, the zener supplies the base current to the Darlington, turning it on and thus clamping VCE to Vz. In this mode the zener carries only a small fraction of the load current and its power dissipation rating can be sized accordingly (a collector-emitter zener must carry the full peak primary current). On the other hand, the transistor is acting as its own voltage clamp and must dissipate the energy contained in the inductive kick.

When a GEMFET is used in place of a Darlington, the same clamping scheme can be used. If the zener is placed across the drain and gate terminals, any zener avalanche current soon charges the GEMFET's input capacitance and initiates turn-on. With this clamping method, the GEMFET experiences the same high power dissipation interval as the Darlington. One additional component is needed in the GEMFET version of the clamp. A diode in series with the zener is needed to block any current that would otherwise flow if the gate were more positive than the collector [high VGF, low VCF].

Since the GEMFET performed very well in this evaluation, the question arises as to the applicability of the power MOSFET in this same circuit. Again the comparison is of the MGM20N50 and the MTM4N50, which are a GEMFET and a MOSFET of identical die size. The first consideration is that a peak drain current of 6.0 A exceeds the MOSFET's 4.0 A continuous rating. This in itself is not a problem, but thermal limitations are possible at higher duty cycles and elevated case temperatures.

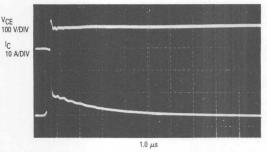


FIGURE 9-33a — CLAMPED INDUCTIVE TURN-OFF WAVEFORMS OF MGM20N50 - RGE = 51 Ω

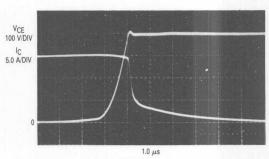


FIGURE 9-33b — CLAMPED INDUCTIVE TURN-OFF WAVEFORMS OF MGM20N50 — RGE = 510 Ω

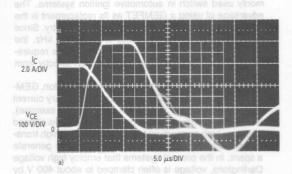


FIGURE 9-34 — AN AUTOMOTIVE ELECTRONIC IGNITION SYSTEM IS AN APPLICATION FOR WHICH THE GEMFET SHOWS GREAT PROMISE. THE SIMPLE GATE DRIVE CIRCUITRY (b) IS ONE OF THE MAJOR ADVANTAGES IN THIS SYSTEM. BECAUSE OF THE COLLECTOR-TO-GATE ZENER, CURRENT FALL TIME IS DICTATED BY THE AMOUNT OF ENERGY STORED IN THE INDUCTIVE KICK.

Although the greatest stress on the switch occurs during the clamping of the inductive kick and generation of the spark, that clamping interval does not necessarily contribute more to the average power dissipation than does the interval in which the switch is on and current ramps up in the primary. This is especially true of the power MOSFET due to its high rps(on).

The difference between the on-resistance of the MOSFET and the GEMFET becomes evident during the monitoring of the case temperatures. Under the same conditions (using a Thermalloy heat sink #6016B), the GEMFET's T_C is 37°C, while the MOSFET's is 59°C, representing a 2.5 W difference in power dissipation.

A second problem, again related to the MOSFET's higher $r_{DS(on)}$, also complicates its use in an electronic ignition control system. Due to the limited battery potential, especially during engine startup in very cold weather, the $r_{DS(on)}$ of the switch must remain low so as not to limit the peak current in the primary of the ignition coil. Therefore, the 1.5 Ω maximum specification for the MTM4N50 is probably too high for this application. In this test the "battery" voltage must be increased by about 30% to achieve the same primary current that the GEMFET conducted.

In addition to its higher on-state efficiency, the GEMFET can also offer a cost advantage over the power MOSFET. A large portion of a power transistor's cost is associated with its die area. Since the GEMFET can operate at current densities at least five times that of a high voltage MOSFET, significant savings can result from using a GEMFET with a smaller die size.

In Application of the GEMFET

An ideal example of a GEMFET application would highght its three strongest features. It would require a switch with high blocking voltage capability, a large ourrent rating and simple drive requirements. The switching element in a sutomotive electronic ignition control system is one of nany such applications in which the GEMFET deserves consideration as an alternative to the switches currently

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OURE 0-33b — CLAMPED INDUCTIVE TURN-OFF OUR PACES OF MCM20M50 — $R_{OE} = 510~\Omega$

MOTOROLA TMOS POWER MOSFET DATA

Chapter 10: Relative Efficiencies of TMOS and Other Semiconductor Power Switches TMOS and TMO

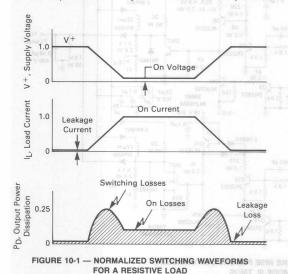
The prime requisite of a power switch (semiconductor or mechanical) is to transfer the maximum power to the load. A comparison of the relative efficiencies of various power semiconductor switches will be demonstrated with three different switching loads: resistive, inductive and a dc motor.

There are four factors that contribute to the system losses: input or driving power losses due to the input current and/or voltage required to turn on the device; saturation or static losses when the device is ON (a product of the on-voltage and current); switching or dynamic losses that result from the transition times when the device is turned ON and OFF; and off losses due to the product of leakage current and the power supply voltage. Generally off losses are by far the least significant since modern semiconductors have low leakage currents and can be ignored in system loss calculations.

The variation of input power losses can be substantial for the various semiconductors. As an example, a high voltage switching transistor would have relatively low current gain and, consequently, requires relatively high input base current to turn it fully on whereas a MOSFET, with its extremely high static input impedance, would require very little input power to turn it on.

The output power losses are illustrated in Figure 10-1. It is apparent that the switching losses, depending on the switching frequency and transition times, can contribute a large share of the total system losses. Thus, for high frequency applications, where switching losses predominate, fast switching devices should be used. Conversely, for low switching frequency applications, low on or saturation losses are more important.

Power MOSFETs are recognized as being extremely fast switching devices, but are they more efficient than bipolars in all or many switching applications? The answer is — it depends. Efficiency is a measure of dissipation,



which, in switchmode circuits, consists primarily of switching losses, both turn-off and turn-on, and saturation losses. Since switching losses are a function of the switching frequency and saturation losses are relatively constant, a point is reached in the frequency spectrum where one loss predominates over the other. Thus, in low frequency applications, devices with low saturation or onvoltage would show lower losses as measured by the device case temperature, and at high frequencies, the fast switchers would run cooler. This applies to all types of semiconductors, be they power MOSFETs, Bipolars, Darlingtons, GTO (Gate Turn Off) SCRs or a GEMFET (Gain Enhanced MOSFET) (A standard SCR can also be used wiith commutating circuitry; however, it is not included in this evaluation due to the additional circuit requirements and associated costs.) A 0.5 mode to memuo grast keep

Temperature Testing High Voltage Devices TMOS versus Bipolar Switchmode I and III

A simple way of measuring the relative efficiencies of the DUTs, one that measures the total device losses, is by measuring the case temperature. This is accomplished by attaching a thermocouple to the mounting flange of a TO-204 (TO-3) package or tab of a plastic (TO-220) package. The first evaluation was to compare the switching efficiency of three high voltage switching transistors the 2N6545, one of the first transistors characterized for switchmode applications, called Switchmode I, (SMI); the MJ16004, a state-of-the-art Switchmode III transistor (SMIII) designed for higher frequencies; and the power MOSFET MTM5N40. All these devices are of similar die size and have similar ratings (Table 1). All were tested with nearly identical loads and were driven by the same test circuit, except that the forward input current (IB1) and input resistance were scaled for the particular DUT). Reverse current or turn-off current was derived from the same input clamp transistor switch and the magnitude of this current (IB2) was dictated by the stored charge of the device under test (DUT).

Since the input drive for both turn-on and turn-off can be chosen to optimize the switching speed, the drives selected were those generally shown on the data sheet; i.e., forced gains of 5.0 and 7.0, respectively, for the 2N6545 and the MJ16004; off-bias voltages of -5.0 V and -2.0 V for the above; and a gate-drive of greater than 10 V for the MTM5N40.

Resistive loads were chosen for the temperature riseversus-frequency test since the load current could be maintained at a constant 2.5 A as the frequency was varied. Recognizing that the "real world" load is usually inductive and that inductive turn-off switching losses are greater than turn-on due to the rectangular load line, a single frequency (75 kHz) inductive test was also run. Due to the different on-voltages and turn-off times for bipolar and MOSFET devices, the load inductances had to be slightly different to achieve the same peak collector (drain)

	SMI 2N6545	SMIII MJ16004	TMOS MTM5N40 126x182 mil (22932 mil ²)		
Die Size (Area)	160x160 mil (25600 mil ²)	157x175 mil (24649 mil ²)			
IC, ID	8.0 A	5.0 A	5.0 A		
VCEO, VDSS	400 V	450 V	400 V		
VCE(sat)max, VDS(sat)max	1.5 V @ 5.0 A	2.5 V @ 3.0 A	2.5 V @ 2.5 A, rDS(on) max = 1.0 Ω		
VCE(sat)typ, VDS(sat)typ	aeil 0.3 V aidT	75 0.3 V	2.2 V @ 0.9 Ω		
hFE(min), 9fs(min)	7.0 @ 5.0 A	7.0 @ 5.0 A	2.0 mhos @ 2.5 A		

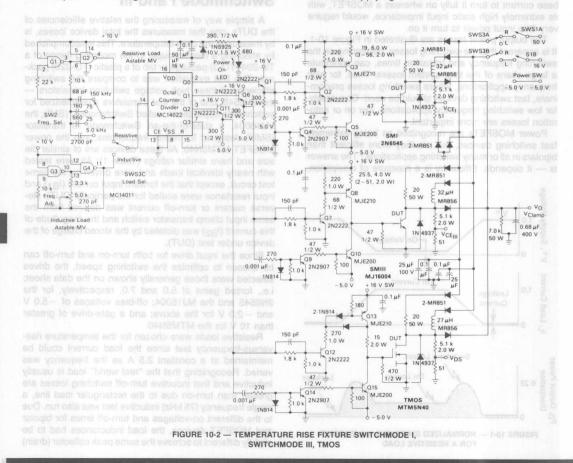
currents for a normalized test. For the 75 kHz test, the peak ramp current of about 3.0 A peak was achieved with inductances of 32 μH and 27 μH respectively when VCC and VDD were +16 V.

The temperature rise test fixture (Figure 10-2) consists of a clocked, three-phase counter sequentially driving the three respective switching circuits; thus, each device un-

frequencies (low on times), DUTs with greater storage times will effectively be powered for longer duty cycles and therefore have greater saturation losses contributing to the device temperature rise. As an example, at 150 kHz (period of 6.7 μ s) the 33% dc drive on-time of about 2.2 μ s would result in about 48% power on-time with only 1.0 μ s of storage time.

The clocks for this system, one for the resistive load case and the other for the inductive load, consist of two CMOS gate configured RC astable multivibrators. Switchable timing capacitors set the frequencies for the resistive load at 5.0, 25, 75 and 150 kHz respectively; the inductive load clock is set at a fixed frequency of 75 kHz. The output of these MV's clock the MC14002 Octal Counter Divider connected as a three-phase ring counter whose respective emitter-follower, positive-going outputs control the three virtually identical drivers.

Forward base current for the bipolar transistors is set by turning on the NPN transistors Q2 and Q7 and the following PNP transistors Q3 and Q8. To minimize storage time, Q3 and Q8 are fashioned as constant-current generators, supplying the base currents to the 2N6545



MOTOROLA TMOS POWER MOSFET DATA

(β_F = 5.0, I_{B1} = 600 mA) and MJ16004 (β_F = 7.0, I_{B1} = 430 mA) for the inductive load current of 3.0 A peak. Forward gate voltage for the power MOSFET is generated by turning on PNP transistor Q13 (Baker clamped to minimize t_s) and thereby applying nearly the full 15 V rail voltage to the gate. The 15 ohm current limiting resistor provides the low source impedance for quickly charging (and thus switching) the MOSFET input capacitance C_{iSS} .

Reverse bias voltage VBE(off) or VGS(off) for rapidly turning off the DUTs, are derived by differentiating the input pulse with the resistor-capacitor networks in the base circuits of Q4, Q9 and Q14. The resulting negative going pulses, which are coincident with the trailing edge of the input pulse, then turns on the following respective PNP transistors Q4, Q8 and Q13 for about 3.0 μ s. These transistors then turn on NPN transistors Q5, Q10 and Q15 whose emitters are referenced to a negative power supply; thus, the reverse bias voltages and resulting reverse bias currents (IB2 for bipolars) are applied to the DUT for the 3.0 µs immediately following the turn-on pulse. This reverse bias voltage can then be varied to determine its effect on switching speeds, power dissipation and case temperature rise. For the following described temperature tests the bias voltages were set for -2.0 V and -5.0 V respectively, the presumed optimum values that are listed

in the respective data sheets.

The resistive loads, being somewhat inductive wirewound resistors, have turn-on switching current rise times limited by the L/R time constant (Figure 10-3) and thus independent of input drive. However, the turn-off voltage and current switching times are affected by off-bias (Figure 10-4); thus at optimum bias voltage, the switching losses and therefore case temperature can be minimized. This is quite evident in the curves of Figure 10-5 showing temperature rise versus frequency at two off-bias voltages. All three devices showed slightly lower case temperatures (1.0 to 3.0°C) when the optimum off-bias was used at the higher frequencies where switching losses predominate.

The power MOSFET also runs cooler at higher off-bias voltage. This is due to the charged input capacitance Ciss being discharged more quickly when clamped to a greater negative voltage; thus the turn-off switching speeds are improved.

As expected at low frequencies, where on losses predominate both the 2N6545 (SMI) and the MJ16004 (SMIII) have temperature rises proportional to $V_{CE(sat)}$, both being about 0.3 V at 2.5 A. The power MOS transistor (TMOS), with a typical on-resistance $r_{DS(on)}$ of about 0.9 ohm [1.0 ohm(max)] has an on-voltage of about 2.2 V at

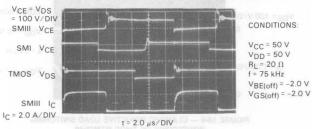


FIGURE 10-3 — RESISTIVE LOAD SWITCHING OF DUTs AT 75 kHz

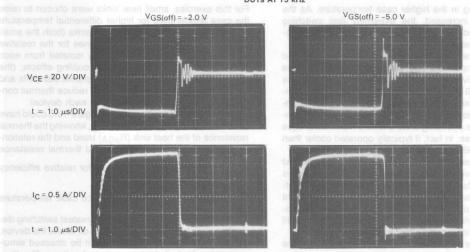
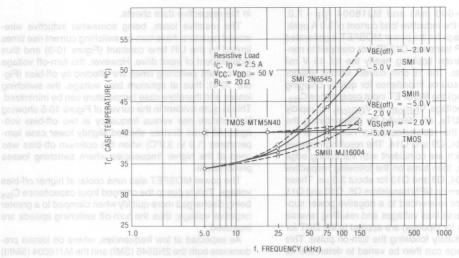


FIGURE 10-4 — RESISTIVE LOAD SWITCHING OF SWITCHMODE III
MJ16004 AT TWO OFF-BIAS VOLTAGES



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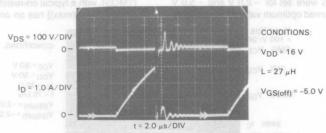


FIGURE 10-6 — CLAMPED INDUCTIVE LOAD SWITCHING WAVEFORMS OF TMOS MTM5N40

2.5 A, resulting in the higher case temperature. As the frequency is increased, the extremely fast switching MOSFET introduces little additional switching losses, resulting in a relatively constant case temperature.

The first generation SMI transistor shows the expected increasing temperature rise with increasing frequencies due to its relatively slow switching speed (the device was designed for 20 kHz applications). By contrast, the Switchmode III transistor, MJ16004, which was designed for improved operation at higher frequencies with improved reverse bias safe operating area, shows a much lower case temperature rise; in fact, it typically operated cooler than the power MOSFET up to the 75-100 kHz range.

The illustrated temperature rise curves were derived with typical devices. Testing of about ten sets of devices produced similar results, although in some cases the effects of off-bias were not as pronounced due to slight differences in device processing, temperature measurement repeatability and accuracy, particularly where small differences in temperature had to be determined.

Although the curves show defined temperatures, the magnitude of the rise is only relative as it is obviously a function of the size and efficiency of the heat sink chosen.

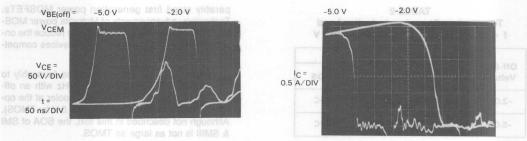
For this exercise, small heat sinks were chosen to raise the case temperature for higher differential temperature measurements. Secondly, the heat sinks (both the small ones for the DUTs and the large ones for the resistive and inductive loads) were thermally isolated from each other to minimize mutual thermal coupling effects; (the DUT heat sinks were mounted on ceramic standoffs and the load sinks on plastic washers to reduce thermal conduction to the chassis and hence to each device).

The vertical temperature axis of Figure 10-5 could have been labeled Power Dissipation (PD), knowing the thermal resistance of the heat sink (R $_{\theta}$ SA) used and the relationship between case temperature and thermal resistance

$$(P_D = \frac{T_C - T_A}{R_{\theta CS} + R_{\theta SA}})$$
. However, for relative efficiency

considerations, measuring the device case temperature will suffice.

For clamped inductive loads, the greatest switching dissipation generally occurs during turn-off where the device, due to the rectangular load line, can be stressed simultaneously with both high current and voltage. The illustrated inductive loads simulate a flyback switching regu-



Romul ent arenw absole violation FIGURE 10-7 — CLAMPED INDUCTIVE LOAD TURN-OFF SMITCHMODE I 2N6545 WITH TWO OFF-BIAS VOLTAGES

lator where the energies stored in the inductors when the DUTs are turned on are transferred via their respective clamp diodes to the resistor-capacitor load during turn-off time. By proper selection of this load, the resulting clamp voltage was set for about 250 Vdc. The actual peak collector-to-emitter voltage VCEM overshoot can be somewhat higher, being dependent on the rate of collector current fall time t_{fi}, the forward recovery time of the clamp diode and the degree of proper RF layout (Figure 9-7). It is not uncommon for this overshoot to exceed the clamp supply voltage by 100 Volts.

An example of how reverse bias affects the switching speed, and thus efficiency, of the 2N6545 is shown in the photos of Figure 10-7. Note the difference in t_S, t_{fi}, V_{CEM} and collector-emitter voltage rise time t_{rV}. At the optimum bias of about -5.0 V, the device turns off faster, there is less energy to be dissipated and a lower case temperature results. This is also true of the other two DUTs.

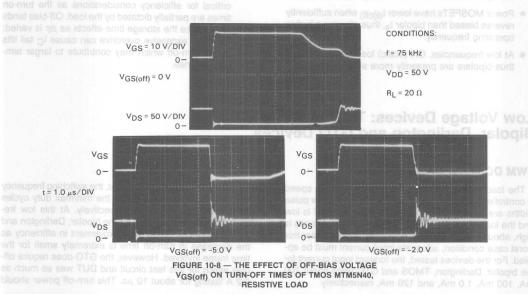
Although there is no "storage time" associated with FETs, there is a turn-off delay time t_{d(off)} due to device capacitances having to be discharged. The photos of Fig-

ure 10-8 describe the turn-off times when the off-bias is varied from 0 V, -2.0 V and -5.0 V respectively. As mentioned previously, the greater off-bias results in the lowest turn-off times.

The average temperature rise measurements of the three DUTs for the inductive load case (Table 2) illustrates the effect of off-bias on device efficiency.

A direct point-by-point comparison between the inductive load and resistive load tests at 75 kHz can't be made since the respective load currents, and thus power dissipation are not the same. However, the trends can be compared; i.e., for the inductive load test, a greater temperature differential resulted between the optimum off-bias voltage and the second tested voltage, being as high as about 15°C for SMI. By comparison, the resistive load test showed only a few degrees difference. This is due to the change in turn-off switching time having a greater effect on the more energy stressful inductive load switching than on the resistive load.

In addition to driving the bipolar devices with the recommended forced beta, β_F of about 5.0 and 7.0 respec-



	Case Temperature						
Off-Bias Voltage	SMI	SMIII	TMOS				
-2.0 V	58°C	34°C	42°C				
-5.0 V	43°C	39°C	38°C				

tively for the 2N6545 and MJ16004, a brief test was conducted by reversing β_F (7.0 and 5.0 respectively). Although the dynamic saturation characteristic of the bipolars changed subtly due to different base drive, and the turn-off switching time (even with off-bias) changed by only a second order, the change in power dissipation was minimal, if any. Within measurement repeatability, the resultant case temperatures were about the same, suggesting no great requirement of maintaining a defined β_F .

Examination of the above test results, the resistive temperature curves and the photos of the switching waveforms lead to the following conclusions about the switching efficiency of the test devices:

- The temperature rise results are a measure of total device dissipation, including the input drive loss.
- The fast switching speeds of TMOS coupled with the low drive power requirements and relatively simple drive circuitry make the MOSFET an attractive high frequency device.
 - Power MOSFETs become more efficient at frequencies beyond about 100 kHz when compared to the new generation of switchmode bipolar transistors.
 - Power MOSFETs have lower t_{d(off)} when sufficiently reverse biased than bipolar t_S, thus allowing a higher operating frequency.
 - At low frequencies, ON (static) losses predominate; thus bipolars are presently more efficient than com-

- resistance, rDS(on) to make these devices competitive with the bipolars.
- Switchmode III MJ16004 compares favorably to power MOSFET MTM5N40 at 75 kHz with an offbias of -5.0 V and generally runs cooler at the optimum bias of -2.0 V (relative to -5.0 V for TMOS).
 Although not described in this text, the SOA of SMI & SMIII is not as large as TMOS.
- For "real world" inductive loads, where the turn-off switching losses predominate, insufficient off-bias can produce higher case temperature rise for SMI transistors due to slower turn-off switching speeds (e.g., @ 75 kHz T_C = 58°C for V_{BE}(off) = -2.0 V compared with 43°C for -5.0 V).
- Optimum off-bias will reduce turn-off switching times and thus switching losses for the bipolars and FET, but does not necessarily minimize the storage time (e.g., for SMIII tfi(min) and ts(min) occur at about -2.0 V and -5.0 respectively.
- Under optimum off-bias voltage condition, the tf of SMIII approaches that of the very fast TMOS, however, drive power is high.
 - Switchmode I 2N6545 can be comparably operated to 75 kHz when there is sufficient off-bias voltage (or reverse base current), approximately -5.0 V.
- Storage time, when it is not compensated for by circuit feedback techniques, somewhat affects efficiency at high frequencies due to increased ON losses.
 - Specified force beta β_F of the bipolars are not too critical for efficiency considerations as the turn-on times are partially dictated by the load. Off-bias tends to minimize the storage time effects as β_F is varied; however, excessive overdrive can cause I_C tail lifts during turn-off which may contribute to larger temperature rise.

Low Voltage Devices: TMOS versus Bipolar, Darlington and GTO Devices

PWM DC Motor Controller Test

The load used in this test is a dc motor whose speed is controlled by PWM. Consequently, when narrow pulse widths are applied — low speed — the back emf is low and the load current (collector, drain or anode current) is high, about 11 A. To ensure device saturation under this worst case condition, adequate input current must be applied. For the devices tested, the forward input current for the bipolar, Darlington, TMOS and GTO were about 700 mA, 100 mA, 1.0 mA, and 120 mA, respectively.

Due to the motor time constant, the switching frequency was set for about 100 Hz and the min/max duty cycles were about 8% and 70% respectively. At this low frequency, the use of off-bias for the bipolar, Darlington and TMOS produces negligible improvement in efficiency as the decrease in turn-off time is extremely small for the time frame involved. However, the GTO does require off-bias which for this test circuit and DUT was as much as 2.2 A lasting for about 10 μ s. This turn-off power should

be considered in the efficiency calculations. At low frequencies, it is relatively small, but as frequency increases, it can become substantial (refer to Figure 10-10 for drive circuits and input power equations).

The bipolar, Darlington, and TMOS are turned on by the input pulse whose width is a function of the required motor speed, whereas the GTO is turned on by a relatively narrow, positive gate current pulse and turned off by a narrow, negative gate current pulse. As the frequency is increased it is apparent that the GTO input power increases and will reach a point where its input power is greater than that of the bipolar or Darlington. This crossover frequency is a function of the power supplies used and the particular duty cycle chosen. As an example, for a 50% duty cycle with the illustrated power supplies, this crossover point between the Darlington and GTO would be about 2.0 kHz.

Test Circuit Analysis

The test circuit, shown in Figure 10-9, consists of a two gate CMOS, astable multivibrator (MV) clocking a CMOS configured monostable multivibrator (MV) to produce the approximate 100 Hz, variable pulse width output. Dar-

lington transistor Q1 furnishes the buffered output to drive the two channels of the power amplifier, with transistors Q2 and Q3 supplying the positive input current to the DUT and Q4 and Q5 the negative current. When the DUT Selector Switch S1 is in positions 1, 2, or 3, the full pulse width will be applied to the DUTs as differentiating capacitor C1 is shorted out. Thus, positive input current is generated by the direct coupled pulse turning on the NPN transistor Q2 and the following PNP transistor Q3 connected, in positions 1, 2, and 4, as a constant current source. The respective emitter resistors set the current IB1 or IGT for the DUTs. Negative current is derived by differentiating the input pulse with C2, R2 and using the negative going, trailing edge pulse for turning on the following PNP transistors Q4 and NPN clamp transistor Q5. Thus, an off-bias voltage (clamped by diodes D1 and D2) is supplied to the selected DUT. If required, the off-bias can be removed by the Negative Bias Switch S2.

The GTO requires only a relatively narrow positive gate current pulse to turn it on. This pulse is derived from the differentiating network C1, R1 (switch S1A open), with the positive going, leading edge pulse turning on Q2 and Q3. For the component values shown, a turn-on, positive drive current pulse IGT of about 120 mA in amplitude and 40

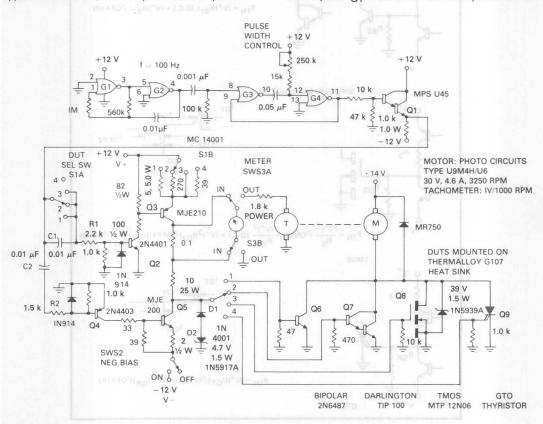


FIGURE 10-9 — TEST CIRCUIT FOR MEASURING RELATIVE EFFICIENCY OF DUT

 μs wide is generated, followed by an approximate -6.0 V, 35 μs wide turn-off voltage pulse that is coincident with the trailing edge of the input pulse. This voltage pulse produces a reverse current IGR of about 2.2 A for 10 μs (anode current of about 11 A) when the stored charge is depleted. Obviously, if no reverse bias is applied (Switch S2 open), the GTO will lose control, always being on, and the motor will run at its maximum speed.

Relative Efficiency Measurement of DUTs

In order to measure the relative efficiencies of the DUTs, both input power and output power are recorded. This is simply done by switching in a current meter to measure the average input current, or a voltmeter to measure out-

put RPM by means of a tachometer coupled to the motor. The output voltmeter, in effect, measures the relative saturation loss of the DUT since this voltage is subtracted from the applied motor voltage and, consequently, the motor speed will be indicative of this loss. Only the relative positive input current is measured as the reverse currents at this low frequency contribute very little additional drive power. However, as the power equations note in Figure 10-10, with increased operating frequency, this off-bias power can be substantial.

The relative efficiency measurements for the four DUTs are listed in Table 3. Of interest, in regard to efficiency, are the measured input currents (both pulsed and relative average), and tachometer outputs, on-voltages and case

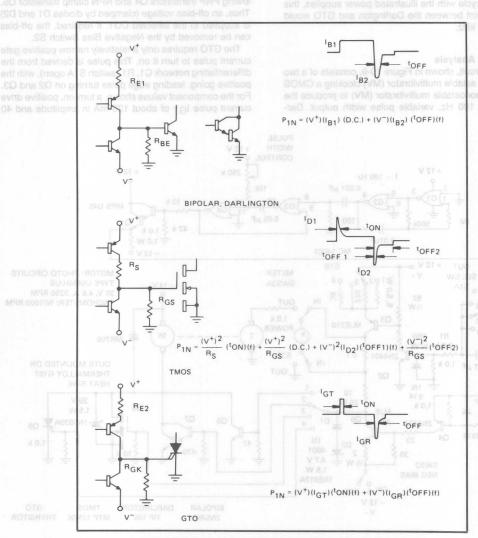


FIGURE 10-10 — DUT DRIVE AND INPUT POWER CALCULATION

temperatures. Within measurement repeatability, the DUTs with the highest on-voltage had the lowest relative output power due to reduced motor voltage and the case

temperature rise correlated with the total power dissipation (input plus output). These readings generally confirmed what was expected:

TABLE 3 — Relative Efficiency Measurement of DUTs

DUT	Bipolar 2N6487			Darlington TIP 100		TMOS** MTP12N06			GTO Thyristor				
Die Size (MIL)	110 x 130			1202			1202			1802			
Voltage Rating	60 V			60 V			60 V			300 V		001	
Current Rating	1/1/	15 A VS7- = 88			8.0 A TSMS			PAJORIE 12 A			10 A		
Switching Speeds (Relative)	111	Medium		Medium 20/0219			TM SOME Fast			Slow		08	
Input Current, (Forward/(P.W.)		700 mA			100 mA			1.0 mA			120 mA (40 μs)		
Input Current, Reverse/(P.W.)	1.0 A	1.0 A @ I _{MAX} (0.2 μs)		0.4 A @ I _{MAX} (0.1 μs)			0.2 @ I _{MAX} (0.1 μs)			2.2 @ I _{MAX} (10 μs)			
Duty Cycle	8%	12%	56%*	8%	12%	81%*	8%	12%	74%*	8%	12%	68%*	
Load Current, Peak	11 A	5.0 A	0.9 A	11 A	5.0 A	0.9 A	11 A	5.0 A	0.9 A	11 A	5.0 A	0.9 A	
Power In (Relative)	5.0	13	75	3.0	4.0	11	1.0	2.0	2.0	1.0	2.0	2.0	
Power Out (Relative)	20	59	85	16	57	84	17	59	87	17	55	84	
V _{(on)IN}	1.9 V	1.3 V	1.0 V	2.8 V	2.0 V	1.6 V	12 V	12 V	12 V	1.4 V	1.2 V	0.85 V	
V _(on) OUT	1.2 V	0.4 V	0.12 V	2.1 V	1.3 V	0.78 V	1.7 V	0.9 V	0.15 V	2.0 V	1.5 V	1.0 V	
Case Temp	36.6°C	32.9°C	38.3°C	43.6°C	41.3°C	40.4°C	42.3°C	36.0°C	29.5°C	39.5°C	41.1°C	38.2°C	

^{*}Clock varied with temperature

TMOS MTP12N06

At low frequency and low motor current, the TMOS is the most efficient device. Its input drive power is extremely low and its On voltage, due to the zero offset, relatively linear rDS(on) is low.

BIPOLAR 2N6487

The bipolar, with its low VCE(sat), has low output dissipation but its input power is the highest to satisfy high collector current — forced β conditions.

At medium and high load currents, the bipolar has the lowest On voltage followed by the TMOS with the Darlington and GTO being about equal in third place.

Efficiency as a Function of Frequency Tests

The PMW Motor Control Circuit was tested at a constant, low frequency, so the relative efficiencies measured were primarily due to static (saturation) losses. To determine the effect of the dynamic (switching) losses, which increase with increasing frequencies, the four different devices were tested with a resistive load, using a variable frequency, constant duty cycle (50%) input signal. The load current was set for about 4.0 A (VCC = 28 V, R1 \approx 7.0 Ω) and the same basic test circuit shown in Figure 9-9 was used. Most of the modifications were in the reverse bias circuit, with the off-bias voltage being either 0 V or -5.0 V for the bipolar, Darlington and TMOS tests and -12 V for the GTO.

Transistor Q4 emitter resistor (2.0 Ω) was shorted out to form an off-bias voltage source; Q3 emitter was tied to the +12 V bus to furnish drive to Q4 when VBE(off) was 0 V; and differentiating capacitor C2 was increased to 0.02 μ F to allow greater turn-off time for the GTO. Also, the bipolar forward base current was set fo 600 mA, resulting in a β F of about 7.0.

DARLINGTON TIP100

Total device dissipation and thus case temperature rise is due to input and output dissipation. The Darlington, with its high $V_{CE(sat)}$ can still have lower case temperature than the bipolar at some peak collector currents, due to its low drive power.

GTO THYRISTOR (Experimental)

The GTO is extremely efficient at low frequencies from a drive point of view since it requires only narrow turn-on and turn-off current pulses, but becomes less efficient as the frequency increases due to the higher duty cycles involved.

Test Results

The results of this efficiency versus frequency test, as measured by the case temperature rise using a small heatsink, are shown in Figure 10-11.

TMOS MTP12N06

As expected, the TMOS device ran the coolest at higher frequencies, being very constant in temperatures up to about 10 kHz and then rising slightly thereafter. At low frequencies, where static losses predominate, the TMOS MTP12N06 case temperature was only about 2°C warmer than the bipolar 2N6487, due to the respective saturation voltages of about $0.6 \text{ V (rps(on) Typ} = 0.15 \,\Omega)$ and 0.4 V. Although not shown, increasing the off-bias voltage (VGS(off)) from 0 V to -5.0 V showed only about a 2°C improvement at 33 kHz, due to slightly faster turn-off time; otherwise, at lower frequencies, the difference in turn-off time had little effect in case temperature.

Bipolar 2N6487 of manh 2OMT off or syrials

The bipolar transistor 2N6487 showed marked improve-

^{**}Data was taken on first generation TMOS devices. Later device designs give a dramatic improvement in on-state efficiency of low voltage devices



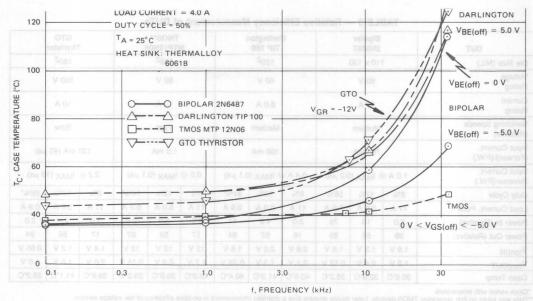


FIGURE 10-11 — TEMPERATURE RISE OF POWER SEMICONDUCTOR AS A FUNCTION OF FREQUENCY

ments in efficiency at the higher frequencies when the VBE(off) was increased from 0 V (base-emitter clamp) to $-5.0\,$ V. Without off-bias, the case temperature approached 115°C at 33 kHz, whereas, with $-5.0\,$ V, it was only about 70°C.

Darlington TIP100

The low voltage TIP100 Darlington does not have a speed-up diode across its input emitter-base resistor and thus the stored charge of the output transistor cannot be efficiently removed. Consequently, there is no improvement in case temperature at low or nominal frequencies and only some moderate improvement at 33 kHz (117°C relative to 133°C) when the off-bias was increased to -5.0 V.

The Darlington, with the highest saturation voltage of the four devices, not surprisingly, had the highest case temperature at low frequencies and, beyond 5.0 kHz, was about as inefficient as the GTO.

GTO (Experimental)

The experimental GTO exhibited static losses somewhere between the bipolar and the Darlington due to its on-voltage of about 1.2 V at 4.0 Å. The device did perform at 33 kHz, however, its case temperature rose to about 125°C. This was due to its relatively slower switching times, as shown by the oscillograms in Figure 10-12. Figure 10-12 (a), (b) and (c) show the 33 kHz waveforms of anode current, anode-cathode voltage and gate current, respectively, relative to the TMOS drain current (Figure 10-12d) and drain-source voltage (Figure 10-12e). Note

that the load current rise time is limited by the inductance of the wire-wound load resistor and that the TMOS switches much faster. Second, to ensure turn-off of the GTO at elevated temperatures, the peak reverse gate current with V_{GR} of -12 V was about 6.0 A with a pulse width of about 1.0 μ s at the 50% point.

THE GEMFET versus THE MOSFET AND BIPOLAR

The GEMFET (Gain Enhanced MOSFET) is a new power semiconductor device with a combination of characteristics that were previously unavailable to the designer of power circuitry. Closely related to the power MOSFET in structure, this device has a forward voltage drop comparable to bipolars while maintaining the high input impedance and fast turn-on of its isolated gate. While turn-on speeds are very fast, turn-off is presently relatively slow and will restrict the use of at least the first generation of these devices to lower frequency applications.

The most pronounced advantage of the GEMFET over the power MOSFET is its lower on-resistance. The rDS(on) of a high voltage MOSFET is fairly large and rises with increasing junction temperature and drain current. Conversely, the rCE(on) of a GEMFET decreases with increasing TJ and is not greatly affected by IC. Since the MOSFET does not have the GEMFET's offset voltage in its output transfer characteristics, at low currents the MOSFET on-resistance is slightly lower. However, at high currents and temperatures, the difference is dramatically in favor of the GEMFET.

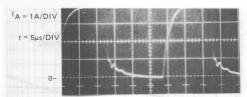


FIGURE 10-12a — GTO ANODE CURRENT

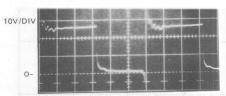


FIGURE 10-12b — GTO ANODE-CATHODE VOLTAGE

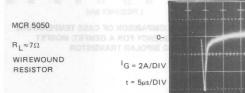


FIGURE 10-12c - GTO GATE CURRENT

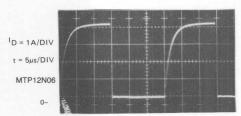


FIGURE 10-12d — TMOS DRAIN CURRENT

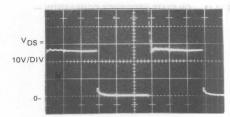


FIGURE 10-12e — TMOS DRAIN-SOURCE VOLTAGE

FIGURE 10-12 — COMPARATIVE SWITCHING OF A GTO AND TMOS AT 33 kHz

To illustrate the relative efficiencies of these two TO-220 devices — MGP20N50 GEMFET and MTP4N50 MOSFET — with that of a comparable die size, TO-220, high voltage Switchmode bipolar MJE13007, the low frequency, PWM motor controller test described in the previous section was performed. The results of a duty cycle versus case temperature rise test is shown in Figure 10-13. Note that at his low frequency test, where saturation losses predominate, the GEMFET is much more efficient than the MOSFET at low duty cycles (high motor armature currents), and even runs cooler than the bipolar device

as the pulse width increases (motor current decreases).

The second test, comparing the three devices with an inductive load at several frequencies (the inductances were changed to maintain the same peak currents for all frequencies) is illustrated in Figure 10-14. Now, at the higher frequencies, the GEMFET runs the hottest — due to its slow turn-off switching time — and the MOSFET becomes more efficient than the bipolar at about 25 kHz.

For more information on the GEMFET, please refer to Chapter 9, the Spin-off Technologies of TMOS.

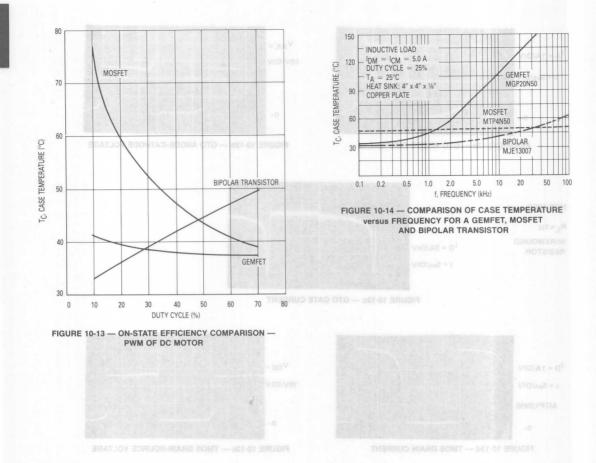


FIGURE 10-12 -- COMPARATIVE SWITCHING OF A GTO AND TIMOS AT 33 IOH

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Chapter 11: TMOS Die for Hybrid Packaging

Using TMOS Die for Hybrid Assembly

Substantial savings in weight and volume can be achieved by hybrid packaging techniques. Selected Motorola TMOS packaged devices are available in die form for custom hybrid assembly. The same advanced MOS processing techniques and silicon-gate structure available in packaged form is available in die form. The unique TMOS design utilizes thousands of source sites, interconnected in parallel, on a single die. This structure minimizes onstate voltage drop. The TMOS processing techniques result in an extremely reliable device which is highly reproducible in various die sizes.

Die Characteristics

Several die sizes are available with voltages ranging from 50 to 500 volts. All die are individually probed, at room temperature, to the dc electrical specifications of their equivalent packaged device.

Due to limitations when probing in wafer form, some of the specifications of the equivalent packaged device cannot be tested and guaranteed in die form. These parameters are safe-operating area (SOA), thermal resistance (R $_{\theta,JC}$), and on-voltage at full rated current. The above parameters depend on the assembly techniques of the individual user.

Visual Inspection of Die

All Motorola TMOS dice meet the visual inspection criteria of Mil-Standard 750B, Method 2072, with the exception of specific criteria listed below. All TMOS dice are visually screened to a 0.1% AQL level.

Die Backing

All standard TMOS dice come with Titanium-Nickel-Silver drain metallization. This metallization is suitable for solder pre-form mounting with solders such as 95/5 PbSn or 92.5/5.0/2.5 PbInAg. Commonly used header or substrate materials such as copper, nickel plated copper, gold plated molybdenum, beryllia and alumina are acceptable. The substrate material must be free of all oxides prior to assembly. Mounting is generally accomplished in a profiled belt furnace (hydrogen atmosphere is recommended). The use of solder fluxes is not recommended.

Wire Bonding

Electrical connection to the gate and source bond pads can be accomplished by ultrasonic wire bonding, using AIMg* wire having an elongation of 10%. Caution should be exercised during wire bonding to insure that the bonding footprint remains within the bonding pad area. Wire bond settings should be optimized and a wire pull test performed (see Method 2037, Mil Standard 750B) to monitor wire bond strength uniformity. Destructive sample testing and 100% non-destructive testing is recommended.

*Wire sizes of 15 mils and greater are pure Al.

Encapsulation

Before encapsulation, the assembly must be kept in a moisture free environment. I_{GSS} and $V_{GS(th)}$ are sensitive to surface moisture. For a non-hermetic package, a high grade electronic coating such as Dow Corning RTV3140 should be applied (coating is optional with a hermetic package). Before encapsulation, a 150°C two-hour bake should be performed to remove any surface moisture and any capping of hermetic packages must be performed in a dry, nitrogen atmosphere.

Handling and Shipping

TMOS Dice are available packaged several ways:

- Anti-static MultiPak Waffle type carrier with individual die package.
- Scribed and Broken Wafers Wafer on Mylar and vacuum sealed in plastic, with rejects inked.
- 3. Wafer Pak Whole wafers, with rejects inked.
- Circle Pak Whole wafer is placed on sticky film before being sawed and broken. Special equipment is needed to remove die from sticky film, with rejects inked

Upon opening the plastic container, dice should be stored in a nitrogen atmosphere to prevent oxidation of bond areas prior to assembly. All dice should be handled with teflon tipped probes to prevent any mechanical damage and the probe needles should be dipped in a conductive solution as teflon can cause ESD problems.

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Chapter 12: Characterization and Measurements

FBSOA Testing of Power MOSFETs

Power MOSFETs are essentially free of second breakdown; at least in the sense that second breakdown is defined for bipolar transistors. If second breakdown is defined as a region in which total allowable power dissipation decreases as drain-source voltage increases, the power MOSFETs do exhibit a second breakdown behavior. However, this phenomena occurs at power levels in excess of the device rating. In terms of measured safearea capabilities, power FETs commonly show higher power dissipation capability at lower voltages than they do at voltages approaching V(BR)DSS.

The phenomena which causes apparent second breakdown in FETs is similar to bipolar second breakdown in that increasing drain-source voltage widens depletion regions, allowing less of the silicon area to be used for current conduction. In FETs, higher voltages constrict the vertical channel somewhat, reducing the total area for current conduction and the maximum power dissipation capacity. Unlike bipolar transistors, there is no regenerative action associated with the current constriction. Its effects, therefore, are much less severe; so much so that FETs are generally regarded as being free of second breakdown. In general, consideration of the thermal ratings is all that is required when devices are operated within their current and voltage ratings.

To ensure that the power MOSFETs do not exhibit any limitation within the thermally limited portion of the FBSOA curve (the theoretical locus of constant power based on the thermal resistance), the DUTs were subjected to energy levels beyond the curve. As in turn-off switching SOA, a non-destruct tester would be advantageous, allowing one DUT to be used to generate a complete curve.

An important advantage of a non-destruct fixture is that it can give individual device trends and, from that, clues to the actual failure mechanism. Some have indicated that a steepening of the SOA slope at high-voltage, low-current indicates breakdown due to negative resistance effects (43,44).

The non-destruct fixture is also safer and is easier on larger power supplies. If a destructive tester were to short out a device, there is nothing to limit the current flow until the device heats to the point of opening up. This non-destruct fixture turns off the power supply and harmlessly dissipates the energy in the circuit.

Basic Theory

When a power MOSFET is operated just outside its SOA, the drain current, I_D, will suddenly increase very rapidly as the device breaks down. Unless the energy can be removed very quickly, the device will be destroyed. The basic idea of the non-destruct fixture is to sense this current surge and divert the energy from the Device Under Test as rapidly as possible. The fixture reacts within approximately 100 ns and usually saves the device.

Circuit Description A029 lautos satt breakings

The circuit performs three main functions. First, it con-

trols the desired drain-source voltage, V_{DS}, drain current, I_D, and pulse width in order to provide a defined energy to the DUT. Second, it protects the device just as it starts to fail; and third, once an overstress is detected, it removes power from the system.

The N-channel circuit is shown in Figure 12-1 and will be described. (The P-channel circuit is virtually identical except for inversion of power supplies, logic outputs and complementary transistors.) Controlled drain current is applied to the common source connected power MOSFET by means of the feedback loop around its gate-source with op-amp U1 being the error amplifier. The loop will force the source voltage (developed across the drain current sense-resistor R1) to be equal to the reference voltage that is applied to the non-inverting input of U1. The gate-source voltage will automatically assume that value required to produce the required drain current. Thus, by varying the reference voltage by means of the I_D Adjust control, a defined, accurate drain current can be chosen.

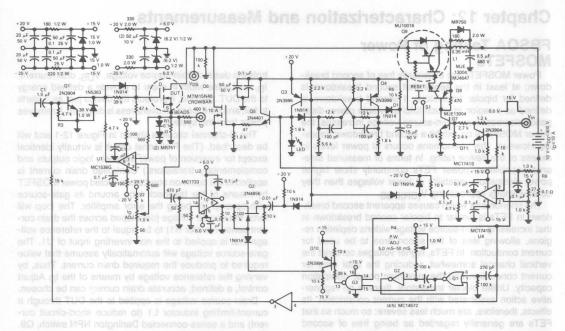
Drain-source voltage is applied to the DUT through a current-limiting inductor L1 (to reduce short-circuit current) and a series-connected Darlington NPN switch, Q9. Thus the drain voltage is approximately equal to the V_{DD} power supply (neglecting the $V_{CE(sat)}$ of Q9).

The series Darlington, configured as an emitter-follower, is controlled by level translating NPN high voltage transistor, Q7, and the following PNP high voltage transistor, Q8. Transistors Q8 and Q9 are in effect a compound Darlington and Q7 acts as a current source to minimize drive variations when VDD is varied. System operation begins by applying a positive-going pulse by means of an external pulse generator to the base of Q7, thus turning on the switched drain supply. The gate is also turned on, but is slightly delayed by the R3C1 base integrating circuit of the unclamped transistor Q1 to minimize turn-on stress on the DUT.

A fast video amplifier, U2, also monitors the DUT source, looking for a current spike. This amplifier, connected to produce a voltage gain of 200 with a bandwidth of 40 MHz, will quickly detect the advent of the destructive current spike and amplify it to a level to trigger a fast discrete R/S flip-flop.

To "lock-out" false signals that may occur due to device turn-on, an N-channel FET series switch, Q2, is connected between the video amp and the flip-flop. This FET is controlled by PNP driver, Q10, NAND Gate, G3, and input-pulse-triggered monostable multivibrator G1 and G2. Thus, by varying the Pulse Width Adjust, R4, the first 5.0 to 50 ms of the switched drain current can be blanked to prevent false triggering of the circuit.

A "true" trigger will turn on PNP transistor Q3 of the flip-flop whose output is buffered by NPN transistor Q5. The positive-going signal will then turn on the fast crowbar power MOSFET Q6, thus quickly diverting the energy from the DUT. The high level flip-flop output from Q3 will also turn on the LED — indicating a crowbar occurrence — and clamp off the input pulse generator by means of turned on transistor Q11. Consequently, Darlington Q9 is



QQV and of Jaupa visiamifigure 12-1 — N-CHANNEL POWER MOSFET NON-DESTRUCT FBSOA TESTERO JETERO III . INVOIDED IN .

also turned off. To protect the crowbar FET and Q9, which are both on for about 30 μ s due to propagation delays, current limiting inductor L1 is placed in series with the power loop.

The system is reset by depressing push-button S1, thus placing the flip-flop in the proper state. The resistor R5, capacitor C2 and diode D1 network in the base circuit of Q4 ensure that the flip-flop will be in the proper state when power is first applied.

The circuit also has over-current protection. A second current sensing resistor R6 in the return bus of the V_{DD} supply monitors the input current and activates the flipflop if more than 10 A is sensed. This is accomplished by comparator U4 and its associated pulse steering circuitry.

The P-channel fixture shown in Figure 12-2 is nearly identical to the N-channel except that it contains its own pulse generator and its supplies and transistors are inverted. The pulse generator uses a quad, two input NOR gate to produce the required astable multivibrator (A1 and A2) that clocks the following monostable multi-vibrator (A3 and A4).

Testing Mechanics and electronic beautiful design to the second s

The intended use of the FBSOA test fixture is to ensure that device operation is limited only by its specified power rating based on a measured $R_{\theta JC}$ and not a second breakdown of the parasitic bipolar transistor or any other phenomena.

To determine if the device was actually facing failure when the fixture crowbarred, V_{DS} was held constant and I_D was gradually increased with successive pulses until the fixture crowbarred. Then the crowbar was disabled and the device was pulsed again. The device would fail

indicating that the crowbar was only being activated when the device was beginning to fail.

Normally, a one second pulse was used, but other pulse durations were investigated. Time was allowed between pulses for cooling. A two second pulse did not significantly change the FBSOA curve. The device would handle about 20.0% more power during a 0.1 second pulse and the slope of the FBSOA curve remained the same (Figure 12-3).

During a 10 ms pulse, the device handled another 20.0% more power before failing. Since the blanking period lasts at least the first 5.0 ms of the 10 ms pulse, the fixture had difficulty saving units at this high energy level. The implication of this test is that the mechanism causing crowbarring is energy (time) dependent, tracking somewhat the thermal response of the device. Presumably, the junction temperature when the fixture crowbars is about the same for all pulse width variations.

Careful testing, i.e., slowly increasing the energy level, can ensure multiple crowbar activations of the DUT. One N-channel device went through 30 crowbars with no degradation in rDS(on), leakage current or drain-source breakdown voltage. Parts were either saved without degradation or destroyed, usually shorted from drain-to-source.

The case temperature of the TO-220 MTP5N20 (R $_{ heta JC}$ = 1.67°C/W), using a large finned, air cooled heat sink, rose to about 120°C when the DUT activated the crowbar. The applied power of 150 W thus produced a calculated junction temperature of about 370°C. At first glance, the Motorola parts appear to be rated with a fair amount of guardband. The actual FBSOA guardband is even larger since the rated curve assumes a case temperature of

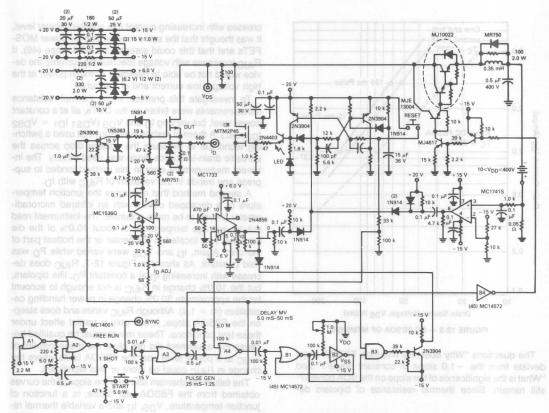


FIGURE 12-2 — P-CHANNEL POWER MOSFET NON-DESTRUCT FBSOA TESTER

25°C and the measured curve was derived at an elevated case temperature. Nevertheless, to ensure reliability, the user must operate the power MOSFET within the specified thermally limited curve.

Results of Testing One Part Along the Entire Curve

Many of the N-channel curves turned out to be very linear when plotted on log-log paper (Figures 12-3, 12-4). Within the same product line, the slope was very similar from device to device and always steeper than the $-1.0\,$ slope of the constant power dissipation curve. The plots from product line to product line also tended to be tightly clustered, with slopes varying from about -1.2 to $-1.5\,$ over the eight different lines tested.

Some have reported a steepening of the SOA curve at higher voltage and that this is due to a negative resistance phenomena. This occurs when avalanche breakdown takes place in the drain junction which increases Ip. Because of the finite resistance of the substrate, the increase in Ip causes an increase in the potential in the substrate. If Ip and the substrate resistance are large enough, the source junction can become forward biased, which would intensify the avalanche multiplication. N-channel devices with short channels are susceptible to this phenomena, but the problem can be alleviated by decreasing the sub-

strate resistance or increasing the channel length. This negative resistance effect on SOA is illustrated in Figure 12-5. The intent is to compare slopes and not to compare power handling capabilities of equivalent die sizes (43,44,45).

Testing indicates that the Motorola Power MOSFETs are not influenced by the negative resistance effect even though they utilize very short channels to decrease on-resistance. This is because of the additional $\mathsf{P}+\mathsf{plug}$ that is diffused beneath the source contact. When the device goes into avalanche breakdown, as illustrated in Figure 12-6b, the preferred avalanche current path is from N substrate through the $\mathsf{P}+\mathsf{plug}$ and into the source. This keeps the forward voltage drop of the source junction low, or below turn on. This avalanche current is quite possibly the current surge that the FBSOA tester detects when the fixture activates the crowbar.

At still higher power levels current may flow, as in Figure 12-6c, increasing the voltage in the P region. The forward voltage drop across the source junction may rise to above turn-on, establishing the negative resistance phenomena. This produces a positive feedback mechanism because the source is now injecting electrons into the substrate and thus intensifying the avalanching, effectively turning on the parasitic transistor. Such an avalanche injection would most likely destroy the device.

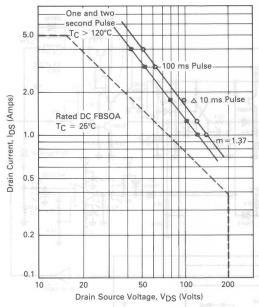


FIGURE 12-3 - DC FBSOA OF MTM5N20

The questions "Why does the empirical FBSOA slope deviate from the -1.0 slope of constant power?" and "What is the significance of the slope on the SOA curves?" still remain. Since thermal resistance of bipolars de-

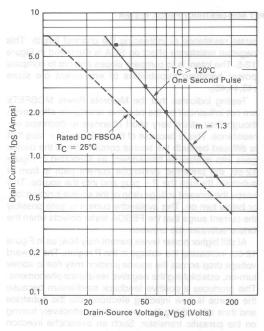


FIGURE 12-4 — DC FBSOA TEST ON MTP7N20

creases with increasing current at a constant power level, it was thought that the same may be true for power MOSFETs and that this could steepen the SOA slope (46). If $R_{\theta JC}$ increases with voltage (decreasing current), the device would not be able to dissipate as much power at the high voltage, low current end of the curve.

To investigate this premise, many thermal resistance measurements were taken on the DUTs, all at a constant power level, but varying Ip and Vps (Vps1 Ip1 = Vps2 Ip2, etc.). A thermal resistance fixture that used a switching technique to measure the voltage drop across the parasitic drain-to-source diode was used initially. The inherent measurement error in this method tended to suppress any trends in the variation of $R_{\rm BJC}$ with Ip.

A second method that measures the junction temperature of a decapped device with an infrared microradiometer proved to be more accurate. The instrument read out an average temperature of about 10.0% of the die area that was located in the center or the hottest part of the chip. Again, ID and VDS were varied while PD was held constant. As shown in Figure 12-7, R_{θJC} does decrease with increasing ID at a constant PD, like bipolars, but the 10.0% change in $R_{\theta,IC}$ is not enough to account for the approximate 30.0% change in power handling capabilities (m = 1.4). Although $R_{\theta JC}$ varies and does steepen the FBSOA slope, it has only a partial effect under these test conditions. These results must be qualified because the equipment did not allow the measurement of Rouc at a power level near the FBSOA limits where the change in $R_{\theta JC}$ could be more or less significant.

The failure mechanism and thus the slope of the curves obtained from the FBSOA test fixture, is a function of junction temperature, VDS, ID and a variable thermal resistance. Because the junction temperature rose so high, the device could be going into avalanche breakdown which would be a strong function of VDS, as the curves indicate. This temperature at failure is above TJ(max) ratings and demonstrates why users must not exceed published SOA curves.

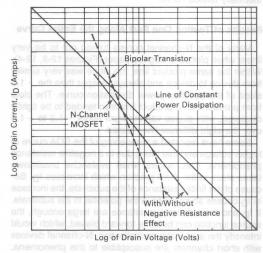


FIGURE 12-5 — COMPARISON OF TYPICAL FBSOA SLOPES

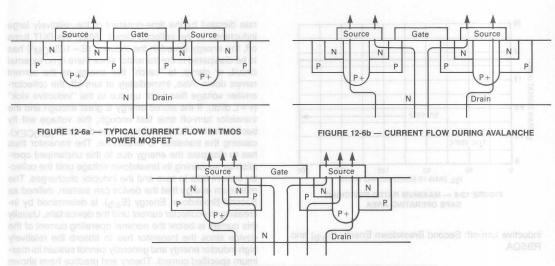


FIGURE 12-6c — CURRENT FLOW DURING NEGATIVE RESISTANCE BREAKDOWN

Since power MOSFETs or, for that matter, bipolar transistors, do change their thermal resistance as operating conditions vary, this could warrant a change in the published SOA curves. The thermally limited portion of the curve is presently based on one thermal resistance reading taken at a single operating condition. If this is a worst case reading (taken at low current, high voltage), this could significantly underrate the device at the high-current, low-voltage portion of the curve. Conversely, if the reading is taken at the high-current end, this could overrate the device at the low-current end. Further study needs to be done to determine if the change in $R_{\theta JC}$ is significant enough to alter the way manufacturers derive published SOA curves.

The significance of the slope greater than minus one, as accurately derived from the non-destruct FBSOA tester, is that a simple power limit of, say, 75 W may not be appropriate because it could overrate a device under certain conditions and underrate the same device at the same power level but lower voltage and higher current. Motorola establishes conservative derating of $R_{\theta JC}$ to ensure reliable operation under all bias conditions.

Switching Safe Operating Area (SSOA)

TURN-OFF SWITCHING SOA OF POWER MOSFETS

One of the advantages of power MOSFETs over bipolars is its superior reverse bias safe operating area (RBSOA) performance. Power MOSFET RBSOA curves are generally "square" at ID(max) and V(BR)DSS, (Figure 12-8) indicating that performance is bounded only by maximum voltage and maximum pulsed current ratings. In other words, MOSFETs are not generally RBSOA limited. There are possible exceptions to this rule, however. As noted in the dv/dt section outlined earlier in Chapter 4, rapid changes in drain-source voltages can limit the RBSOA

(turn-off switching SOA) capability of the MOSFET due to the injected current into the $C_{\rm rSS}$ capacitance inadvertently biasing-on the MOSFET.

Many practical power loads are inductive which can cause severe stress on the power switching device during turn-off. Due to the nature of an inductive load line, the switch, be it a power MOSFET or bipolar transistor, can simultaneously experience a high current and high voltage. Depending on whether the switch is unclamped (Figure 12-9a) or protected with a clamp circuit (Figure 12-9b) will determine the two energy limitations during

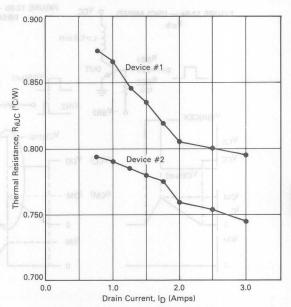


FIGURE 12-7 — THERMAL RESISTANCE OF MTM12N10 versus
DRAIN CURRENT AT PD = 50 W

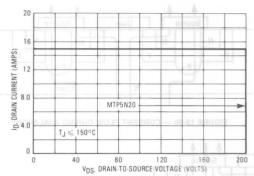


FIGURE 12-8 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

inductive turn-off: Second Breakdown Energy ($\mathsf{E}_\mathsf{S/b}$) and RRSOA

Second Breakdown Energy (E_{S/b})

Power transistors were originally characterized with an unclamped inductive load (Figure 12-9a). The Device Under Test (DUT), typically a low voltage, extremely rugged transistor, is turned on by applying a positive pulse to its base through a resistive network terminated in a reverse bias voltage VBB2. Collector current then ramps up at a

rate dictated by the time-constant of the relatively large inductance in the collector circuit. When the DUT turns off, the energy stored in the inductor $(E = 1/2LI_{CM}^2)$ has to be dissipated in the transistor since there is no external circuit, or clamp, to "catch" this energy as the current ramps down. Also, immediately at turn-off, the collectoremitter voltage flies back up due to the "inductive kick" (v = L di/dt). If the stored energy is great enough and the transistor turn-off time fast enough, this voltage will fly back to the breakdown voltage of the device (V(BR)CFX), causing the transistor to avalanche. The transistor thus has to dissipate the energy due to this unclamped operation by sustaining its breakdown voltage until the collector current falls to zero and the inductor discharges. The maximum energy that the device can sustain, defined as Second Breakdown Energy (Es/h), is determined by increasing the collector current until the device fails. Usually this current is below the nominal operating current of the device since the transistor has to absorb the relatively high inductor energy and generally cannot sustain its maximum specified current. Theory and practice have shown that most low-voltage transistors have decreasing Es/h capability with increasing reverse-bias voltage due to current crowding.

The unclamped inductive loads stress the power MOSFET in a similar manner. Now, the falling drain current will cause the flyback voltage to avalanche the drain-source of the MOSFET (V(BR)DSS).

The problem with this $E_{\rm S/b}$ rating is that the derived energy is only related to that particular inductance and is highly dependent on its Q (quality factor, i.e., series re-

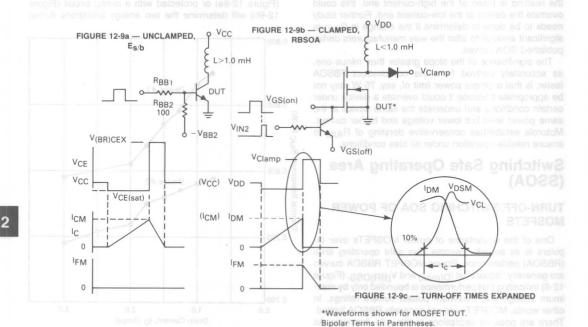


FIGURE 12-9 — INDUCTIVE LOAD SWITCHING

sistance). Additionally, the inductance specified to achieve $E_{\rm S/b}$ is generally quite large, 10 mH or greater, and does not represent the real world inductance seen in Switch-mode applications. Finally, and most important, most applications use some form of clamping to prevent drain-voltage breakdowns. For this reason, most high voltage switching transistors are specified with a clamped inductive load.

RBSOA

A more precise and definitive inductive turn-off rating is the clamped inductive turn-off rating labeled RBSOA. In the simplified test circuit of Figure 12-9b, the DUT is subjected to a real world clamped condition. The inductance need be only large enough to ensure that the flyback time is greater than the drain current fall time, generally resulting in inductances from 100 $\mu\rm H$ to 1.0 mH. These values also more accurately represent the leakage inductances encountered in switching applications.

To subject the device to the greatest stress during turn-off, the inductance should be of high Q to ensure that the peak drain current, IDM, and flyback voltage, VDSM, are simultaneously presented to the DUT, Figure 12-9c, resulting in a turn-off load line that approximates a rectangle. Under these conditions, ID will start to fall when VDS forward biases the clamp diode, at which time the stored inductor energy (current) will be transferred to the external diode circuit.

To determine the RBSOA capability of the device, I_{DM} is set to a typical operating current and the clamp voltage is increased until the transistor goes into second breakdown. Then other current levels are tested until the complete RBSOA curve is established. These second breakdown points relate to the energy dissipated in the device during turn-off, specifically the crossover time $t_{\rm C}$, (Figure 12-9c) and represents the energy encountered in inductive switching applications, (whereas, the lower $I_{\rm DM}$ for the unclamped $E_{\rm S/b}$ mode does not). Reverse biasing in this example is provided by a transistor clamp from the gate of the N-Channel MOSFET to either a negative voltage or ground.

Switching Safe Operating Area (SSOA)

The term Switching Safe Operating Area is the generalized SOA limitation during turn-on and turn-off of the power MOSFET. Turn-off switching SOA is equivalent to RBSOA for bipolar devices and will henceforth be used to describe this characteristic.

The straightforward method of determining the turn-off switching SOA is through destructively testing the power MOSFET in the clamped inductive turn-off circuit. This is accomplished by setting the drain current to a specified value by either adjusting the applied input pulse width (tpw) or the drain supply voltage V_{DD} since $I_D \equiv \frac{V_{DD} \ tpw}{}$. Then the clamp supply voltage is gradually

L control of the specified ID is less than the IDM rating, the clamp voltage can be increased until the device avalanches and begins dissipating the inductor's energy. Since the MOSFET is operating in an E_{S/D} mode at this point, failures may occur.

At drain currents greater than I_{DM}, the device is operating outside its current ratings and the MOSFET may fail at clamp voltages less than V_{(BR)DSS}. In short, the MOSFET's SSOA curves guarantee that the locus of failures is outside the I_{DM} — V_{(BR)DSS} boundaries. The SSOA curve shown in Figure 12-8 is applicable for both turn-on and turn-off of devices with switching times less than one microsecond.

Normally a destructive fixture is used to ensure that the fail points lie outside the turn-off SOA boundaries. This requires testing of many devices and device trends are difficult to determine. The use of a non-destructive fixture greatly simplifies establishing the SSOA ratings since usually only one DUT can be used to generate a complete turn-off switching SOA curve.

N-Channel Non-Destruct Turn-Off Switching SOA Test Fixture

In order to save the DUT from the normally destructive second breakdown energy, the stored inductive energy must be guickly diverted from the transistor to an external crowbar circuit. A test fixture, based on the work done at the United States National Bureau of Standards,31 was designed to have the capability of crowbarring as much as 50 A and blocking as much as 1000 V. The 10 A crowbarred propagation delay was about 70 ns and the current rise time was about 40 ns. Triggering of the crowbar was accomplished by detecting the fast rate of change of the collapsing drain-source voltage once the device went into second breakdown. Using this test fixture, a complete SOA curve can often be formed using only one DUT; consequently, the DUT must sustain as many as 30 or 40 crowbars (second breakdowns) to establish the curve. Not all devices will survive so many crowbars without degradation or failure, but a large percentage do, allowing a relatively simple and non-ambiguous curve to be generated. Degradation is measured by a relatively large change in drain leakage current, IDSS, after testing. For this magnitude of leakage current change, subsequent retesting will usually show a decrease in device turn-off SOA capability.

The main elements of the non-destruct SOA test fixture are illustrated in the block diagram of Figure 12-10. Of these blocks the most important are the Drive Circuit consisting of the $V_{GS(0n)}$ and $V_{GS(0ff)}$ Transistor Switches, the Detector/Crowbar and a Pulse Generator capable of being inhibited when crowbarring occurs. Of secondary importance are the V_{DD} Switch, and a Greater than 10% Duty Cycle Lockout circuit. Also required is an externally connected inductor, typically about 200 μ H.

Referring to Figure 12-10, the circuit operates as follows: An input pulse, V_{in}, is applied to the input of the Drive Circuit controlling the three respective switches, VGS(on), VGS(off), and VDD. The VGS(on) switch supplies the positive turn-on gate voltage and concurrent with its turn-off, the VGS(off) switch is turned on. The drain supply is also turned on (VDD switch) when positive gate voltage is applied and, to ensure proper system operation, will remain on for several microseconds (due to drive transistor storage time) after removal of the input pulse. During this on-time, the collector current ramps-up and, upon

FIGURE 12-10 — BLOCK DIAGRAM OF THE N-CHANNEL NON-DESTRUCT
TURN-OFF SWITCHING SOA TEST FIXTURE

turn-off, the drain voltage flies back. When the flyback voltage reaches the clamp voltage, the inductor current is transferred to the clamp circuit. The drain voltage will then fall at a relatively slow rate, typically a couple of hundred nanoseconds, as the energy stored in the inductor is completely discharged.

If, however, excessive energy is applied to the DUT during this switching time, the FET can go into second breakdown. Then the drain voltage falls very rapidly, possibly in less than 10 ns. When this occurs, the low R-C time-constant Differentiator detects this fast falling waveform — discriminating against the normal slow falling waveform — and produces a negative-going pulse which ultimately triggers the crowbar. The crowbar fires and the current in the DUT is quickly diverted to the crowbar, removing the turn-off energy stress from the transistor. The Pulse Generator is also disabled, preventing any successive pulses from being reapplied until the system is reset.

Drive Circuit

The drive circuit for the SOA test fixture is shown in Figure 12-11 and consists of the three aforementioned switches. A Darlington transistor, Q1, is used to buffer the CMOS-derived input pulse of 15 V from the drive circuit.

Positive gate voltage is generated by turning on the NPN transistor, Q2, with the positive going input pulse. This stage supplies drive to the PNP Baker-clamp-configured transistor, Q3, whose output feeds the gate of the DUT, turning it on.

Reverse bias is derived by differentiating the input pulse with the R1C1 network. The generated negative-going pulse, which is coincident with the trailing edge of the input pulse, then turns on PNP transistor, Q4, and the following NPN transistor, Q5.

This off-bias voltage pulse is set by R1C1 and, for the

values chosen, is about 10 μ s. Also, due to the trailing edge coincidence of the two pulses (plus approximately equal propagation delays through the two respective switches), the transition time between VGS(on) and VGS(off) can be relatively fast for some DUTs and operating conditions, approaching less than 200 ns.

The drain switch is used as a safety device, removing current from the inductor if the DUT were to fail short. This circuit utilizes two cascaded Baker-clamped monolithic Darlingtons (NPN Q6 and PNP Q7) to reach the 50 A capability of the fixture. The Baker-clamp diodes (D3, D4 and D5, D6) minimize the storage time of this switch after the DUT is turned off.

Once the DUT is turned off, the inductor-stored energy is dissipated through the two clamp diodes (D7 and D8 for high-voltage capability), the clamp supply and filter network, and Q7 clamp diode D9. Diodes D10 and D11 in the drain circuit of the DUT are used to prevent reverse drain currents from flowing and also to ensure that the crowbar saturation voltage is lower than the parasitic transistor second breakdown voltage, thus diverting the drain current.

Drain current can be monitored by the current loop as shown. Additionally, the current-sense resistor, R2, can be used to monitor I_D , but care must be taken in the layout to minimize ground loops which can distort this current replica. As in any high-speed, high-current switch, good RF techniques should be used in the layout.

Detector/Crowbar Circuit

As previously mentioned, an RC differentiator is used to discriminate between the normal V_{DS} fall time and second breakdown fall time; the components used are a 1.0 kV capacitor, C2, fixed resistor R3, and Sensitivity Control R4

Originally, the output pulse from this network fired a 25 A

SCR as a crowbar, but the turn-on time of about 600 ns proved to be too long to save the DUT. What is required is a fast latching crowbar. This is now achieved by using a common-base-connected NPN transistor, Q10, as a level detector-pulse amplifier, triggering a fast, discrete monostable multivibrator (MV) consisting of PNP transistors Q11 and Q12. This 25 μ s MV, which allows adequate time for the inductor stored energy to be dissipated, then drives the direct-coupled NPN transistor, Q13, and following PNP transistor, Q14, to a power level capable of turning on the crowbar. Diode D12 is used to block any noise

pulses on the $V_{\mbox{\scriptsize DD}}$ line from false triggering the monostable MV.

The crowbar consists of four parallel MJ10011 monolithic Darlington transistors (Q15–Q18) selected for VCEO greater than 1000 V. This transistor, designed for horizontal deflection circuits, offers the best blocking voltage-switching speed tradeoff of the several different devices tested. By using fast, wide-band transistors throughout, propagation delay and rise time of 70 ns and 40 ns, respectively, were measured at an I_C of 10 A.

Diode D13 and resistor R5 prevent possible high dv/dt

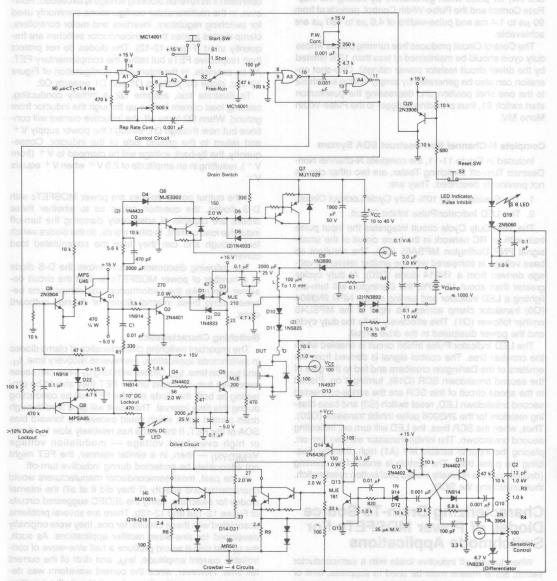


FIGURE 12-11 - N-CHANNEL POWER MOSFET NON-DESTRUCT TURN-OFF SWITCHING SOA TESTER 1000 V, 50 A

flyback voltages from falsely turning on the crowbar.

The resistor-diode networks (R6–9, D14–21) in the respective Darlington emitter circuits serve both as a ballasting-voltage clipping circuit and a crowbar indication source for the second breakdown LED indicator circuit.

Pulse Generator

The timing functions for the Non-Destruct Turn-off SOA Test Fixture are generated by a quad, 2-input NOR gate, MC14001. These gates are configured as an astable MV (gates A1 and A2) clocking a monostable MV (gates A3 and A4) for pulse-width generation. By setting the Rep-Rate Control and the Pulse-Width Control, periods of from 90 μ s to 1.4 ms and pulse-widths of 4.0 μ s to 180 μ s are achievable.

The Control Circuit produces free running pulses whose duty cycle should be maintained at less than 10% (limited by the driver circuit resistor power ratings). One-shot operation can also be generated by simply setting switch S2 to the one shot position and depressing the pushbutton start switch S1, thus providing a trigger to the Pulse-Width Mono MV.

Complete N-Channel Non-Destruct SOA System

Included in Figure 11-11, the complete N-channel Non-Destruct Turn-off Switching Tester, are two other circuits not previously described. They are:

- 1. The Greater Than 10% Duty Cycle Lockout Circuit.
- 2. The LED Indicator/Pulse Inhibit Circuit.

The 10% Duty Cycle circuit integrates the input pulse train with an RC network in the base circuit of the small-signal PNP Darlington MPSA65 (Q8). The resultant dc base voltage is compared with the emitter reference voltage derived from a 1N914 diode (D20). At duty cycles greater than about 15–20%, the Darlington will turn-on, lighting a LED indicator and turning on the NPN 2N3904 (Q9) transistor clamp across the input of the MPSU45 emitter follower (Q1). This effectively limits the duty cycle and the power dissipated in the drive circuit.

The LED Indicator/Pulse Inhibit circuit is enabled when the crowbar fires. The control signal is derived from the emitters of the Darlington crowbars and fed to the gate of the second breakdown SCR (Q19), turning it on. Placed in the anode circuit of this SCR are the series-connected second breakdown LED, reset switch (S3) and base biasing resistors for the 2N3906 pulse inhibit transistor (Q20). Thus, when the SCR fires, the LED will turn on, indicating second breakdown. The inhibit transistor will also turn on, placing the input to astable MV (A1) high, thereby disabling the pulse train. The system is enabled by opening (depressing) the normally closed pushbutton reset switch, thus unlatching the SCR.

Characterizing Drain-To-Source Diodes of Power MOSFETs For Switchmode Applications

When turning off inductive loads with a semiconductor switch, some means must be used to suppress, limit or clamp the resulting "inductive kick" from exceeding the breakdown voltage of the switch. Various types of suppressors or "snubber" circuits such as Zeners, MOVs, RC networks and clamp or "free-wheeling" diodes are generally used. The energy stored in the inductor is diverted from the transistor at turn-off and is harmlessly dissipated in the snubber, thus protecting the transistor switch.

To protect single power MOSFET switches, the snubber can be placed across either the inductor or the MOSFET. A Zener diode or RC snubber circuit can protect the drainsource of the power MOSFET but a simple clamp diode across these terminals will not, as it will only come into operation if its reverse blocking voltage is exceeded. However, in the multitransistor configurations commonly used for switching regulators, inverters and motor controllers, clamp diodes across the semiconductor switches are frequently used (Figure 12-12). The diodes do not protect their respective FETs but rather the complementary FET. As an example, in the totem-pole configuration of Figure 12-12c, diode D2 protects Q1 and D1 protects Q2.

To illustrate this, assume Q2 is initially conducting, causing load current to flow up through the inductor from ground. When Q2 turns off, the inductive current will continue but now through D1, through the power supply V+ and return to the ground side of the inductor. Consequently, the fly-back voltage will be clamped to V+ (from V-), resulting in an amplitude of 2.0 V+ when V+ equals V-

If the output power devices are power MOSFETs with D-S diodes, the question arises as to whether these diodes are capable of adequately clamping the turn-off inductive load current. In other words, do the diodes switch fast enough and can they take the commutated load current?

The following discussion characterizes the D-S diode of a number of power MOSFETs so that the circuit designer can make the performance/cost comparisons between using these internal diodes or discrete outboard ones.

Switching Characteristics

The important switching characteristics of clamp diodes in switchmode applications are reverse recovery time, t_{rr} , and turn-on time, t_{on} . Diodes with long t_{rr} times can cause excessive turn-on stress on the FET they should be protecting as both the diode and the FET will be conducting during this time interval. The result will be a feed through drain current spike which could exceed the forward bias SOA of the FET. If the diode has relatively slow t_{on} times or high overshoot voltage — modulation voltage $V_{FM(DYN)}$ — then, in a similar manner, the FET might not adequately be protected during inductive turn-off.

In the past, most semiconductor manufacturers would characterize and specify (if they did it at all) the internal diodes for switching, using the JEDEC suggested circuits of Figure 12-13a and 12-13b. There are several problems associated with these circuits; for one, they were originally developed for sine-wave rectifier applications. As such, the t_{rr} test circuit would produce a half sine-wave of controllable current amplitude, I_{FM}, and di/dt of the current fall time. However, since the current waveform was derived from a capacitor dump, tuned circuit, the resulting

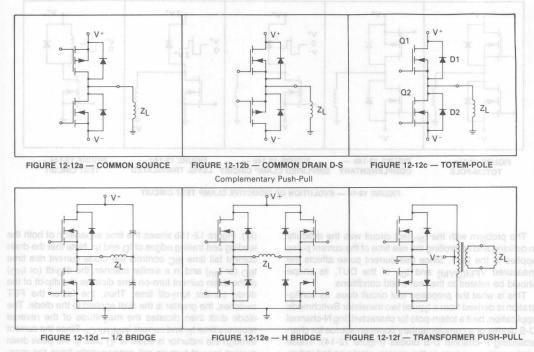
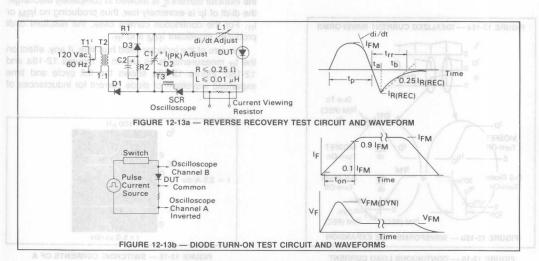


FIGURE 12-12 — MULTIPLE POWER FET DRIVE CONFIGURATIONS USING D-S DIODES

current duration t_p was dictated by I_{FM} and di/dt. Under some high di/dt conditions, t_p can become relatively short compared to the t_{rr} of the device under test (DUT) and consequently the diode is not fully turned on, thus producing inaccurate t_{rr} measurements. To ensure adequate DUT turn-on, t_p should exceed five times t_{rr} .

Second, since t_{rr} is dependent on I_{FM} and di/dt, what should these variables be set to? I_{FM} is obvious: it should be the diverted drain current, but di/dt could be anything, be it 25 A/ μ s or 100 A/ μ s, etc. In reality, this diode current turn-off time is controlled by the complementary FET turnon time



GAGE SYMBOL FIGURE 12-13 — JEDEC SUGGESTED DIODE SWITCHING TEST CIRCUITS

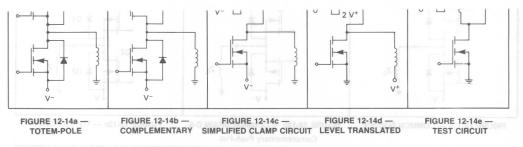


FIGURE 12-14 — EVOLUTION OF INDUCTIVE CLAMP TEST CIRCUIT

The problem with the ton test circuit was the difficulty in defining and controlling the rise time of the current pulse applied to the DUT. Since this current pulse affects the measured VFM(DYM) and ton of the DUT, its shape should be related to the real world conditions.

This is what the proposed test circuit does. Its configuration is derived from a typical two transistor Switchmode application, be it a totem-pole for characterizing N-channel D-S diodes or a complementary common source for characterizing P-channel D-S diodes (Figure 12-14). These configurations reduce to the simple, single-ended inductive clamp circuit (Figure 12-14e) whereby the clamp diode would be the D-S diode of either the N-channel FET (totem-pole) or the complementary P-channel FET.

The reverse recovery time is of greatest significance for continuous load currents common in switching inductive loads. Figure 12-15a describes the idealized current waveforms when a continuous inductive load current li is commutated between the FET (ID) and clamp diode

(IF). Figure 12-15b shows the time expansion of both the leading and trailing edges of ID and IF. Note that the drain current fall time tfIC controls the diode current rise time tfID (or ton) and in a similar manner, the dID/dt (or trID) of the drain current turn-on time dictates the dlp/dt of the diode current turn-off time. Thus, the faster the FET switches, the greater is the di/dt applied to the diode. The diode di/dt then dictates the magnitude of the reverse recovery time trr and current IRM(REC). Since the current through the inductor is equal to ID plus IF the peak drain current IDM at turn-on will consequently have the magnitude of IDM impressed on it. This is illustrated in Figure 12-16 whereby the switching times of ID and IF are the mirror image of each other; the sum of the two waveforms would yield the inductor current, whose ripple magnitude is dependent on the switching frequency and load

An example of discontinuous and continuous load current waveforms are shown in Figures 12-17a and 12-17b respectively. Note that for the discontinuous case, where the inductor current I₁ is allowed to completely discharge, the di/dt of IF is extremely low, thus producing no IRM or trr. For the continuous current case, the resultant di/dt produces significant IRM and trr.

The size of the inductor used has little, if any, effect on the trr measurements as shown in Figures 12-18a and 12-18b; Figure 12-18a shows the full cycle and time expanded waveform of diode current for inductances of

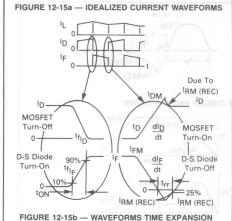


FIGURE 12-15 — CONTINUOUS LOAD CURRENT SWITCHING WAVEFORMS

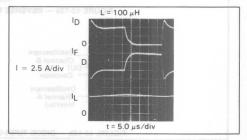


FIGURE 12-16 - SWITCHING CURRENTS OF A **CLAMPED INDUCTIVE LOAD**

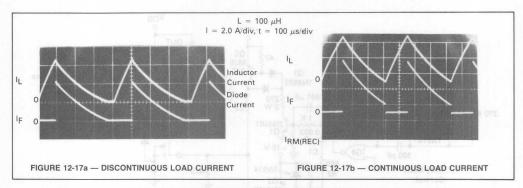


FIGURE 12-17 — THE EFFECT OF SWITCHING INDUCTIVE LOAD CURRENT ON trr AND IRM(REC) OF D-S DIODE

100 μH (air core) and Figure 12-18b for a 10 mH (iron core) inductor. The major difference is the magnitude of the ripple current, the larger inductor producing a more constant current source.

Test Circuit

The test circuit used for generating the diode switching characteristics, a translation of the "real world" circuit of Figure 12-14e, is shown in Figure 12-19. It consists of a CMOS, astable multivibrator (Gates G1 and G2) driving two parallel connected Gates 3 and 4 as a buffer. Potentiometer R1 varies the duty cycle of the approximately 25 kHz output which therefore sets the magnitude of the DUT current (along with $V_{\rm DD}$). The positive-going output from the buffer is direct-coupled to turn on the NPN transistor Q1 and the following Baker-clamped PNP transistor Q2.

To produce an off-bias to the driver, which can shape its turn-off time and consequently the diode turn-on time, the negative going edge of the output pulse from the buffer is used. Capacitor C1 and resistor R2 form a differentiating circuit to produce the negative pulse for turning on PNP

transistor Q3 and the following NPN transistor Q4. This transistor acts as the off-bias switch, applying to the driver a negative voltage pulse (approximately V $^-$) coincident with the trailing edge of the input pulse and lasting as long as the R2C1 time constant, about 5.0 μs for the component values shown.

Switching Test Results

TMOS D-S diodes are usually tested at the rated continuous drain current. The supply voltage V_{DD} should be greater than 10 V to ensure that the DUT driver is operating with typical transconductance. Since the DUT current is a function of duty cycle and/or V_{DD}, reducing the input pulse width will allow a greater V_{DD} to be used, if so required.

Although it is not always possible to test the DUT with its real world supply voltage (i.e., high voltage devices with higher $V_{\mbox{\scriptsize DD}}$ s than low voltage devices), the results would be more indicative if it were possible, since $g_{\mbox{\scriptsize fS}}$ and switching speeds will vary somewhat with $V_{\mbox{\scriptsize DD}}$.

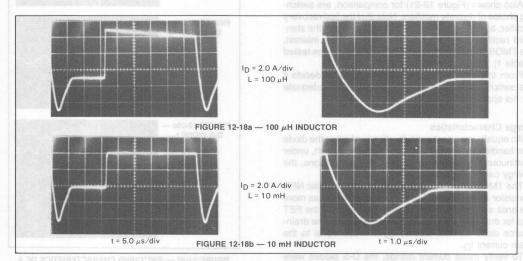
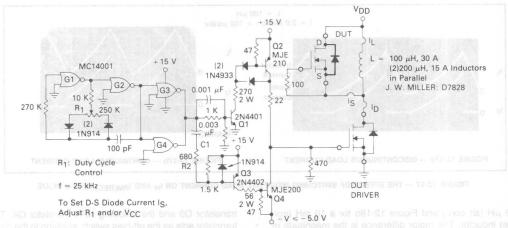


FIGURE 12-18 — THE EFFECTS OF LOAD INDUCTANCE ON D-S DIODE REVERSE RECOVERY CHARACTERISTICS



NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT

Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)

FIGURE 12-19 — TMOS D-S DIODE SWITCHING TIME TESTER

Testing of several different FETs as a function of V_{DD} showed a second order variation in t_{TT} measurements. At any rate, to ensure measurement repeatability, V_{DD} , frequency, duty cycle and inductor specification should be listed. For most of the TMOS FETs tested, the inductor was either one 200 μ H, 15 A rated air core or two in parallel (100 μ H, 30 A). Whatever the conditions, the DUT driver and diode under test should be adequately heat sunk to minimize excessive case temperature rise.

The switching characteristics of an MTM15N15 as shown in Figure 12-20, and the complete switching results for the TMOS FETs tested are compiled in Table 1.

Also shown (Figure 12-21) for comparison, are switching photos of discrete rectifiers. Note that the fast recovery rectifier, as expected, had the lowest t_{rr} and that the standard rectifier, the largest t_{rr} . But of even more interest, the TMOS D-S diode had the lowest t_{rr} of all diodes tested (Table 1).

From this data, the circuit designer can now decide if the switching characteristics of the diode are adequate for his application.

Surge Characteristics

An equally important consideration is whether the diode can handle the commutated load current in which, under continuous load current, high duty cycle conditions, the energy can be quite high.

The TMOS D-S diode is the result of the parasitic NPN transistor across the FET and as such, actually has more die area available to conduct diode current than the FET has for drain current. For data sheet purposes, the drain-source diode current, labeled I_S, is made equal to the drain current I_D.

To verify these current ratings, the D-S diodes were subjected to two different pulse width surge tests, a one

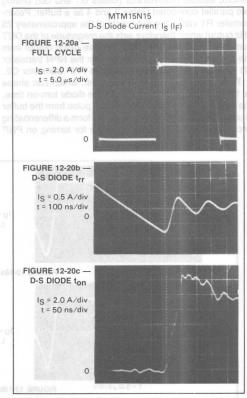


FIGURE 12-20 — SWITCHING CHARACTERISTICS OF A

TABLE 1 — Switching and Surge Current Characteristics of TMOS D-S Diodes

		Spec ID Cont (A)	Switching OMATM -						Surge Current	
	Type (Chan)		IFM (A)	di/dt (A/μs)	IRM (A)	t _{rr} (μs)	ton (μs)	300 μs 60 pps (A)	1.0 s 1 Shot (A)	
MTM8N10	N	8.0	6.0	8.5	1.0	0.20	0.20	30	11	
MTM15N06	N	15	10	9.0	1.0	0.24	0.29	80	24	
MTM15N15	N	15	10	5.0	0.8	0.28	0.05	120	19	
MTP1N60	N	1.0	1.0	8 10	0.3	2.0	0.03	25	6.0	
MTP5N06	N	5.0	5.0	3.7	0.24	0.14	0.09	50	12	
MTP25N06	N ma	25	25	10	1.0	0.20	1.0	140	35	

second, one-shot pulse and a 300 μ s, 1.8% duty cycle (60 Hz rep rate) pulse train. The one second test, which approximates a dc test, was run with the DUT bolted to a four inch square copper heat sink, initially water cooled and then in free air. The DUT forward current was then increased until the device was destroyed. The test results on one product line for the water cooled versus free air cooled were virtually identical so all subsequent tests were done in free air. The results of these tests are shown in the surge current sections of Table 1.

For power dissipation purposes and clamping efficiency determination, the typical forward characteristics of the diodes were also taken, as shown in Figure 12-22. These VF-IF curves were derived from a curve tracer using a 300 μ s current pulse at 60 PPS; the low duty cycle en-

sured low case temperature readings. For comparison purposes, Figure 12-23 describes the forward characteristics of discrete diodes under the same test conditions. Knowing the voltage drop and current, the diode dissipation can be calculated. For any combination of power dissipation, the total diode and FET dissipations should not exceed the rating of the devices. After determining the switching characteristics and the power handling capability of the diodes, a cost/performance trade-off can be made. If the switcher is in the development phase, it is relatively simple to determine the effects of using the internal monolithic diode over a discrete, outboard diode, i.e. measuring case temperature rise, current and voltage waveforms, load lines to ensure safe SOA, device and system efficiency, etc.

Diode Current I_F = 0.5 A/div. t = 1.0 μ S/div

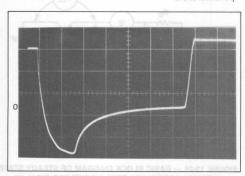


FIGURE 12-21a — 1N4001 STANDARD RECTIFIER

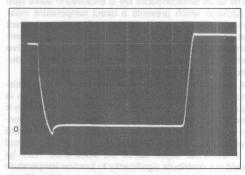
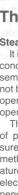


FIGURE 12-21b — 1N4935 FAST RECOVERY RECTIFIER

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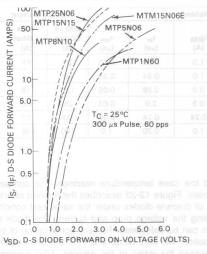


FIGURE 12-22 — FORWARD CHARACTERISTICS OF POWER MOSFET'S D-S DIODES

Thermal Measurements

Steady State Thermal Resistance Measurements

It is a well known fact that, for reliable operation of a semiconductor, junction temperature is of great concern. All semiconductor die have a critical temperature which must not be exceeded or failure will occur. Also, semiconductor operating life can be either extended or shortened by its operating temperature.

The usual semiconductor die is enclosed in some type of package which prevents a direct temperature measurement. Due to the inaccessibility of the die, an indirect method must be used to determine the junction temperature. A common method is to use a temperature sensitive electrical parameter. The parameter used can vary, depending upon the type of semiconductor measured.

A basic block diagram for steady-state thermal resistance measurements for bipolar transistors is shown in Figure 12-24. The forward biased base-emitter-junction is used as the temperature sensitive parameter. This junction is calibrated at an elevated temperature in the forward direction, with a low calibration current (I_M), and should be in the linear region above the diode knee. Also, I_M should not contribute significantly to junction temperature nor turn-on the transistor; typical values are 2.0 to 10 mA.

The calibration procedure can be performed in a temperature chamber, with the temperature set for a normal operating temperature value for the semiconductor being measured. A typical temperature for a silicon die is around 100°C. The base-emitter forward voltage is measured and recorded at I_M and at the calibration temperature.

After calibration, a power switching fixture (Figure 12-24) is used to alternately apply and interrupt the power to the test device. The transistor is operated in the active region and power dissipation can be adjusted by varying I_E and/or V_{CE} until the junction is at the calibration tem-

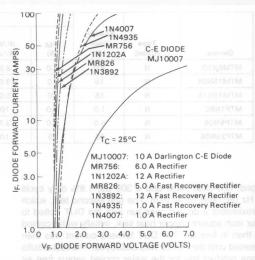


FIGURE 12-23 — FORWARD CHARACTERISTICS OF DISCRETE RECTIFIERS

perature. This condition is known by monitoring the baseemitter voltage during the time when I_M only is flowing, with either an oscilloscope or a sample-and-hold circuit. When V_{BE} is equal to the value obtained in the calibration procedure, the junction temperature is known. The case temperature is noted at this time, as well as I_E and V_{CE}.

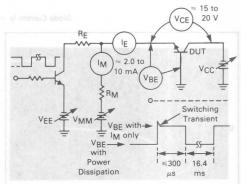


FIGURE 12-24 — BASIC BLOCK DIAGRAM OF STEADY STATE
THERMAL RESISTANCE TEST CIRCUIT FOR BIPOLAR
TRANSISTORS

The heating period is long, so the temperature of the transistor case is stabilized and the interval of power interruption short, usually 300 μ s, so junction cooling will be minimal.

The steady state thermal resistance can be easily calculated from the information obtained in the calibration and power dissipation procedures. The simple formula is derived from the basic thermal resistance model (Figure 12-25) showing the thermal to electrical analogy for a semiconductor.

Steady state thermal resistance, junction-to-case, is as follows:

$$R_{\theta JC} = \frac{T_J - T_C}{V_{CF} \times I_E}$$
 or $\frac{\Delta T}{P_D}$

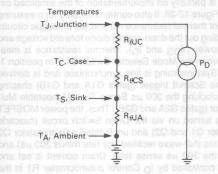


FIGURE 12-25 — BASIC THERMAL RESISTANCE MODEL SHOWING THERMAL TO ELECTRICAL ANALOGY FOR A SEMICONDUCTOR

For junction-to-case measurements, sufficient heat sinking should be provided to prevent excessive junction temperature. Measurement accuracy is improved with a large temperature delta between the junction and case. This delta can be achieved by using an efficient heat sink permitting a power dissipation (IF VCF) of sufficient magnitude to reach the calibration temperature.

Using Temperature Sensitive Parameters for Measuring Power MOSFETs Thermal Resistance

In order to determine the thermal resistance of any semiconductor device, an accurate and repeatable method of measuring the device temperature is required. The linear temperature dependence of the on-voltage of a forward biased semiconductor junction has proven to be a reliable parameter and is consequently used for bipolar transistors (emitter-base or collect-base junctions), rectifiers, zeners and thyristors. Because of their intrinsic D-S diode, this

DIODE VOLTAGE

technique is also applicable to TMOS power MOSFETs.

When measuring the thermal resistance of power MOSFETs, the gate-source threshold voltage or the drainsource on-resistance rDS(on) can be used in addition to the on-voltages of the drain-source diode. Knowing the temperature characteristics of these parameters — by measuring the voltage or resistance variations with temperature in an oven, as an example - the device temperature, when powered, can be determined and the thermal resistance can be calculated.

These temperature sensitive parameters (TSP) of a power MOSFET with their approximate temperature coefficients are listed as follows:

Drain-Source Diode $\approx -2.0 \text{ mV/}^{\circ}\text{C}$

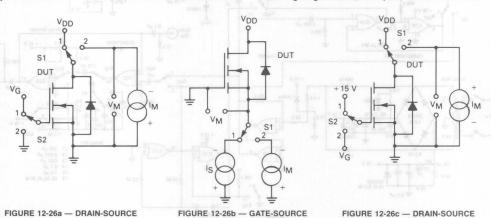
Gate-Source Threshold Voltage ≈ -2.0 to -6.0 mV/°C Drain-Source On-Resistance $\approx +7.0 \text{ m}\Omega/^{\circ}\text{C}$ when $rDS(on) = 1.0 \Omega / V = 0$ mode epubora of sulav a to se

How these TSP can be measured is described in the simplified schematics of Figure 12-26, with Figure 12-26a using the D-S diode, Figure 12-26b, the VGS(th) and Figure 12-26c, the rDS(on)-

D-S Diode TSP

Generally, the most often used circuit for measuring RAIC of power MOSFETs uses the D-S diode. When electronic switches S1 and S2 are in position 1, the FET is biased on and the heating power (VDSID) is applied to the FET for a relatively long period. Then the switches are thrown to position 2 for a short period of time (sense time) so that the FET temperature will not change appreciably. Next, the FET is turned off and a constant current IM (the same sense current at which the TSP was temperature calibrated) is applied to the forward biased D-S diode. By measuring the forward voltage drop of the diode and comparing it to the calibration curve, the FET junction temperature can be ascertained. Knowing the input power and the junction temperature, the thermal resistance can be calculated. In practice, the input power, either voltage or current, is varied until the D-S diode drop is equal to a calibration point, thus simplifying the test procedure by not having to generate a complete calibration curve.

ON RESISTANCE



THRESHOLD VOLTAGE FIGURE 12-26 — CIRCUIT CONFIGURATIONS FOR MEASURING TSP

Gate-Source Threshold Voltage TSP calls at suplanteet

This thermal resistance test circuit is extremely useful for measuring $R_{\theta JC}$ of GEMFETs since this device has no parasitic diode. As in the D-S diode tester, heating power is applied to the DUT when switch S1 is in position 1. Then, switch S1 is briefly thrown to position 2, applying the sense current to the FET (ID at VGS(th)) and the gate-source threshold voltage is measured. Input power (VDS-IS) is varied to make VGS(th) equal to the elevated temperature, calibration reading resulting in a known junction temperature and thus $R_{\theta JC}$.

Drain-Source On-Resistance volled as betall

This circuit is conceptually similar to the D-S diode tester. However, now when the switch is in position 2 (Sense Time), a positive constant current I_M and +15 V gate bias are applied to the device, turning it on. I_M should be of a value to produce about 0.5 V VDS. The voltage VDS measured (VM) is related to rDS(on) by:

$$r_{DS(on)} = V_{M}/I_{M}$$

Thermal Test Fixtures seem lanners state theady state themal Test Fixtures

D-S Diode Thermal Fixture

$R_{\theta JC}$

The D-S diode Thermal Fixture, shown in Figure 12-27, is partially an implementation of the simplified circuit of Figure 12-26. It also contains circuitry for measuring transient thermal resistance r(t) and the analogue circuits for reading out the drain-source diode forward voltage and input power (VDS and ID). Thermal resistance is measured when the Mode Selector Switch S1 is in position 1, $R_{ heta JC}$. System timing is line synchronized and is derived from the Schmitt trigger (gates G1A and G1B) shaping circuit clocking the 300 µs Sense Time Monostable Multivibrator (gates G2A and G2B). Thus, the power MOSFET DUT is turned on via the Drain Switch circuit (cascade transistor Q1 and Q2) and unclamped gate transistor Q3 for 8.0 ms (full-wave rectified line rate minus 300 μ s) and off for the 300 μs sense time. Drain current is set and readily controlled by ID Control potentiometer R1 in the gate-source, closed loop, regulator circuit (op-amp U5).

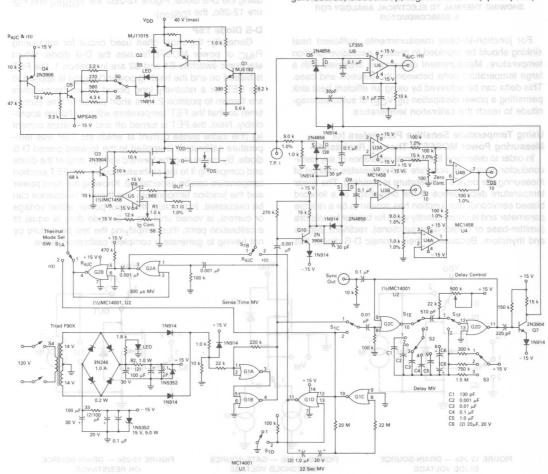


FIGURE 12-27 — POWER MOSFET D-S DIODE THERMAL FIXTURE

During the sense interval, DUT power is turned off (Q2 is off, Q3 is on) and the sense current Is is applied to the now forward biased D-S diode by means of turned on transistors Q4 and Q5. The resultant D-S diode voltage can be observed by a scope or measured by the Sample and Hold circuit consisting of series FET switch Q6, buffer amp U6, sample driver Q7 and line synchronized, Delay Monostable MV gates G2C and G2D. The Delay Control of this MV allows the sample pulse to be positioned some time after the start of the Sense time so as to measure the settled voltage of the D-S diode, ignoring the possible thermal and/or electrical switching transients on the leading edge of the sense pulse. This delay time is typically 50 μs to 150 μs .

Using similar sample-and-hold circuitry, the applied power (VDS/ $_{10}$ and ID/ $_{10}$) can be measured. This is accomplished by the respective FETs Q8 and Q9, sample driver Q10, buffer U3A and U3B and difference connected op-amps U4A and U4B.

Transient Thermal Resistance r(t)

Transient thermal resistance, r(t), is measured when switch S1 is in position 2. Now the system timing is derived by the 22 second astable MV (gates G1C and G1D) which turns the DUT on and off for about 11 seconds each. During the off time, cooling cycle, the voltage of the D-S diode can be measured at any selected period of time. This is accomplished by selecting the various resistor-capacitor timing components of the Delay MV, thus positioning the sample pulse accordingly. The six switchable capacitors, by means of Selector Switch S2, will produce the six time decades of control (100 μ s to 10 s) and the three resistors (switch S3), the multipliers within the decade, e.g., 0.2, 0.5 and 1.0.

Gate Threshold Voltage VGS(th) Thermal Fixture

The Gate-Source Threshold Voltage (V_{GS(th)}) Thermal Fixture, Figure 12-28, was specifically designed for measuring the thermal resistance of GEMFETs as this device does not have a D-S diode. Since it detects temperature

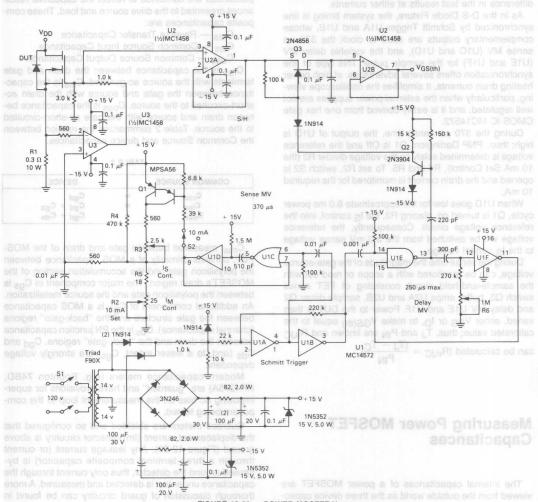


FIGURE 12-28 — POWER MOSFET VGS(th)

induced variations in the gate-source threshold voltage, it can also be used for power MOSFETs. Its line synchronization and current regulator loop around the gate and source make it very similar to D-S Diode Thermal Fixture. The major difference is the setting of the two different drain currents (or source currents), the power current, IS, and sense current IM. This is accomplished by switching two different reference voltages to the positive input of the loop regulator op-amp U3. As in any regulator loop of this type, the voltage at the negative input of the op-amp, as derived from the voltage drop across the source sense resistor R1, will be driven by the closed loop to a value equal to the reference input. Thus, if a heating current, Is, of say 10 A is required, the reference voltage should be 3.0 V (10 A x 0.3 Ω). If a sense current IM of 10 mA is specified, VRFF should be 3.0 mV.

Although most power MOSFETs are specified for a 1.0 mA drain current at VGS(th), the 10 mA level was chosen for measurement simplicity; in reality, there is negligible difference in the test results at either currents.

As in the D-S Diode Fixture, the system timing is line synchronized by Schmitt Trigger U1A and U1B, whose complementary outputs are used to clock the 370 μs sense MV (U1C and U1D), and the variable delay MV (U1E and U1F) for the sample pulse. This type of line synchronization offers several advantages: at high power heating drain currents, it simplifies the oscilloscope viewing, particularly when the external power supplies are not well regulated, and it is easily derived from one hex gate CMOS IC MC14572.

During the 370 μs sense time, the output of U1D is high; thus, PNP Darlington, Q1 is Off and the reference voltage is determined solely by the voltage divider R2 (the 10 mA Set Control), R4 and R5. To set R2, switch S2 is opened and the drain current is monitored for the required 10 mA.

When U1D goes low for the approximate 8.0 ms power cycle, Q1 is turned on, placing R3, the Is control, into the reference voltage circuit. Consequently, the reference voltage will be switched from the 3.0 mV sense voltage to the Is control voltage.

During the sense time the magnitude of the gate-source voltage, can be monitored with a scope or read out with the sample-and-hold circuit consisting of FET series switch Q3, buffer amps U2A and U2B, sample driver Q2 and delay MV U1E and U1F. Power to the DUT is then varied, either VDS or ID, to make VGS(th) equal to the calibrated value; thus, TJ and PIN are known and R $_{\theta}$ JC

can be calculated (R<sub>$$\theta$$
JC</sub> = $\frac{(T_J - T_C)}{P_{IN}}$)

1-12

Measuring Power MOSFET Capacitances

The internal capacitances of a power MOSFET are viewed from the outside world as the three device capacitances, $C_{\rm QS}$, $C_{\rm Qd}$ and $C_{\rm dS}$ (Figure 12-29).

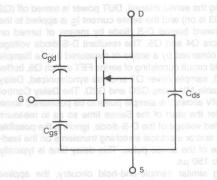


FIGURE 12-29 — DEVICE CAPACITANCES

For the Common Source configuration, the device capacitances are combined to reflect the capacitive reactances presented to the drive source and load. These composite capacitances are:

C_{rss} — Reverse Transfer Capacitance

Ciss — Common Source Input Capacitance

Coss — Common Source Output Capacitance

C_{TSS} is the capacitance between the drain and gate terminals with the source ac-guarded. C_{ISS} is the capacitance between the gate and source with the drain ac-short-circuited to the source. C_{OSS} is the capacitance between drain and source with the gate ac-short-circuited to the source. Table 2 summarizes the relation between the Common Source and device capacitances.

TABLE 2

COMMON SOURCE		DEVICE
Crss	Ī	Cgd + Cgo
Coss	RA 🚊	Cgd + Cds

 $C_{\text{rss}},$ measured between gate and drain of the MOSFET, consists primarily of a MOS capacitance between the polysilicon gate and the accumulation section of the MOSFET's drain region. The major component of C_{gs} is between the polysilicon gate and the source metallization. An additional component of C_{gs} is a MOS capacitance between the gate structure and the "back-gate" regions (channel capacitance). C_{ds} is the PN junction capacitance between the drain and the "back-gate" regions. C_{gd} and C_{ds} (and, to a lesser extent, C_{gs}) are strongly voltage dependent.

Modern capacitance meters (e.g. Boonton 74BD, HP4275A) are "guarded" and have provisions for superimposing dc bias on the measurement loop to the component being tested.

Guarded meters are shielded and so configured that the displacement current (Im) detector circuitry is above ground (Figure 12-30). Any leakage current (or current through a three-terminal composite capacitor) is bypassed around the detector, thus only current through the capacitance under test is detected and measured. A more thorough discussion of guard circuitry can be found in (1-2).

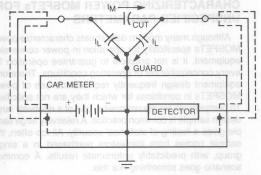


FIGURE 12-30 — "GUARDED" CAPACITANCE MEASUREMENT

A guarded arrangement is seen in Figure 12-31, the test configuration for Crss. As shown, the measurement loop encloses only Cgd. Any displacement current through Cgs or Cds is bypassed around the measurement loop; only Cgd displacement current enables the measurement circuitry. Dc bias voltage, however, may be placed in the "L" bus appearing between drain and source, and allowing measurement of Crss at various voltages.

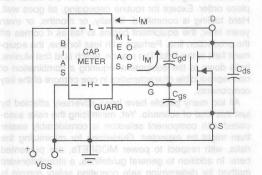


FIGURE 12-31 — Crss TEST CONFIGURATION

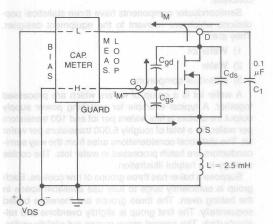


FIGURE 12-32 — Ciss TEST CONFIGURATION

To measure C_{iss} , the displacement current through C_{gs} must be included in the measurement loop. One easy way to accomplish this would be to "hard-wire" the source to the drain, however, such an arrangement would preclude measurement at any drain-source voltage other than zero. A better way is illustrated in Figure 12-32. In this arrangement the source is ac shorted to the drain by C_{1} , thus including C_{gs} in the measurement loop. RFC1 provides a dc return from ground to the source, enabling measurement of C_{iss} versus V_{DS} .

Measurement of $C_{\rm OSS}$ is similarly straightforward. The simplest way to include the $C_{\rm dS}$ displacement current in the $C_{\rm rSS}$ measurement loop is to "hard-wire" the source to the gate (Figure 12-33). Such an arrangement still allows the desirable feature of measurement at various drain-source voltages.

An inspection of the measurement configurations of Figures 12-31, 12-32 and 12-33 shows that they differ only in termination of the device source terminal. Figure 12-34 embodies Figures 12-31, 12-32 and 12-33 in one test setup. A two-pole, three position rotary switch connects the source terminal to the appropriate nodes for the three common-source capacitance measurements. The 50 k Ω resistor between gate and source insures proper termination of the MOSFET in case of capacitance meter failure. A pushbutton enables the drain-source bias voltages. P-Channel devices may be measured simply by inverting the connections of the biasing power supply.

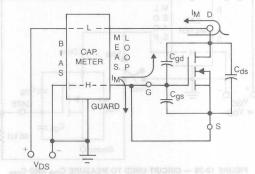


FIGURE 12-33 — Coss TEST CONFIGURATION

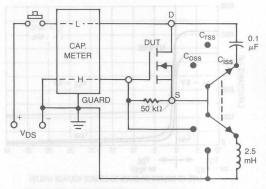


FIGURE 12-34 — COMMON SOURCE CAPACITANCE TEST SET-UP

Figure 12-35 shows a typical family of Common Source Capacitance curves derived with use of the test set-up of Figure 12-34.

For reasons detailed in Chapter 6, Figure 12-35 is not a complete picture of the variation of $C_{\rm FSS}$ and $C_{\rm iSS}$. In brief, the missing data are the changes that occur as the device moves deep into the on-state. The circuit shown in Figure 12-36 provides a means of measuring the additional capacitance variation, which is shown to the left of zero in Figure 12-37.

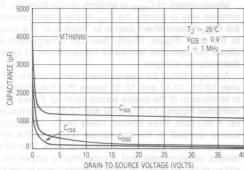


FIGURE 12-35 — C_{iss} , C_{rss} and C_{oss} variation of the MTH6N60

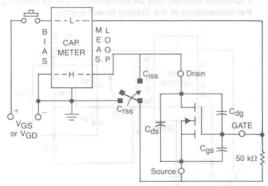


FIGURE 12-36 — CIRCUIT USED TO MEASURE C_{iss} AND C_{rss}
OF A POWER MOSFET WHEN IT IS IN OR ENTERING INTO
ITS ON-STATE

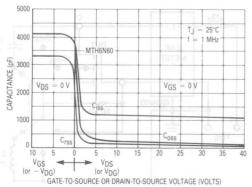


FIGURE 12-37 — COMPLETE REPRESENTATION OF CAPACITANCE VALUATION OF THE MTH6N60

CHARACTERIZING POWER MOSFETS FOR UNSPECIFIED PARAMETERS

Although many modern data sheets characterize power MOSFETs specifically for operation in power conversion equipment, it is not practical to guarantee operation for every conceivable set of operating conditions. Therefore, equipment design frequently requires the use of power MOSFETs in conditions for which they are not specified. To compensate for the unknowns, use of a relatively large design sample is common practice. A relatively large sample gives a feeling of statistical security. All too often, the sample comes from transistors purchased in a single group, with predictably unfortunate results. A common scenario goes something like this.

Design Scenario

The designer orders as many as 100 of each of the key components to try in this equipment. He may simply verify that the equipment performs satisfactorily, or he may attempt to do a worst case analysis based upon parametric variations. Either way, it is believed that the 100 pieces constitute a statistically conservative sample.

With performance and worst case analysis indicating satisfactory performance, the design is finalized. Preproduction begins with components from the initial 100 piece order. Except for routine debugging, all goes well. Hard tooling is committed. Initially, or months, or even years later, the equipment begins to fail as it comes off the production line. Perhaps with less fortune, the equipment fails in the field. The reason, which is at first elusive, boils down to the equipment requiring a combination of non-reproducible characteristics in one or more of the key components.

All too many people have been adversely affected by just this kind of scenario. Yet, minimizing the risks associated with component selection is considerably easier than might be expected. Guidelines for minimizing the risks, with respect to power MOSFETs, are presented here. In addition to general guidelines, a straightforward method for determining safe operating safety margin is highlighted. The discussion begins with statistical concepts.

Semiconductor components have three statistical populations which are relevant to the equipment designer. They are:

- 1) Wafer lot
- 2) Wafer
- 3) Individual component

A wafer lot is a group of wafers which are processed together. A typical example for switching power supply output transistors is fifty wafers per lot and 100 transistors per wafer, for a total of roughly 5,000 transistors per wafer lot. The statistical considerations arise from the way semi-conductors are batch processed in wafer lots. The cookie analogy is a helpful illustration.

Suppose a baker has three groups of raw cookies. Each group is sufficiently large to fully use available space in the baking oven. The three groups are therefore baked sequentially. The first group is slightly overdone and relatively dark. The second group comes out slightly underdone and very light. The third group turns out medium.

Lightness or darkness of the individual cookies will vary somewhat within each group, but probably not by very much. Variations in color are much more dependent upon which group a cookie was baked in than which individual cookie was chosen from a given group. A sample of cookies chosen from any one group will poorly predict the variations expected from the baking process.

Semiconductor characteristics vary in much the same way. Many characteristics are far more dependent upon the wafer lot in which a device is processed than upon which individual device is chosen from a given wafer lot. An illustration is shown in Figure 12-38.

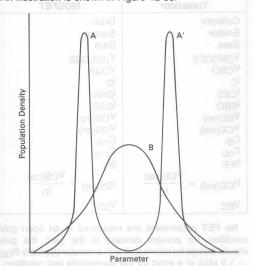


FIGURE 12-38 — EXAMPLE PROBABILITY DISTRIBUTIONS

Population densities for transistors in two different wafer lots, curves A and A', are plotted on the same scale as the wafer lot distribution for the same parameter. It is clear that a sample selected from wafer lot A will poorly predict the performance expected from transistors in lot A'. These curves are typical of the way many transistor parameters vary. They are also descriptive of batch processed components in general.

From an equipment design point of view, these characteristics have serious implications. The validity of a 100 piece design sample becomes questionable, when the possibility that all 100 devices may be from the same wafer lot is considered. In fact, the validity of using 100 devices, which are purchased all in one group, is more than questionable. For those parameters which are highly wafer lot dependent, such a sample is, in effect, not a 100 piece sample, but a one piece sample, since there is a very high probability that only one wafer lot is represented.

The unfortunate circumstances in the opening scenario are a direct result of a one piece wafer lot sample. The one piece sample does not buy much statistical insurance. Surprises are likely, since a false sense of security is generated when it is believed that 100 physical units in a design sample represent a 100 piece statistical sample. The results are predictable and unpleasant for all concerned.

Design Samples

A key factor in top notch design work is obtaining statistically relevant samples of key components. With respect to power transistors, this means including a number of different wafer lots in the design sample. This task can be seemingly difficult since, in general, the number of wafer lots in a given sample is not known. However, the minimum number of wafer lots in a sample can be determined by assuming that each date code consists of separate wafer lots. There may be many wafer lots in a date code, but usually two date codes will not contain transistors from the same wafer lot.

Often, transistors have two date codes, one which corresponds to the time period in which they are tested and the other which denotes the time period in which they were assembled. The assembly date code is by far the more valuable of the two. As an example, Motorola TO-204 transistors have a three-digit assembly date code stamped on the ear. The first digit is coded to the year. The second and third digits correspond to workweek. A transistor built in the last workweek of 1987 would read

Sample selection, then, hinges on being able to obtain transistors from a number of different date codes. Here are some suggestions.

- 1) Place several small orders sequentially in time.
- 2) Order from several different distributors, preferably in more than one geographic location. Five 20 piece shipments from five different distributors will cost more than a single shipment of 100 pieces, but the benefits dwarf the added expense.
- 3) Ask the manufacturer for assistance.

As a practical matter, it will generally be rather difficult to obtain a sample with more than four or five wafer lots represented. Since this is a relatively small sample, a working knowledge of parameter variations is very helpful. This is particularly true of Safe Operating Area (SOA) which is presented here as a special case.

Safe Operating Area

Safe Operating Area is probably the most troublesome of the unspecified parameters. Operation in unspecified regions is difficult to avoid since it is not practical to guarantee the transistor for all conditions in which it can be used. Usually, unspecified operation is related to the fact that SOA curves are drawn for given circuit configurations and bias conditions. Operation in conditions other than specified is not necessarily guaranteed. Therefore, it is often easy to operate fully within the boundaries of an SOA curve, yet be in an unspecified region because of differences in circuit configuration or bias.

At times like this, a straightforward test can be very effective. The steps are as follows:

- 1. Starting with the equipment in which the transistor will operate, or a suitable test circuit, raise the input bus voltage to 1.25 × its worst case value. Test the equipment for survivability. If any transistors in the design sample fail, there is not enough safety margin. Future trouble is almost guaranteed. If none fail, proceed to Step 2.
- 2. Raise the bus voltage to 1.33 × its worst case value.

 Repeat the testing. If more than 50% of the sample transistors survive, then SOA safety margin is probably more than adequate.

3. Recognize that worst case SOA stress, in switching power conversion systems, will often occur at conditions other than full load and high temperature. It is important to either choose conditions which maximize transistor stress, or cycle the equipment through its mini-max load and temperature ranges. Successful results will depend largely on attention to test conditions. An example is noteworthy.

SOA stress is often maximized in the first or last switching cycle, when the equipment is turned-on or turned-off. Load lines for the first or last cycle often have larger excursions than steady-state full load operation. A single excursion to a high voltage is usually more hazardous than operating at a lower voltage on a continuous basis.

These steps are very effective at eliminating unwanted surprises, provided transistors from at least three wafer lots are included in the test. They form the same basic procedure that is used to generate data sheet SOA curves.

General Guidelines with to redmon a most avotalenes

It is often of interest to obtain reasonable limits for parameters other than SOA. A discussion of expected variations is a good place to start.

Variations within a given sample are obvious. Of interest here is the expected worst case variations over the life of a multi-year production run. Table 3 gives an indication of what can generally be expected for various parameters. Measured mean values come from data taken on transistors in the design sample. They are normalized to 1.0 for ease of comparison. It is important to note that Table 3 applies only if at least three wafer lots are included in the sample data.

2) RSTA COURSE OF TABLE 3 of whether the st

Parameter	Measured Mean Value	Expected Min	Expected Max
Leakage Currents	dede1.0 21 86	10-3	10+3
Breakdown Voltages	1.0	0.7	1.5
Gain	1.0	0.5	4.0
Turn-On Delay Time	1.0	0.7	1.5
Rise Time	1.0	0.5	2.0
Turn-Off Delay Time	1.0	0.5	2.0
Fall Time	1.0	0.5	2.0
Crossover Time	1.0	0.5	2.0
Gate Threshold Voltage	1.0	0.6	1.5
rDS(on)	1.0	0.5	2.0
VDS(on)	1.0	0.5	2.0
Ciss	1.0	0.7	1.5
Coss	1.0	0.5	2.0
C _{rss}	01.0	0.6	1.6

Although some of the resulting tolerances may seem rather large, they are realistic when production runs spanning a number of years are considered. It is far better to face these numbers up front, than be surprised downstream with equipment failures.

Conclusion

The risk of equipment failure can be significantly reduced by straightforward improvements in the selection of design samples. Risks are further minimized with realistic estimation of worst case parameter variations, and the proper choice of test conditions for maximum stress.

Power MOSFET Measurement Techniques For The Curve

The curve tracer is an extremely useful tool in measuring the pertinent power MOSFET parameters. The techniques are not dissimilar to those used for measuring bipolar transistors. Table 4 lists the equivalent parameters between the two.

which individual devices TABLE from a given water lot

Transistor	MOSFET
Collector Emitter Base V(BR)CES VCBO IC ICES IEBO VBE(on) VCE(sat) Cib Cob hFE	Drain Source Gate V(BR)DSS VDGR ID IDSS IGSS VGS(th) VDS(on) Ciss Coss 9fs
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_{C}}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_{D}}$
VEC	V _{SD}

No FET parameters are measured in an open gate condition. To prevent damage to the part, the gate should always be terminated with a resistor (typically RGS = 1.0 M Ω) or a short for the appropriate test condition.

DEFINITIONS OF ELECTRICAL

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V(BR)DSS, Drain-Source Breakdown Voltage - Maximum sustaining voltage between the drain and source, measured at a specific drain current, ID; Gate shorted to

IDSS, Drain-Current With Zero Gate Voltage - Drain leakage current at a specified drain-source voltage, VDSS; Gate shorted to source.

IGSS, Gate Body Leakage Current - Gate leakage current for a specified gate-source voltage; Drain shorted to

On Characteristics VGS(th), Gate Threshold Voltage - Value of the gate voltage that must be applied to initiate conduction. It has a negative temperature coefficient of about -6.7 mV/°C.

VDS(on), Drain-Source On-Voltage - Voltage drop measured between the drain and source at a specified drain current and specified gate-source voltage.

rDS(on), Drain-Source On-Resistance — Value of the resistance measured between drain and source at a specified drain current and a specified gate-source voltage. It is defined as:

$$r_{DS(on)} = \frac{V_{DS(on)}}{I_{D}}$$

gfs, Forward Transconductance — The MOSFET gain parameter. It is the ratio between the change in drain current, I_D, for a given change in gate-source voltage, at a specified drain-source voltage and specified drain curreNt. In algebraic fOrm:

$$g_{fS} = \frac{\Delta I_D}{\Delta V_{GS}}$$

V_{SD}, Diode Forward On-Voltage — The forward voltage drop between the source and drain at a specified S-D diode current I_S.

Curve Tracer Measurements

The following explains how to measure the parameters listed above on a curve tracer. Although the set-up charts correspond to the Tektronic Type 576 Curve Tracer, the same measurements can be performed on a Tektronix Type 577 Curve Tracer.

Before applying power to MOSFETs on a curve tracer, the following precautions should be observed:

- Test stations should be protected from Electro-Static Discharge.
- 2 When inserting parts into a curve tracer, voltage should not be applied until all terminals are solidly connected in the socket.
- 3 A resistor of 100 Ω should be connected in series with the gate to damp spurious oscillations that can occur on the tracer.
- 4 When switching from one test range to another, voltage settings should be reduced to zero to avoid generation of potentially destructive voltage surges during switching.

The test set-ups to follow are for the Motorola MTP12N10 Power MOSFET, which is a 12 Amp, 100 volt N-Channel device in the TO-220 package.

 $V_{(BR)DSS}$ — Also known as BVDSS. Specified at an ID of 5.0 mA at $T_{C}=25^{\circ}C$.

Test set-up and Source Trace (See Figure 12-39).

- Set maximum peak volts on 350, Series Resistors on 3.0 k.
- 2 Polarity to NPN, Mode to Norm.
- 3 Vertical on 1.0 mA/Division, Display Offset on 0, Horizontal on 20 volts/Division.
- 4 Step Generator is not used for this measurement.
- 5 Emitter grounded; Base Term on short.
- 6 With device in socket, adjust variable collector supply until trace breaks and reaches 5.0 mA.

IDSS — Specified at 85% of rated V(BR)DSS. Maximum allowable leakage is 250 μ A at TC = 25°C.

Test Set-Up

Set-up is the same as V(BR)DSS/except:

- 1 Set Mode Switch to Leakage.
- 2 Set Vertical to 50 μ A/Division
- 3 Adjust variable collector supply to 85 volts and read leakage. If Leakage reads 0, adjust Vertical to desired level (This increases sensitivity on low leakage devices).

 I_{GSS} — Specified at $V_{GS}=\pm 20$ volts, maximum allowable leakage is 500 nA at $T_{C}-25^{\circ}C$.

Test Set-Up

- 1 Drain and gate connections on socket are reversed so drain is shorted to source.
- 2 Set maximum peak volts to 75, and Series Resistors to 140 Ω_{\star}
- 3 Polarity to NPN and Mode Switch to Leakage.
- Vertical on 50 nA/Division, Display Offset on 0, Horizontal on 2.0 Volts/Division.
- 5 Step generator is not used for this measurement.
- 6 Emitter grounded; Base Term on short.
- 7 With device in socket, adjust variable collector supply to 20 volts and read Leakage. If leakage reads 0, adjust vertical to desired level.

 $V_{GS(th)}$ — Specified at 1.0 mA with limits of 2.0 volts minimum and 4.5 volts maximum at $T_{C}=25^{\circ}C$.

(Figure 12-40)

- 1 Set Maximum Peak Volts to 15, Series Resistors to 0.3 Ω .
- 2 Polarity to NPN, Mode Switch on Normal.
- 3 Vertical on 0.2 mA/Division, Display Offset on 0, Horizontal on 2.0 Volts/Division.
- 4 Step Generator; number of steps = 1, Offset Mult on 0, Offset on Aid, Steps Button in, Step Family on Single, Rate on Norm, Step offset amplitude = 1.0 V.
- 5 Emitter grounded: Base Term on Step Generator.
- 6 With device in socket, adjust variable collector supply to 10 volts, then adjust Offset Mult until trace reaches 1.0 mA. Read V_{GS}(th) directly from Offset Mult Control.

 $V_{DS(on)}$ — Specified at $V_{GS}=10$ volts and at one half rated I_D . $r_{DS(on)}$ is calculated from measured $V_{DS(on)}$ value.

(Figure 12-41)

- 1 Set Maximum Peak Volts on 15, Series Resistors on 0.3 Ω .
- 2 Polarity on NPN, Mode to Norm.
- 3 Vertical on 1.0 A/Division, Display Offset on 0, Horizontal on 0.5 Volts/Division.
- 4 Step Generator; number of steps 10, Offset on zero, pulsed steps on 300 μs, Step Family on Rep, rate on Norm, Step Offset/Amplitude = 1.0 V.
- 5 Emitter grounded; Base Term on Step Gen.
- 6 With device in socket, adjust variable collector supply until the top left dot on trace reaches 6.0 Amps then read V_{DS(on)} off horizontal scale.

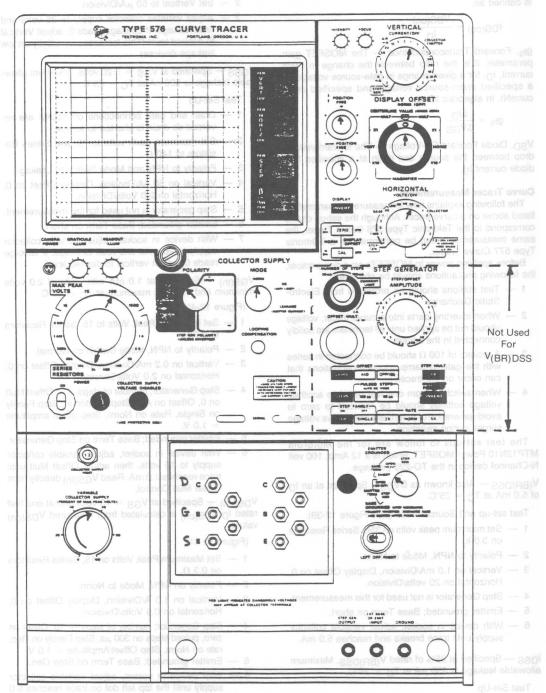


FIGURE 12-39 - TEST SET-UP CHART TYPE 576 FOR MEASURING POWER MOSFET PARAMETERS

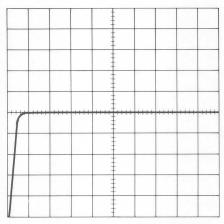


FIGURE 12-40 — CURVE TRACER PRESENTATION FOR VGS(th) - MTP12N10

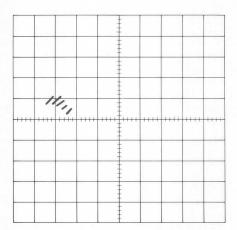


FIGURE 12-41 — CURVE TRACER PRESENTATION FOR VDS(on)

gfs - Specified at one half rated ID at VDS = 15 volts. (Figure 12-42)

- 1 Maximum Peak Volts on 15, Series Resistors on 0.3Ω .
- 2 Polarity on NPN, Mode to Norm.
- 3 Vertical on 1.0 Amp/Division/Display Offset on zero, Horizontal on 2.0 Volts/Division.
- 4 'Step Generator; number of steps = 10, Offset on zero, Pulsed Steps on 300 µs, Step Family on Rep, rate on Norm, Step Offset Amplitude - 1.0 V.
- 5 Emitter grounded; Base Term on Step Gen.
- 6 Readout illum turned fully clockwise.
- 7 With device in socket, adjust variable collector supply until trace with steps closest to 6.0 Amps reaches 15 volts. gfs is the number of divisions between those two steps, as designated by the right hand corner of the screen labeled gm per Division.

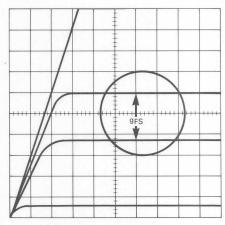


FIGURE 12-42 — CURVE TRACER FOR gfs

 V_{SD} — Specified at rated I_D with $V_{GS} = 0$.

(Figure 12-43)

- 1 Set Maximum Peak Volts on 15 and Series Resistors on 0.3 Ω .
- 2 Polarity on PNP, Mode on Norm.
- 3 Vertical on 2.0 Amps/Division, Display Offset on 0, Horizontal on 0.5 Volts/Division.
- 4 Push Display Invert in.
- 5 Step Generator is not used for this measurement.
- 6 With device in socket, adjust variable collector supply until trace reaches 12 Amps and read voltage.

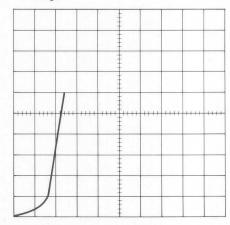
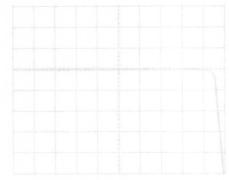


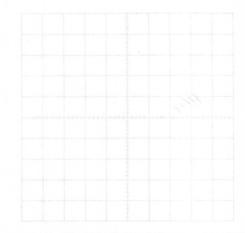
FIGURE 12-43 — CURVE TRACER PRESENTATION FOR VSD

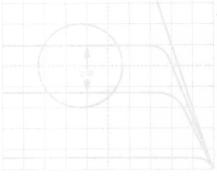
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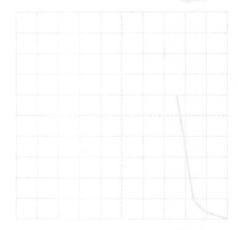
- 1. Fink, Electronic Engineers' Handbook, 1 ed 1975, McGraw Hill, pp17-31 to 17-32.
- 2. Henny, Radio Engineering Handbook, 5 ed, 1959, McGraw Hill, pp14-36 to 14-37.

Additional Reference Material: Measurement Concepts From Tektronix.









MOTOROLA TMOS POWER MOSFET DATA

Chapter 13: Reliability and Quality and Supplied to the beautiful and supplied to the chapter in the chapter in

Introduction

In today's semiconductor marketplace two important elements for the success of a company are product quality and reliability. Both are interrelated — reliability is the quality extended over the expected life of the product. For any manufacturer to remain in business, their products must meet and/or exceed the basic quality and reliability standards. Motorola, as a semiconductor supplier, has successfully achieved these standards by supplying product for the most strenuous applications to perform in the most adverse environments.

It is recognized that the best way to accomplish an assured quality performance is by moving away from the previous methods of "testing in" quality and embracing the newer concept of "building in" quality. At Motorola, we use a twofold approach toward reaching the ultimately achievable level of quality and reliability. First, we develop and implement a process that is inherently reliable. Then we exercise meticulous care in adhering to the specifications of the process every step of the way — from start to finish. This allows the development and application of inspections and procedures that will uncover potentially hidden failure modes. It is this dedication to long-term reliability that will ultimately lead to the manufacture of the "perfect product."

Motorola approaches the ideal in TMOS product reliability by instigating a four-step program of quality and reliability:

- 1. Stringent in-process controls and inspections.
- 2. Thoroughly evaluated designs and materials.
- Process average testing, including 100% QA redundant testing.
- Ongoing reliability verifications through audits and reliability studies.

These quality and reliability procedures, coupled with rigorous incoming inspections and outgoing quality control inspections add up to a product with quality built in — from raw silicon to delivered service.

Reliability Tests "1990" as viscontable extents

Motorola TMOS products are subjected to a series of extensive reliability tests to verify conformance. These tests are designed to accelerate the failure mechanisms encountered in practical applications, thereby ensuring satisfactory reliable performance in "real world" applications.

The following describes the reliability tests that are routinely performed on Motorola's TMOS devices.

High Temperature Reverse Bias (HTRB) Per MIL-STD-750, Method 1039:

The HTRB test is designed to check the stability of the device under "reverse bias" conditions of the main blocking junction at high temperature, as a function of time.

The stability and leakage current over a period of time, for a given temperature and voltage applied across the junction, is indicative of junction surface stability. It is therefore a good indicator of device quality and reliability.

For TMOS devices, voltage is applied between the drain and source with the gate shorted to the source. IDSS, V(BR)DSS, IGSS, VGS(th), and VDS(on) are the dc parameters monitored. A failure will occur when the leakage achieves such a high level that the power dissipation causes the devices to go into a thermal runaway. The leakage current of a stable device should remain relatively constant, only increasing slightly over the testing period.

Typical conditions:

V_{DS} = 100% of maximum V_{DS} rating

 $V_{GS} = 0$ (shorted)

 $T_A = 150^{\circ}C$

Duration: 1000 hrs for qualification

High Temperature Gate Bias (HTGB): Per MIL-STD-750, Method 1039:

The HTGB test is designed to electrically stress the gate oxide at the maximum rated dc bias voltage at high temperature. The test is designed to detect for drift caused by random oxide defects and ionic oxide contamination.

For TMOS devices, voltage is applied between the gate and source with the drain shorted to the source. IGSS, VGS(th), and VDS(on) are the dc parameters monitored. Any oxide defects will lead to early device failures.

Typical conditions:

 $V_{GS} = \pm 20 V$

VDS = 0 (shorted) (pniloy0 town9 to JOI)

 $T_A = 150^{\circ}C$

Duration: 1000 hrs for qualification

High Temperature Storage Life (HTSL) Test: Per MIL-STD-750, Method 1032.

The HTSL test is designed to indicate the stability of the devices, their potential to withstand high temperatures and the internal manufacturing integrity of the package. Although devices are not exposed to such extreme high temperatures in the field, the purpose of this test is to accelerate any failure mechanisms that could occur during long periods at storage temperatures.

The test is performed by placing the devices in a mesh basket, then placed in a high temperature chamber at a controlled ambient temperature, as a function of time.

Typical conditions:

T_A = 150°C on Plastic package Duration: 1000 hrs for qualification

High Humidity High Temperature Reverse Bias of 10 (H³TRB) Test: Per MIL-STD-750, Method 1039.

The H³TRB test is designed to determine the resistance of component parts and constituent materials to the combined deteriorative effects of prolonged operation in a high temperature/high humidity environment. This test only applies to nonhermetic devices.

Humidity has been a traditional enemy of semiconductors, particularly plastic packaged devices. Most moisture related degradations result, directly or indirectly, from penetration of moisture vapor through passivating materials,

and from surface corrosion. At Motorola, this former problem has been effectively addressed and controlled through use of junction "passivation" process, die coating, and proper selection of package materials.

Typical conditions:

 $V_{DS} = 100\%$ of maximum V_{DS} rating up to 200 V

VGS = 0 (shorted) bns (m)80V 880I 880(88)V

 $T_A = 85^{\circ}C$ RH = 85%

Duration: 1000 hrs for qualification

Autoclave Test (Pressure Cooker).

The Autoclave Test is designed to determine the moisture resistance of devices by subjecting them to high steam pressure levels. This test is only performed on plastic/epoxy encapsulated devices and not on hermetic packages (i.e., metal can devices). Within the pressure cooker a wire mesh tray is constructed inside to keep the devices approximately two inches above the surface of deionized water and to prevent condensed water from collecting on them. After achieving the proper temperature and atmospheric pressure, these test conditions are maintained for a minimum of 24 hours. The devices are then removed and air dried. Parameters that are usually monitored are leakage currents and voltage.

Typical Conditions: alnoi bus stosleb shixo mobust vd

TA = 121°C d belique is applied b 2°121 = TA

PE= 14.7 psi II of betrorts nish erit ritiw ecruos bna

Veschi), and Vescon) are the do parami %001 = HR

Duration: 72 hrs for qualification liw alosisb sboto yn/

Intermittent Operating Life: (IOL or Power Cycling) Per MIL-STD-750, Method 1037.

The purpose of the IOL test is to determine the integrity of the chip and/or package assembly by cycling on (device thermally heated due to power dissipation) and cycling off (device thermally cooling due to removal of power applied) as is normally experienced in a "real world" environment.

DC power is applied to the device until the desired function temperature is reached. The power is then switched off, and forced air cooling applied until the junction temperature decreases to ambient temperature.

$$\Delta T_J = \Delta T_C + R_{\theta JC}Pd$$

$$\Delta T_J = 100^{\circ}C$$
(typically, which is an accelerated condition)
$$\Delta T_C = T_C HIGH - T_C LOW$$

The sequence is repeated for the specified number of cycles. The temperature excursion is carefully maintained for repeatability of results.

The Intermittent Operating Life test indicates the degree of thermal fatigue of the die bond interface between the chip and the mounting surface and between the chip and the wire bond interface. In a bandisab at test BRTCH and

For TMOS devices, parameters used to monitor performance are thermal resistance, threshold voltage, onresistance, gate-source leakage current and drain-source leakage current.

A failure occurs when thermal fatigue causes the thermal resistance or the on-resistance to increase beyond the maximum value specified by the manufacturer's data Typical conditions:

VDS ≥ 10 V

 $\Delta T_{,J} = 100 \, ^{\circ}C$ $R_{\theta JC}$ = Device dependent

Ton, Toff ≥ 30 seconds

Duration: 15K cycles for qualification

TEMPERATURE CYCLE (TC) PER MIL-STD-750, METHOD 1051:

The purpose of the Temperature Cycle Test is to determine the resistance of the device to high and low temperature excursions in an air medium and the effects of cycling at these extremes.

The test is performed by placing the devices alternatively in separate chambers set for high and low temperatures. The air temperature of each chamber is evenly maintained by means of circulation. The chambers have sufficient thermal capacity so that the specified ambient is reached after the devices have been transferred to the chamber, i. ent onintosen brewer noscribes blotowt is estilled

Each cycle consists of an exposure to one extreme temperature for 15 minutes minimum, then immediately transferred to the other extreme temperature for 15 minutes minimum; this completes one cycle. Note that it is an immediate transfer between temperature extremes and thereby stressing the device greater than non-immediate nidden failure mores. It is this dedication to lor.refenant

Typical Extremes

-65/+150°C OMT ni leebi ent serbaorgos storotoM

The number of cycles can be correlated to the severity of the expected environment. It is commonly accepted in the industry that ten cycles is sufficient to determine the quality of the device.

Typical Cycles for Evaluations

TO-204 and TO-220 devices: Minimum 100 cycles

TO-204 and TO-220 devices: Maximum 1000 cycles

Temperature cycling identifies any excessive strains set up between materials within the device due to differences in coefficients of expansion. Sensyllets of neolife was mo

A failure occurs when there is a change in the device's parameters beyond specified levels, or when a device checks electrically as "open" or "short".

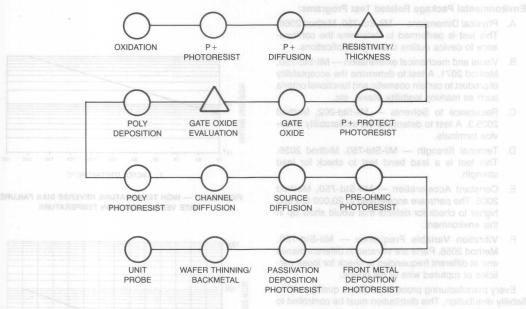
Thermal Shock (TC) Per MIL-STD-750, OMT state of MIL-STD-750, OMT stat Method 1056:

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in

The test is performed by placing the devices in a mesh basket, then alternatively immerse in baths of liquid (maintained at -55°C and +150°C). They are kept for thirty seconds in each bath and immediately transferred to the alternate bath, (STTR) als earness Fundament doll

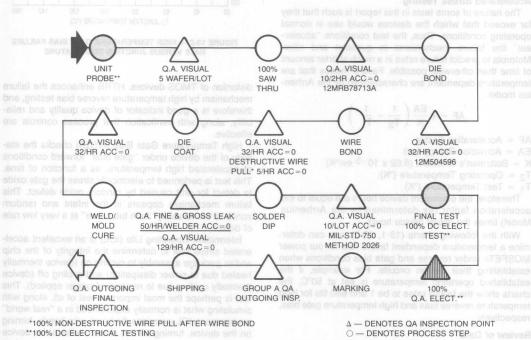
This test produces sudden heating and cooling of the device, and produces unusual stresses due to the short term temperature gradients that are set up. It is commonly accepted in the industry that five cycles is sufficient to determine the quality of the device.

A failure occurs when there is a change in the device's parameters beyond specified levels, or when a device checks electrically as "open" or "short".



 Δ — DENOTES QA INSPECTION POINT \bigcirc — DENOTES PROCESS STEP

TMOS WAFER FABRICATION



stability of leakage current, which is related 1 word associated are compatible. Molarola performs extensive

MOTOROLA TMOS POWER MOSFET DATA

ance to device outline drawing specifications.

- B. Visual and mechanical examination Mil-Std-750, Method 2071. A test to determine the acceptability of product to certain cosmetic and functional criteria such as marking legibility, stains, etc.
- C. Resistance to Solvents Mil-Std-202, Method 2025.3. A test to determine the solderability of device terminals.
- D. Terminal Strength Mil-Std-750, Method 2036. This test is a lead bend test to check for lead strength.
- E. Constant Acceleration Mil-Std-750, Method 2006. The parts are accelerated to 20,000 G's and higher to check for defects that would show up in this environment.
- F. Vibration Variable Frequency Mil-Std-750, Method 2056. Parts are vibrated in different planes and at different frequencies to check for loose particles or ruptured wire or die bonds.

Every manufacturing process exhibits a quality and reliability distribution. This distribution must be controlled to assure a high mean value, a narrow range and a consistent shape. Through proper design and process control this can be accomplished, thereby reducing the task of screening programs which attempt to eliminate the lower tail of the distribution.

Accelerated Stress Testing

The nature of some tests in this report is such that they far exceed that which the devices would see in normal operating conditions. Thus, the test conditions "accelerate" the failure mechanisms in question and allow Motorola to predict failure rates in a much shorter amount of time than otherwise possible. Failure modes that are temperature dependent are characterized by the Arrhenius model.

$$\mathsf{AF} = \mathsf{e}\,\frac{\mathsf{EA}}{\mathsf{K}}\left(\,\frac{\mathsf{1}}{\mathsf{T}_2} - \frac{\mathsf{1}}{\mathsf{T}_1}\,\,\right)$$

AF = Acceleration Factor

EA = Activation Energy (ev)

 $K = Boltzman's Constant (8.62 x 10^{-5} ev/^{\circ}K)$

T₂ = Operating Temperature (°K)

T₁ = Test Temperature (°K)

Therefore, the equivalent device hours are equal to the acceleration factor (as determined by the Arrhenius Model) times the actual device hours.

With the following charts (13-1, 13-2), one can determine a temperature dependent failure rate for our power MOSFETs under reverse and gate bias conditions when establishing their design circuits. For example, if the established operating temperature is set at 50°C, the charts show the failure rates to be 1 and 680 fits for high temperature reverse bias and high temperature gate bias, respectively.

Review of Data

High Temperature Reverse Bias (HTRB) indicates the stability of leakage current, which is related to the field

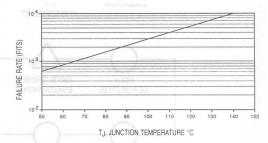


FIGURE 13-1 — HIGH TEMPERATURE REVERSE BIAS FAILURE

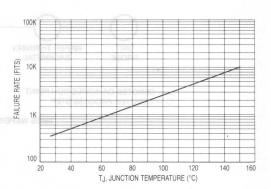


FIGURE 13-2 — HIGH TEMPERATURE GATE BIAS FAILURE RATE VERSUS JUNCTION TEMPERATURE

distortion of TMOS devices. HTRB enhances the failure mechanism by high temperature reverse bias testing, and therefore is a good indicator of device quality and reliability, along with verification that process controls are effective.

High Temperature Gate Bias (HTGB) checks the stability of the device under "gate bias" forward conditions at accelerated high temperature, as a function of time. This test is performed to electrically stress the gate oxide to detect for drift caused by random oxide defect. This failure mechanism appears in the infant and random zones of the reliability "bath tub curve" at a very low rate of defect.

Intermittent Operating Life (IOL) is an excellent accelerated stress test to determine the integrity of the chip and/or package assembly to cycling on (device thermally heated due to power dissipation) and cycling off (device thermally cooling due to removal of power applied). This test is perhaps the most important test of all, along with simulating what is normally experienced in a "real world" environment. IOL exercises die bond, wire bonds, turning on the device, turning off the device, relates the device performance, and verifying the thermal expansion of all materials are compatible. Motorola performs extensive

IOL testing as a continual process control monitor that best relates to the "device system**" as a whole. Motorola also performs extensive analysis and comparison of delta junction temperatures. Motorola has determined that to effectively stress the device a delta T_{.I} of 100°C is necessary which far exceeds many customers' application and determines the reliability modeling of the device.

Temperature Cycling (TC) is also an excellent stress test to determine the resistance of the device to high and low temperature excursions in an air medium. Where IOL electrically stresses the "device system" from internally, temperature cycle stresses the "device system" thermally from external environment conditions.

High Temperature Storage Life (HTSL), High Humidity Temperature Reverse Bias (H3TRB), Thermal Shock (TC) and "Pressure Cooker" (Autoclave) are routinely tested, however it is felt by Motorola Reliability Engineering that HTRB, HTGB, IOL and TC are of primary importance. Motorola has been in the semiconductor industry for many years and will remain there as a leader with continued reliability, quality and customer relations.

Test Results Summaries

Audit failures which are detected are sent to the and at the A SUMMARY OF TIME DEPENDENT TESTS and anti-less to trade local elevions

	(shed), 15,000 cycles (long)	Inallylical	th a variety of a	Equivalent	specialized are
Test Type	Test Conditions	Devices Failed	Device Hrs. (Actual)	Device Hrs. @ 90°C	Failure Rate % Per 1000 Hrs.
HTRB	V _{DS} = 80% of Max. Rating* V _{GS} = 0 (Shorted) T _A = 150°C	43	ong orosam moir	6.51 x 10 ⁸	sect 8000.) Sold (-ray, suger spe Consther these
HTGB	V _{GS} = ±20 V V _{DS} = 0 (Shorted) T _A = 150°C	24 81 8	3.11 x 10 ⁶	1.21 x 10 ⁹	.2063 Englished States
HTSL	T _A = 150°C 250°C	official and	8.9°x 10 ⁵	8.3 x 10 ⁷	0.0025
H ³ TRB	T _A = 85°C R.H. = 85% V _{GS} = 0 (Shorted) V _{DS} = 80% of Max. Rating up to 200 V		3.2 x 10 ⁵ Isubong BOMT and Miw mash	uncev er ing eve anomalies in the	of bo 0.28 whe

Modern electronic system reliability utilizing today's semiconductor devices requires quite low component failure rates, and therefore requires a workable number. This number called a FIT (Failure Unit) is defined as: FIT = one failure on 109 device hours.

Mean Time Between Failures (MTBF):
The significant distribution properties of electronic system reliability is expressed as MTBF, which is defined as:

 $t = 1/\lambda$

Where, t = time, hours λ = failure rate

* (changed to 100% of max rating 2Q87)

TABLE 2 SUMMARY OF CYCLE DEPENDENT TESTS

Test Type	Test Co	nditions	Devices Failed	Device Cycles (Actual)	Equivalent Device Hrs. @ 90°C	Failure Rate % Per 1000 Cycles
loL	$\Delta T_J = 100^{\circ}C$ $V_{DS} \ge 10 \text{ V}$ $t_{on}, t_{off} \ge 30 \text{ s}$	t Reject Devices er of Devices		4.3 x 10 ⁷	e Prog	.023
TC	T _{low} = -65°C T _{high} = 150°C (Plastic) T _{high} = 200°C (Metal)	s in Sample x Lot Siz		2.44 x 10 ⁶	jor9 s	0.74

*Activation energy for HTRB, HTSL = 1 eV; for HTGB = 0.3 eV.

Reliability Audit Program and alove mulanagment

At Motorola reliability is assured through the rigid implementation of a reliability audit program. All TMOS products are grouped into generic families according to voltage ranges and package types. These families are sampled weekly from the raw stock at final test, then submitted for audit testing. The extreme stress testing, in real-time for each product run, may uncover process abnormalities that are detectable by the in-process controls. Typical reliability audit tests include high temperature reverse bias, high temperature gate bias, intermittent operating life, temperature cycling, and autoclave. To uncover any hidden failure modes, the reliability tests are designed to exceed the testing conditions of normal quality and reliability testing.

Audit failures which are detected are sent to the product analysis laboratory for real-time evaluations. This highly specialized area is equipped with a variety of analytical capabilities, including electrical characterizations, wet chemical and plasma techniques, metallurgical cross-sectioning, scanning electron microscope, dispersive x-ray, auger spectroscopy, and micro/macro photography. Together, these capabilities allow the prompt and accurate analysis of failure mechanisms — ensuring that the results of the evaluations can be translated into corrective actions and directed to the appropriate areas of responsibility.

The Motorola reliability audit program provides a powerful method for uncovering even the slightest hint of potential process anomalies in the TMOS product line. It is this stringent and continuing concern with the reliability audits that gives positive assurance that customer satisfaction will be achieved.

Power FET TMOS Reliability Audit Program

Test	Conditions	S/S	Frequency
HTRB eolyeb seeds inel bos rigid o	V _{DS} = 100% Max Rating V _{GS} = 0 T _A = 150°C Duration = 72 Hours (short), 1000 Hours (long)		
When BDTH internally,	$V_{GSS} = \pm 20 \text{ V}$ m and a second $V_{DS} = 0$ and	50/Family	Weekly
IOL	Metal Products	36/Family	Weekly
T HT 90 FTM	Δ T _J = 100°C V _{DS} \geqslant 10 V Duration = 5000 Cycles (short), 15,000 cycles (long)	36/Family	Weekly
Solder Heat	1 Cycle @ 260°C for 10 seconds followed by:	25/Family	Weekly
Temperature Cycle	100 Cycles (short) 500 Cycles (long) -65 to + 150°C	25/Family	Weekly
	Dwell Time ≥ 15 minutes Requires Faraday Cages		
Pressure	P = 15 psi, T = 121°C	25/Family	Weekly
Cooker	Duration = 48 Hours (short),		HTSL
	96 Hours (long) (Plastic Package Only)		

AVERAGE OUTGOING QUALITY (AOQ) and one of 127 are benifed as the U as also

AOQ refers to the number of devices per million that do not fall within specification limits at the time of shipment. By implementing the philosophy of building in quality and reliability, Motorola has continually improved its outgoing quality. This pursuit of quality has led to a vendor certification program which guarantees a specific level of quality for the customer which has in many cases reduced or eliminated the need for incoming inspections.

AVERAGE OUTGOING QUALITY (AOQ)

AOQ = Process Average x Probability of Acceptance x 10⁶ (PPM)

- Process Average =
 Total Projected Reject Devices
 Total Number of Devices
- Projected Reject Devices = $\frac{\text{Defects in Sample}}{\text{Sample Size}} \times \text{Lot Size}$
- Total Number of Devices = Sum of all the units in each submitted lot
- Probability of Acceptance = $1 \frac{\text{Number of Lots Rejected}}{\text{Number of Lots Tested}}$
- 10⁶ = Conversion to Parts Per Million

Essentials of Reliability:

Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of trouble free service it can offer. The reliability of a device is exactly that — an expression of how well it will serve the customer. Reliability can be redefined as the probability of failure free performance, under a given manufacturer's specifications, for a given period of time. The failure rate of semiconductors in general, when plotted versus a long period of time, exhibit what has been called the "bath tub curve" (Figure 13-3).

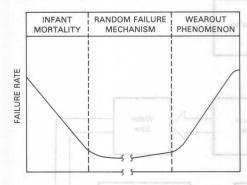


FIGURE 13-3 — FAILURE RATE OF SEMICONDUCTOR

Reliability Mechanics

Since reliability evaluations usually involve only samples of an entire population of devices, the concept of the central limit theorem applies and a failure rate is calculated using the λ^2 distribution through the equation:

$$\lambda \leqslant \frac{\lambda^2 (\alpha, 2r + 2)}{2 \text{ nt}}$$

 λ^2 = chi squared distribution

where
$$\alpha = \frac{100 - cl}{100}$$

λ = Failure rate

cl = Confidence limit in percent

r = Number of rejects

n = Number of devices

t = Duration of tests

The confidence limit is the degree of conservatism desired in the calculation. The central limit theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate, and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher λ which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 13-4).

The term (2r+2) is called the degrees of freedom and is an expression of the number of rejects in a form suitable to λ^2 tables. The number of rejects is a critical factor since

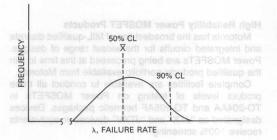


FIGURE 13-4 — CONFIDENCE LIMITS AND THE DISTRIBUTION OF SAMPLE FAILURE RATES

the definition of rejects often differs between manufacturers. Due to the increasing chance of a test not being representative of the entire population as sample size and test time are decreased, the λ^2 calculation produces surprisingly high values of λ for short test durations even though the true long term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long term failure rate. Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing has shown that temperature will accelerate failures and that this behavior fits the form of the Arrhenius equation:

$$R(t) = R_0(t)e^{-\theta/KT}$$

Where R(t) = reaction rate as a function of time and temperature

 $R_0 = A constant$

t = Time

T = Absolute temperature, °Kelvin (°C + 273°)

0 = Activation energy in electron volts (ev)

K = Boltzman's constant = 8.62 x 10⁻⁵ ev/°K

This equation can also be put in the form:

AF = Acceleration factor

T2 = User temperature

T1 = Actual test temperature

The Arrhenius equation states that reaction rate increases exponentially with the temperature. This produces a straight line when plotted on log-linear paper with a slope physically interpreted as the energy threshold of a particular reaction or failure mechanism.

Reliability Qualifications/Evaluations Outline:

Some of the functions of Motorola Reliability and Quality Assurance Engineering is to evaluate new products for introduction, process changes (whether minor or major), and product line updates to verify the integrity and reliability of conformance, thereby ensuring satisfactory performance in the field. The reliability evaluations may be subjected to a series of extensive reliability testing, such as those outlined in the "Tests Performed" section, or special tests, depending on the nature of the qualification requirement.

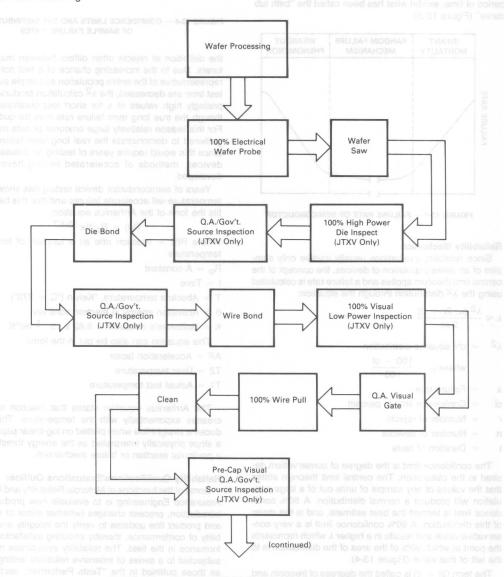
High Reliability Power MOSFET Products

Motorola has the broadest line of MIL-qualified discrete and integrated circuits for the widest range of designs. Power MOSFETs are being processed at this time to join the qualified products portfolio available from Motorola.

Complete facilities are available to conduct all three product levels of testing on Power MOSFETs in TO-204AA and TO-205AF hermetic packages. Devices designated as "JTX" and "JTXV" devices or equivalents receive 100% screening.

Motorola offers Power MOSFETs of a custom nature which have been processed to the specific high reliability requirements of a critical scientific or industrial application.

Figure 13-5 illustrates the processing flow for JAN, JTX, and JTXV and their equivalent Power MOSFETs in accordance with MIL-S-19500.



Company and the

Motorola High Reliability Parts Pending QUAL as of JAN 1984

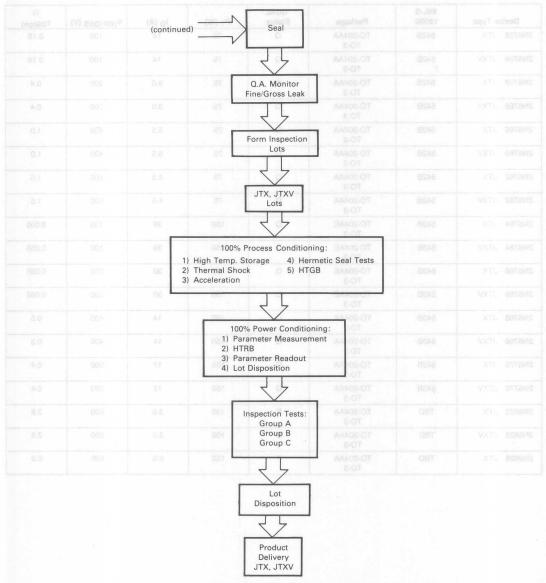


FIGURE 13-5 — JTX, JTXV AND/OR EQUIVALENT PROCESS FLOW (continued)

Motorola High Reliability Parts Pending QUAL as of JAN 1984

Device Type	MIL-S 19500/	Package	*QUAL Status	P _T (W)	ID (A)	V(BR)DSS (V)	Ω rDS(on)
2N6756 JTX	542B	TO-204AA TO-3	Q	75	14	100	0.18
2N6756 JTXV	542B	TO-204AA TO-3	a	75	14	100	0.18
2N6758 JTX	542B	TO-204AA TO-3	Q.A. Nonitor ine/Gross Leak	75	9.0	200	0.4
2N6758 JTXV	542B	TO-204AA TO-3	O L	75	9.0	200	0.4
2N6760 JTX	542B	TO-204AA TO-3	om Inspection	75	5.5	400	1.0
2N6760 JTXV	542B	TO-204AA TO-3	Q	75	5.5	400	1.0
2N6762 JTX	542B	TO-204AA TO-3	Q	75	4.5	500	1.5
2N6762 JTXV	542B	TO-204AA TO-3	Q	75	4.5	500	1.5
2N6764 JTX	543B	TO-204AE TO-3	Q	150	38	100	0.055
2N6764 JTXV	543B	TO-204AE TO-3	recess Omitifion	0.0150 P	38	100	0.055
2N6766 JTX	543B	TO-204AE TO-3	OTH (B Q	The 150 should have a second statement of the second s	30	200	0.085
2N6766 JTXV	543B	TO-204AE TO-3	0	150	30	200	0.085
2N6768 JTX	543B	TO-204AA TO-3	Power Condition	150	14	400	0.3
2N6768 JTXV	543B	TO-204AA TO-3	meter oggavrein	150 ATRI (S	14	400	0.3
2N6770 JTX	543B	TO-204AA TO-3	QiagoaiC	150	12	500	0.4
2N6770 JTXV	543B	TO-204AA TO-3	9	150	12	500	0.4
2N6823 JTX	TBD	TO-204AA TO-3	spection Tests: Group A	100	3.0	600	2.8
2N6823 JTXV	TBD	TO-204AA TO-3	Group B Group C	100	3.0	600	2.8
2N6826 JTX	TBD	TO-204AA TO-3	P	150	8.0	600	0.9



Motorola High Reliability Parts Pending QUAL as of JAN 1984 (Continued)

	е Туре	MIL-S 19500/	Package	*QUAL Status	P _T (W)	I _D (A)	V _{(BR)DSS} (V)	Ω rDS(on)
2N6826	JTXV	TBD (A)	TO-204AA TO-3	P	150	8.0	600	0.9
2N6782	JAN	556	TO-205AF TO-39	Р	15 _{85-OT}	3.5	100	0.6
0.1	JTX	556	TO-205AF TO-39	Р	15	3.5	100	0.6
- 0.1	JTXV	556	TO-205AF TO-39	Р	15 ₀₀₋₀₁	3.5	100	0.6
2N6784	JAN	556	TO-205AF TO-39	Р	15 _{88-OT}	2.25	200	1.5
	JTX	556	TO-205AF TO-39	Р	15	2.25	200	1.5
	JTXV	556	TO-205AF TO-39	Р	15	2.25	200	1.5
2N6786	JAN	556	TO-205AF TO-39	Р	15	1.25	400	3.6
	JTX	556	TO-205AF TO-39	Р	15	1.25	400	3.6
	JTXV	556	TO-205AF TO-39	Р	15	1.25	400	3.6
2N6788	JAN	555	TO-205AF TO-39	Р	20	6.0	100	0.3
	JTX	555	TO-205AF TO-39	Р	20	6.0	100	0.3
	JTXV	555	TO-205AF TO-39	Р	20	6.0	100	0.3
2N6790	JAN	555	TO-205AF TO-39	Р	20	3.5	200	8.0
	JTX	555	TO-205AF TO-39	Р	20	3.5	200	0.8
	JTXV	555	TO-205AF TO-39	Р	20	3.5	200	0.8
2N6792	JAN	555	TO-205AF TO-39	Р	20	2.0	400	1.8
	JTX	555	TO-205AF TO-39	Р	20	2.0	400	1.8
	JTXV	555	TO-205AF TO-39	Р	20	2.0	400	1.8
2N6794	JAN	555	TO-205AF TO-39	Р	20	1.5	500	3.0
	JTX	555	TO-205AF TO-39	Р	20	1.5	500	3.0
0110==:	JTXV	555	TO-205AF TO-39	Р	20	1.5	500	3.0
2N6796	JAN	557	TO-205AF TO-39	Р	25	8.0	100	0.18
Jul 1	JTX	557	TO-205AF TO-39	Р	25	8.0	100	0.18
	JTXV	557	TO-205AF TO-39	Р	25	8.0	100	0.18
2N6798		557	TO-205AF TO-39	Р	25	5.5	200	0.4
	JTX	557	TO-205AF TO-39	Р	25	5.5	200	0.4
	JTXV	557	TO-205AF TO-39	Р	25	5.5	200	0.4
2N6800	JAN	557	TO-205AF TO-39	Р	25	3.0	400	1.0

Actorola High Reliability Parts Pending GUAL as of JAN 1964 (Continued)

Motorola High Reliability Parts Pending QUAL as of JAN 1984 (Continued)

Devic	се Туре	MIL-S 19500/	Package	*QUAL Status	P _T (W)	I _D (A)	V _{(BR)DSS} (V)	Ω rDS(on)
8.0	JTX	557	TO-205AF TO-39	P	25	3.0	400 MA	1.0
	JTXV	557	TO-205AF TO-39	Pg	25	3.0	400	1.0
2N6802	JAN	557	TO-205AF TO-39	P	25	2.5	500	1.5
ē /	JTX	25 752	TO-205AF TO-39	Pq	25	2.5	500 M	1.5 2N6784
3.1	JTXV	557	TO-205AF TO-39	P	25	2.5	500	1.5

**P denotes proposed qualifications
***Q denotes qualified

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Chapter 14: Mounting Techniques For Power MOSFETs

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, semiconductor-industry field history indicates that the failure rate of most silicon semiconductors decreases approximately by one-half for a decrease in junction temperature from 160°C to 135°C.*

Many failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from mounting securely to a warped surface. With the widespread use of various plastic-packaged semiconductors, the dimension of mechanical damage becomes very significant.

Figure 14-1 shows an example of doing nearly everything wrong. In this instance, the device to be victimized is in the TO-220 package. The leads are bent to fit into a socket — an operation which, if not properly done, can crack the package, break the bonding wires, or crack the dice. The package is fastened with a sheet-metal screw through a ¼"-hole containing a fiber-insulating sleeve. The force used to tighten the screw pulls the package into the hole, causing enough distortion to crack the dice. Even if the dice were not cracked, the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heat sink surface and some burns around the hole are present, many — but unfortunately not all — poor mounting practices are covered.

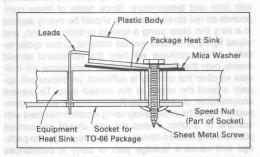


FIGURE 14-1 — EXTREME CASE OF IMPROPERLY MOUNTING A SEMICONDUCTOR (DISTORTION EXAGGERATED)

In many situations the case of the semiconductors must be isolated electrically from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc-over problems is introduced if high voltages are being handled. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures necessitate attention to the following areas:

- 1. Mounting surface preparation
- 2. Application of thermal compounds
- 3. Installation of the insulator
- 4. Fastening of the assembly
- 5. Lead bending and soldering

In this Chapter, the procedures are discussed in general terms. Specific details for each class of packages are given in the figures and in Table 1. Appendix A contains a brief review of thermal resistance concepts, and Appendix B lists sources of supply for accessories. Motorola supplies hardware for most power packages. It is detailed on separate data sheets for each package type.

Mounting Surface Preparation

In general, the heat-sink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heat-sink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high-power applications, a more detailed examination of the surface is required.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 14-2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e. $\Delta h/$ TIR, is satisfactory in most cases if less than 4.0 mils per inch, which is normal for extruded aluminum — although disc type devices usually require 1.0 mil per inch.

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory*; a finer finish is costly to achieve and does not significantly lower contact resistance. Most commercially available cast or extruded heat sinks will require spotfacing when used in high-power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger packages having mounting holes removed from the semiconductor die location, such as TO-204AA (TO-3), may successfully be used with larger holes to accommodate an insulating bushing, but Thermopad plastic packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heat sink around the mounting hole can cause two problems.

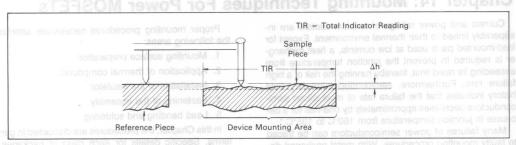


FIGURE 14-2 — SURFACE FLATNESS

The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heat sink indentation, or the device may only bridge the crater and leave a significant percentage of its heat-dissipating surface out of contact with the heat sink. The first effect may often be detected immediately by visible cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heat sinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine-edge blanking or sheared-through holes when applied to sheet metal as commonly used for stamped heat sinks. The holes are pierced using Class A progressive dies mounted on fourpost die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. The edges should be broken to remove burrs which cause poor contact between device and heat sink and may puncture isolation material.

Many aluminum heat sinks are black-anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Another treated aluminum finish is iridite, or chromate-acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heat sinks. For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heat sink, anodized or painted surfaces may be more effective than other insulating materials which tend to creep (i.e., they flow), thereby reducing contact pressure.

It is also necessary that the surface be free from all

foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Unless used immediately after machining, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse. Thermal grease should be immediately applied thereafter and the semiconductor attached as the grease readily collects dust and metal particles.

Thermal Compounds

To improve contacts, thermal joint compounds or greases are used to fill air voids between all mating surfaces. Values of thermal resistivity vary from 0.10°C-in/W for copper film to 1200°C-in/W for air, whereas satisfactory joint compounds will have a resistivity of approximately 60°C-in/W. Therefore, the voids, scratches, and imperfections which are filled with a joint compound, will have a thermal resistance of about 1/20th of the original value which makes a significant reduction in the overall interface thermal resistance.

Joint compounds are a formulation of fine zinc particles in a silicon oil which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Experience will indicate whether the quantity is sufficient, as excess will appear around the edges of the contact area. To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic-encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the assembly.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator and is therefore highly desirable despite the handling problems

*Tests run by Thermalloy (Catalog #74-INS-3, page 14) using a copper TO-204AA (TO-3) package with a typical 32-microinch finish, showed that finishes between 16 and 64 μ -in caused less than \pm 2.5% difference in interface thermal resistance.

TABLE 1 — Approximate Values for Interface Thermal Resistance and Other Package Data (See Table 2 for Case Number to JEDEC Outline Cross-Reference)

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heat sink. (See Note 3)

	Pac	kage Type and Data				Interface T	hermal I	Resistance	(°C/W)	
PP-9-03-01	A7002	Recommended		1	Metal-	to-Metal	V	ith Insulat	or	73
JEDEC Outline	Description	Mounting Hole and Drill Size	Machine Screw Size ²	Torque In-Lb	Dry	Lubed	Dry	Lubed	Туре	See Note
TO-204AA	Diamond Flange	0.140, #28	6-32	6.0	0.5	0.2	1.3	0.36	3 mil Mica	1
TO-213AA	Diamond Flange	0.140, #28	6-32	6.0	1.5	0.5	2.3	0.9	2 mil Mica	
TO-218AC	5/8" x 1/2"	0.140, #28	6-32	6.0	0.75	0.40	1.60	0.7	2 mil Mica	
TO-220AB	Thermowatt	0.140, #28	6-32	8.0	1.2	1.0	3.4	1.6	2 mil Mica	1, 2
TO-225AA	Thermopad 1/4" x 3/8"	0.113, #33	4-40	6.0	2.0	1.3	4.3	3.3	2 mil Mica	Jeve

Note 1: See Figures 14-3 and 14-4 for additional data on TO-204AA and TO-220 packages. Hello 21 bns Intelligence at Intelligence and Intelligence and Intelligence at Intelligence and Intelligence at Intelli

Note 2: Screw not insulated.

Note 3: Measurement of Interface Thermal Resistance. Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the device, a thermocouple on the heat sink, and a means of applying and measuring dc power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by the surface flatness and finish and the amount of pressure on the surfaces. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are in poor agreement.

created by its affinity for foreign matter. Some sources of supply for joint compounds are shown in Appendix B.

Some users and heat-sink manufacturers prefer not to use compounds. This necessitates use of a heat sink with lower thermal resistance which imposes additional cost, but which may be inconsequential when low power is being handled. Others design on the basis of not using grease, but apply it as an added safety factor, so that if improperly applied, operating temperatures will not exceed the design values.

Consider the TO-220 package shown in the accompanying figure. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly.

The thermocouple locations are shown:

- a. The Motorola location is directly under the die reached through a hole in the heat sink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.
- b. The EIA location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.
- c. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the EIA location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction-to-sink thermal resistance is constant for a given setup, junction-to-case values decrease and case-to-sink values increase as the case thermocouple readings become warmer.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heat sink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heat sink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple temperature at the Thermalloy location could be close to the temperature at the EIA location as the lateral heat flow is generally small.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the higher temperature of the case at a point where, hopefully, the device is making contact to the heat sink, since heat sinks are measured from the point of device contact to the ambient. Once the special heat sink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. How-

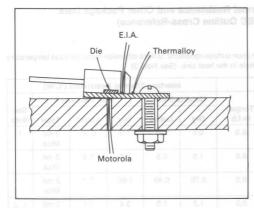


TABLE 2 — Cross Reference Chart

Motorola Case Number to JEDEC Outline Number and Table 1 Reference

Motorola Number	JEDEC Number	Reference in Table 1
Med bne et	TO-204AA	TO-204AA
T7 staff phil	TO-225AA	TO-225AA
80	TO-213AA	TO-213AA
197	TO-204AE	TO-204AE
221A	TO-220AB	TO-220AB
340	TO-218AC	TO-218AC

ever, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1.0°C/W for a TO-220 package mounted to a heat sink without thermal grease and no insulator. This error is small when compared to the heat dissipators often used with this package, since power dissipation is usually a few watts. When compared to the specified junction-to-case values of some of the higher power semiconductors becoming available, however, the difference becomes significant, and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heat sink. The washer is flat to within 1.0 mil/inch, has a finish better than 63 μ -inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application-oriented. It is also easy to use and yields reproducible results. At this printing, however, sufficient data to compare results to other methods is not available.

The only way to get accurate measurements of the interface resistance is to also test for junction-to-case thermal resistance at the same time. If the junction-to-case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

Insulation Considerations

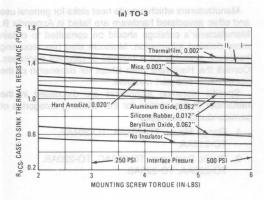
Since it is most expedient to manufacture power MOS-FETs with drains electrically common to the case, the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, it is best to isolate the entire heat sink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heat sink. Where heat sink isolation is not possible, because of safety reasons or in instances

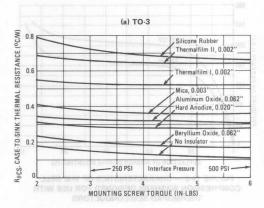
where a chassis serves as a heat sink or where a heat sink is common to several devices, insulators are used to isolate the individual components from the heat sink.

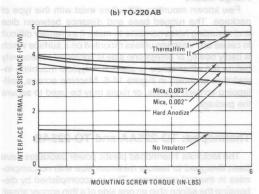
When an insulator is used, thermal grease assumes greater importance than with a metal-to-metal contact, because two interfaces exist instead of one and some materials, such as mica, have a markedly uneven surface. Reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

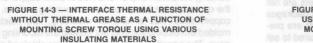
Data obtained by Thermalloy, showing interface resistance for different insulators and torque applied to TO-204AA and TO-220 packages, are shown in Figure 14-3 for bare surfaces and Figure 14-4 for greased surfaces. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case). When high power is handled, beryllium oxide is unquestionably the best choice. Thermafilm is Thermalloy's trade name for a polyimide material which is also commonly known as Kapton; this material is fairly popular for low power applications because it is low cost, withstands high temperatures and is easily handled, in contrast to mica which chips and flakes easily.

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly so that having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the breakdown voltage of the insulation system. Because of these factors, which are not amenable to analysis, high potential testing should be done on prototypes and a large margin of safety employed. In some situations, it may be necessary to substitute "empty" packages for the semiconductor to avoid shorting them or to prevent the semiconductors from limiting the voltage applied during the hi-pot test.









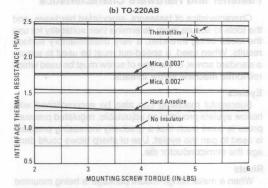


FIGURE 14-4 — INTERFACE THERMAL RESISTANCE USING THERMAL GREASE AS A FUNCTION OF MOUNTING SCREW TORQUE USING VARIOUS INSULATING MATERIALS

in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Washers

A very useful piece of hardware is the bell-type compression washer. As shown in Figure 14-5, it has the ability to maintain a fairly constant pressure over a wide range of physical deflection — generally 20% to 80% — thereby maintaining an optimum force on the package. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package or insulating washer caused by temperature changes. Bell type washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme.

Motorola washers designed for use with the Thermopad package maintain the proper force when properly secured. They are used with the large face contacting the packages.

Machine Screws

Machine screws and nuts form a trouble-free fastener system for all types of packages which have mounting holes. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of any of the Thermopad plastic package types as the screw heads are not sufficiently flat to provide properly distributed force.

Self-Tapping Screws

Under some conditions, sheet-metal screws are acceptable. However, during the tapping process with a standard screw, a volcano-like protrusion will develop in

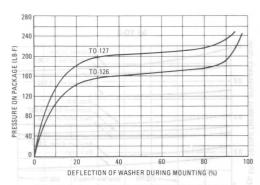


FIGURE 14-5 — CHARACTERISTICS OF THE BELL
COMPRESSION WASHERS DESIGNED FOR USE WITH
THERMOPAD SEMICONDUCTORS

Fastener and Hardware Characteristics

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use the metal being threaded; a very unsatisfactory surface results. When used, a speed-nut must be used to secure a standard screw, or the type of screw must be used which roll-forms machine screw threads.

Evelets

Successful mounting can also be accomplished with hollow eyelets provided an adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Rivets

When a metal flange-mount package is being mounted directly to a heat sink, rivets can be used. Rivets are not a recommended fastener for any of the plastic packages except for the tab-mount type. Aluminum rivets are preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

Insulators and Plastic Hardware

Because of its relatively low cost and low thermal resistance, mica is still widely used to insulate semiconductor packages from heat sinks despite its tendency to chip and flake. It has a further advantage in that it does not creep or flow so that the mounting pressure will not reduce with time in use. Plastic materials, particularly Teflon, will flow. When plastic materials form parts of the fastening system, a compression washer is a valuable addition which assures that the assembly will not loosen with time.

Fastening Techniques

Each of the various types of packages in use requires different fastening techniques. Details pertaining to each type are discussed in the following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heat sinks in a corrosive atmosphere, many devices are nickel- or gold-plated. Consequently, precautions must be taken not to mar the finish.

Manufacturers which provide heat sinks for general use and other associated hardware are listed in Appendix B. Manufacturer's catalogs should be consulted to obtain more detailed information. Motorola also has mounting hardware available for a number of different packages. Consult the Hardware Data Sheet for dimension of the components and part numbers.

Specific fastening techniques are discussed in the remainder of this section for the following categories of semiconductor packages.

- 1. Flange Mount: TO-204AA, TO-204AE, TO-213AA.
- Plastic Packages: TO-218AC, TO-220AB, TO-225AA, TO-225AB.

Flange Mount

Few known mounting difficulties exist with this type of package. The rugged base and distance between dice and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. A typical mounting installation is shown in Figure 14-6. Machine screws, self-tapping screws, eyelets, or rivets may be used to secure the package.

Thermopad: TO-225AA and TO-225AB

The Motorola Thermopad plastic power packages have been designed to feature minimum size with no compromise in thermal resistance. This is accomplished by diebonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting, i.e., plastic is molded enveloping the chip but leaving the mounting hole open. The benefits of this construction are obtained at the expense of a requirement that strict attention be paid to the mounting procedure. Success in mounting Thermopad devices depends largely upon using a compression washer which provides a controllable pressure across a large bearing surface. Having a small hole with no chamfer and a flat, burr-free, well-finished heat sink are also important requirements.

Several types of fasteners may be used to secure the Thermopad package; machine screws, eyelets, or clips are preferred. With screws or eyelets, a bell compression washer should be used which applies the proper force to the package over a fairly wide range of deflection. Screws should not be tightened with any type of air-driven torque gun or equipment which may cause high impact. Characteristics of the recommended washers are shown in Figure 14-5.

Figure 14-7 shows details of mounting TO-225AA and TO-225AB devices. Use of the clip requires that caution be exercised to insure that adequate mounting force is applied. When electrical isolation is required, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

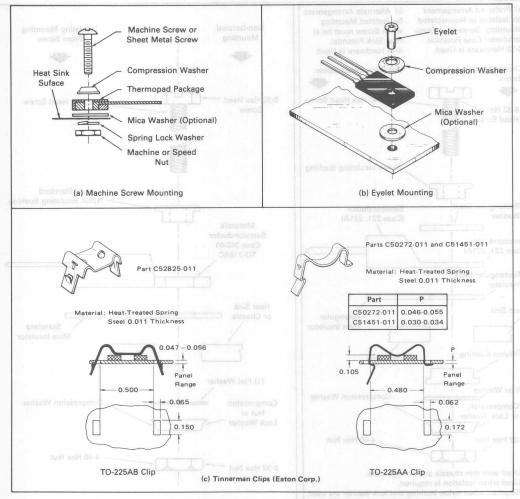


FIGURE 14-6 — RECOMMENDED MOUNTING ARRANGEMENTS FOR TO-225AA (TO-126)

Thermowatt: TO-220 W food white sall In

The popular TO-220 Thermowatt package also requires attention to mounting details. Figure 14-8 shows suggested mounting arrangements and hardware. The rectangular washer shown in Figure 14-8a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque or 8 inch-pounds is suggested when using a 6-32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO-220 packages have a chamfer on one end. TO-220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

In situations where the Thermowatt package is making direct contact with the heat sink, an eyelet may be used, provided sharp blows or impact shock is avoided.

Mounting TO-218AC

Non-isolated and isolated mounting hardware and procedures are shown in Figure 14-9. Generally, the precautions listed for the TO-220AB package are applicable to the TO-218AC package.

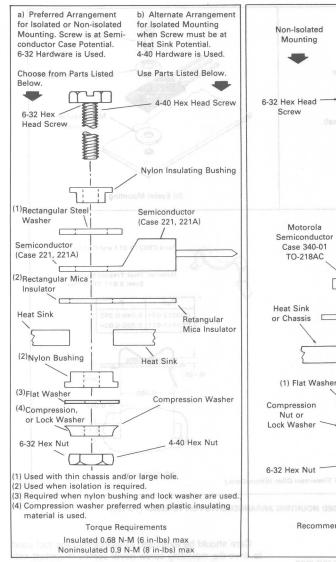


FIGURE 14-7 — MOUNTING ARRANGEMENTS FOR THERMOWATT PACKAGES (TO-220)

Free Air Power Dissipation

Frequently it is asked, "What is the maximum power dissipation capability of a particular semiconductor package without heat sinking?" The question arises more often for plastic encapsulated packages than for metal ones. Unfortunately, there is no exact maximum power dissipation for any semiconductor package without known heat sinking properties.

Power dissipation capability of a semiconductor is based upon the maximum junction temperature specification.

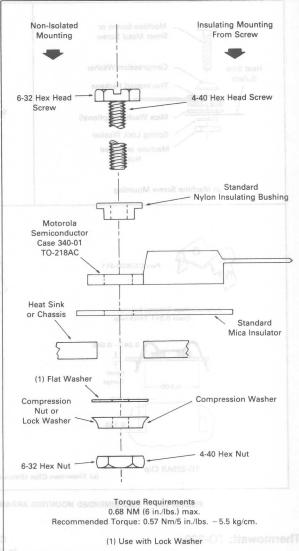


FIGURE 14-8 — MOUNTING METHODS FOR TO-218AC PACKAGE

Typical junction-to-ambient $(R_{\theta JA})$ thermal resistance values and the resulting power dissipation capability is shown in Table 3 for some popular package types. These values are typical when there is no heat sink attached to the case. Obviously, electrical connections have to be made to the package and this is one of the several variables.

There are seven factors which determine the power dissipation capability of a given package and they are: Attachment, Power Dissipation, Package Orientation, Still Free Air, Ambient Temperature, Lead Length (if applicable), and TJ(max).

One of the chief variables is mounting attachments. For maximum power dissipation, it is helpful if the electrical connection to the terminal which will permit the greatest heat removal be as massive as possible. For a metal package, it would be the case and for a plastic package lead mounted, it would be the drain lead for a power MOSFET.

Free Air and Socket Mounting

In applications where average power dissipation is of the order of a watt or so, power semiconductors may be mounted with little or no heat sinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked glass-to-metal seals around the leads. The plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heat sink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance.

In many situations, because its leads are fairly heavy, the TO-225AB package has supported a small heat sink; however, no definitive data is available. When using a

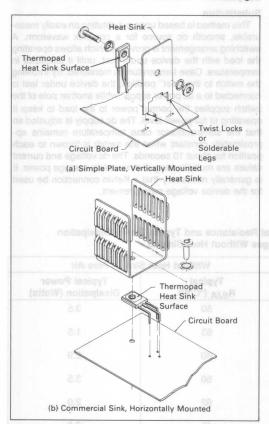


FIGURE 14-9 — METHODS OF USING SMALL HEAT SINKS WITH PLASTIC SEMICONDUCTOR PACKAGES

small heat sink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 14-9. The arrangement of part (a) could be used with any plastic package, but the scheme of part (b) is more practical with Case 77. With the other package types, mounting the transistor on top of the heat sink is more practical.

In certain situations, in particular where semiconductor testing is required, sockets are desirable. Manufacturers have provided sockets for all the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details.

Handling Pins, Leads, and Tabs

The pins and lugs of metal-packaged devices are not designed for any bending or stress. If abused, the glass-to-metal seals could crack. Wires may be attached using sockets, crimp connectors, or solder, provided the data sheet ratings are observed.

The leads and tabs of the plastic packages are more flexible and can be reshaped, although this is not a recommended procedure for users to do. In some cases, a heat sink can be chosen which makes lead-bending unnecessary. Numerous lead- and tab-forming options are available from Motorola. Preformed leads remove the risk of device damage caused by bending from the users.

If, however, lead-bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

- 1. A lead-bend radius greater than 1/16 inch is advisable for the TO-225AA and 1/32 inch for TO-220.
- 2. No twisting of leads should be done at the case.
- 3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than four pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. An acceptable lead-forming method that provides this relief is to incorporate an S-bend into the lead. Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 275°C and must be applied for not more than five seconds at a distance greater than 1/8 inch from the plastic case. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead-to-plastic junctions.

Cleaning Circuit Boards boog at the latest Hame

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices.

Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline may cause the encapsulant to swell, possibly damaging the transistor die. Likewise, chlorinated Freon solvents are unsuitable, since they may cause the outer package to dissolve and swell.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if the packages are free-standing without support.

Thermal System Evaluation and and and

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN-569.

Other applications including switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A) A fine thermocouple should be used, such as #32AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

 $T_J = T_C + R_{\theta JC} \times P_D$ where

T_J = junction temperature (°C)

T_C = case temperature (°C)

 $R_{\theta JC}$ = thermal resistance junction-to-case as specified on the data sheet (°C/W)

PD = power dissipated in the device (W).

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration is lead on to slittly the behavior

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

TABLE 3 — Typical Junction-to-Ambient Thermal Resistance and Typical Power Dissipation for Various Transistor Packages Without Heat Sinking

			ACTIVE AND COURSE	
I pull. Force in this direction greater virefull in permenent damage to the		Without Heat Sink in Free Air		
Motorola Case Number	JEDEC Number	Typical R _θ JA (°C/W)	Typical Power Dissipation (Watts)	
d of strain relief sinfuld be devised		50 soutable October Board	3.5	
an S-bend into the 77rd. Wire wrap- ermasible, provided that the lead is	TO-225AA	83	1.5	
ne plastic case an 08 a point of the maximum solution		60	2.9	
low-wer, must not a 701 ed 275°C and to those than five seconds at a dis	TO-204AE	50	3.5	
8 inch from the A1SS case. When	The state of the s	62 SemucM-yiletnosi	2.0 (b) Commercial Sink, He	
ent of the wire does 046 cause move-	TO-218AC	45	2.8	

APPENDIX A

THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady-state conditions is generally written as:

$$q = hA\Delta T$$
 (1)

where $\ \ q = rate of heat transfer or power dissipation (PD),$

h = heat transfer coefficient,

A = area involved in heat transfer.

See ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, R_{θ} , is $R_{\theta} = \Delta T/q = 1/hA$ (2)

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that ΔT could be thought of as a voltage; thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A1.

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A$$
 (3)

where T_J = junction temperature,

PD = power dissipation,

R_BJC = semiconductor thermal resistance

(junction to case),

 $R_{\theta}CS$ = interface thermal resistance (case to

0888-815 (Tray heat sink),

 $R_{\theta SA}$ = heat sink thermal resistance (heat

sink to ambient).

T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result. The value for the interface thermal resistance, $R_{\theta CS}$, is affected by the mounting procedure and may be significant compared to the other thermal-resistance terms.

The thermal resistance of the heat sink is not constant; it decreases as ambient temperature increases and is affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. In some applications such as in RF power amplifiers and short-pulse applications, the concept may be invalid because of localized heating in the semiconductor chip.

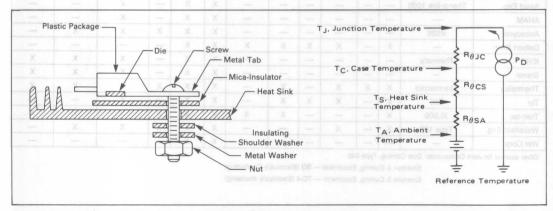


FIGURE A1 — BASIC THERMAL RESISTANCE MODEL SHOWING THERMAL TO ELECTRICAL ANALOGY FOR A SEMICONDUCTOR

APPENDIX B year directly all the equivalent electrical circuit may B XIDNATA

SUPPLIERS ADDRESSES

Aavid Engineering, Inc., 30 Cook Court, Laconia, New Hampshire 03246 (603) 524-4443

AHAM Heat Sinks, 27901 Front Street, Rancho, California 92390 (714) 676-4151

Astrodyne, Inc., 353 Middlesex Avenue, Wilmington, Massachusetts 01887 (617) 272-3850

Delbert Blinn Company, P.O. Box 2007, Pomona, California 91766 (714) 623-1257

Dow Corning, Savage Road Building, Midland, Michigan 48640 (517) 636-8000

Dayton Corporation, Engineered Fasteners Division, Tinnerman Plant, P.O. Box 6688, Cleveland, Ohio 44101 (216) 523-5327

Emerson & Cuming, Inc., Dielectric Materials Division, 869 Washington Street, Canton, Massachusetts 02021

et bna 29250000 etutstegmet Insigme (617) 828-3300

International Electronics Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502

(213) 849-2481

The Staver Company, Inc., 41-51 North Saxon Avenue, Bay Shore, Long Island, New York 11706

(516) 666-8000

Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243-4321

Tor Corporation, 14715 Arminta Street, Van Nuys, California 91402 (213) 786-6524

Tran-tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564-2748

Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245-5900

Wei Corporation, 1405 South Village Way, Santa Ana, California 92705 (614) 834-9333

SOURCES OF ACCESSORIES DOE (A) CONTRACTOR OF ACCESSORIES

Manufacturer	Joint Compound	ed blisvei ed Insulators					Heat Sinks						
		BeO	Al0 ₂	Anodize	Mica	Plastic Film	Silicone Rubber	Stud	Flange	Disc	Thermowatt	Unit/Duo Watt	RF Stripline
Aavid Eng.	Ther-o-link 1000	_	_		_	_	_	X	X	_	X	_	-
AHAM	_	_	_	_	-	_	_	Х	X	_	Х	_	
Astrodyne	#829	тьогт	e.f. Wo	stampt 4	_		_	X	Х	X	X	X	1819
Delbert Blinn		X	_	X	Х	X	X	X	X	-	_	_	_
IERC	Thermate	_	_	_	_	_	de T I stel	X	×	_	X	Х	Х
Staver	81076	00,00	3	1.01	_	Tests	Later Frenchis	X	X	_	X	X	Х
Thermalloy	Thermacote	X	Х	X	_	X	alt -	X	X	X	X	X	X
Tor	TJC	X	_	X	Х	X	-/	X	X	kana.	X	6 - B	B B
Tran-tec	XL500	X	_	_	_	X	X	X	X	X	X	X	X
Wakefield Eng.	Type 120	X	-	Х	-	politel	neral -	X	X	X	Х	X	_
Wei Corp.	67U361	io <u>m</u> a	_	_		orla ni V v	-Shoulde	X	X	2000	_	_	_

Other sources for Joint Compounds: Dow Corning, Type 340

Emerson & Cuming, Eccoshield — SO (Electrically Conducting)
Emerson & Cuming, Eccotherm — TC-4 (Electrically Insulating)

Chapter 15: Electrostatic Discharge and Power MOSFETs

One of the major problems plaguing electronics components today is damage by electrostatic discharge (ESD). ESD can cause degradation or complete component failure. Shown in Table 1 are the susceptibility ranges of various devices to ESD. As circuitry becomes more complex and dense, device geometries shrink, making ESD a major concern of the electronics Industry.

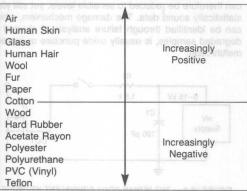
Generation of ESD

Electrostatic potential is a function of the separation of non-conductors on the list of materials known as the Triboelectric Series. (See Table 2.) Additional factors in charge generation are the intimacy of contact, rate of separation and humidity, which makes the material surfaces partially conductive. Whenever two non-conductive materials are flowing or moving with respect to each other, an electrostatic potential is generated.

TABLE 1 - Susceptibility to ESD

Device Type	Range of ESD Susceptibility (Volts)
Power MOSFET	100-200
in begrario a lo fugitio enti eJFETbris atriementissen	140-10,000 elosT) show
CMOS and and balante	250-2,000
Schottky Diodes, TTL	300-2,500
Bipolar Transistors	380-7,000
ECLAIDE Houte LAIDE	500 bluoris anodenidimos
SCR id obliko-etsp tarti w oda era enoitonul beseid-e	680–1,000 Varimilaria

TABLE 2 — Triboelectric Series



From Table 2, it can be seen that cotton is relatively neutral. The materials that tend to reject moisture are the most significant contributors to ESD. Table 3 gives examples of the potentials that can be generated under various conditions.

TABLE 3 — Typical Electrostatic Voltages

	Electrostatic Voltages					
Means of Static Generation	10 to 20 Percent Relative Humidity	65 to 90 Percent Relative Humidity				
Walking across carpet	35,000	1,500				
Walking over vinyl floor	12,000	250				
Worker at bench	6,000	100				
Vinyl envelopes per work instructions	7,000	600				
Common poly bag picked up from bench	20,000	1,200				
Work chair padded with polyurethane foam	18,000	1,500				

From the Tables, it is apparent that sensitive electronic components can be easily damaged or destroyed if precautions are not taken.

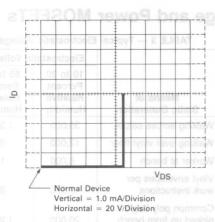
ESD and Power MOSFETs

Being MOS devices, TMOS transistors can be damaged by ESD due to improper handling or installation. However, TMOS devices are not as susceptible as CMOS. Due to their large input capacitances, they are able to absorb more energy before being charged to the gate-breakdown voltage. Nevertheless, once breakdown begins, there is enough energy stored in the gate-source capacitance to cause complete perforation of the gate oxide. With a gate-to-source rating of VGS = \pm 20 V maximum and electrostatic voltages typically being 100–25,000 volts, it becomes very clear that these devices require special handling procedures. Figure 15-1 shows curve tracer photos of a good device, and the same device degraded by ESD.

Static Protection

The basic method for protecting electronic components combines the prevention of static build up with the removal of existing charges. The mechanism of charge removal from charged objects differs between insulators and conductors. Since charge cannot flow through an insulator, it cannot be removed by contact with a conductor. If the item to be discharged is an insulator (plastic box, person's clothing, etc.), ionized air is required. If the object to be discharged is a conductor (metal tray, conductive bag, person's body, etc.), complete discharge can be accomplished by grounding it.

A complete static-safe work station should include a grounded conductive table top, floor mats, grounded operators (wrist straps), conductive containers, and an ionized air blower to remove static from non-conductors. All soldering irons should be grounded. All non-conductive items such as styrofoam coffee cups, cellophane wrappers, paper, plastic handbags, etc. should be removed from the work area. A periodic survey of the work area with a static



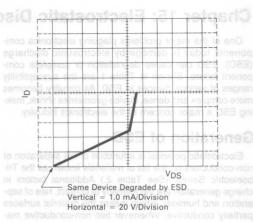
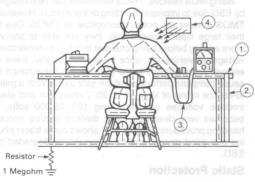


FIGURE 15-1 — CURVE TRACER DRAWINGS OF A GOOD DEVICE AND A DEVICE 10 001Wolf 215 dailed WITH A DEGRADED GATE DEVICE IS A 100 VOLT, 12 AMP POWER MOSFET IS IN 150 DAILS 2015 15 TO 15

meter is good practice and any problems detected should be corrected immediately. Above all, education of all personnel in the proper handling of static-sensitive devices is key to preventing ESD failures. Figure 15-2 shows a typical manufacturing work station.



NOTES: 1. 1/16 inch conductive sheet stock covering bench top work area

- 2. Ground strap
- 3. Wrist strap in contact with skin
- Static neutralizer (Ionized air blower directed at work) Primarily for use in areas where direct grounding is impractical

FIGURE 15-2 — TYPICAL MANUFACTURING WORK STATION

By following the above procedures, and using the proper equipment, ESD sensitive devices can be handled without being damaged. The key items to remember are:

- Handle all static sensitive components at a static safeguarded work area.
- Transport all static sensitive components in static shielding containers or packages.
- Education of all personnel in proper handling of static sensitive components.

Test Method:

Military specifications MIL-STD-883B Method 3015.1. DOD-HDBK263, and DOD-STD-1686 classify the sensitivity of semiconductor devices to electrostatic discharge as a function of exposure to the output of a charged network (Table 4). Through measurements and general agreement, the "human-body model" was specified as a network that closely approximated the charge storage capability (100 pF) and the series resistance (1.5 k) of a typical individual (Figure 15-3). Discharge of this network directly into a device indicates that the model assumes a "hard" ground is in contact with the part. Although all pin combinations should be evaluated in both polarities (a total of six combinations for a TMOS Power MOSFET), preliminary tests usually show that gate-oxide breakdown is most likely, and that reverse-biased junctions are about an order of magnitude more sensitive than forward-biased ones. The amount of testing, and components required, can therefore be reduced to sensible levels, yet still yield statistically sound data. The damage mechanism, which can be identified through failure analysis of shorted or degraded samples, is usually oxide puncture or junction meltthrough.

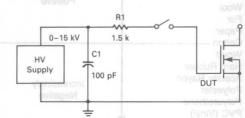


FIGURE 15-3 — THE HUMAN-BODY EQUIVALENT NETWORK

Significance of Sensitivity Data

Assuming that corrective measures cannot be immediately applied in a manufacturing area, or that products manufactured using MOSFET components are likely to

be exposed to ESD events in the field, the sensitivity of the device can be used as a general indicator of the likelihood of failure. Additionally, the extent and cost of

protective measures increases as device susceptibility increases.

signal Annual TABLE 4 — Sensitivity of Semiconductors to ESD from a Charged Network obsist lostoco fuglio

Device Sensitivity (C ₁ Peak Voltage)	MIL-STD-883 Class	DOD-HDBK-263 Class	Typical Preventive Measures(2)
0-1000 onless	ment of E(A) sensitivity	Class 1	Careful Case, Keyboard Design,
the results shown be-	(Sensitive)	UT is se- 100 oF-1	Wrist Straps, Ionized Air,
1000-2000 leb alif	portant colAlusion from	Class 2	Conductive Flooring, Conductive Clothing, etc. Field-Strength Alarm.
2000-4000	osiA esserBni (vtilidens	Class 3	Antistatic Carpet Spray, Wrist Straps,
as 688-bi8-liM vd ber	(Nonsensitive)	he trioper or below I	Conductive Packaging Materials.
4000-15,000(1)	as solvebB, settisselo	Class 3	Humidity Adjustment

Notes: 1. Data collected in many applications have shown that under special conditions voltages considerably in excess of 15 kV can be generated with certain materials in the Triboelectric Series.

These examples are intended only as very general guidelines. The actual accuracy of a given method is highly variable, as a large number of interdependent factors influence electrostatic field generation. Operator awareness, complemented with a high quality hand-held electrostatic field-strength meter referenced to ground, can be very effective in controlling profit losses due to ESD.

A Simple ESD Pulser

A simple electrostatic discharge circuit, which simulates the human body model, is shown in Figure 15-4.

The high voltage supply consists of a 20 mA constantcurrent luminous-tube transformer and a half-wave voltage doubler circuit. Adjustment of the high voltage is accomplished with a 1.0 Amp Variac. (An oscillator-type supply may also be constructed, using a flyback transformer.) Voltage is monitored by a microammeter, using a 600 megohm current resistor, constructed from 30-1/2 watt, 20 $\mathrm{M}\Omega$ carbon composition resistors connected in series.

A low voltage supply powers a 555 I.C. timer to provide trigger pulses. This circuit fires a C106 SCR, discharging the 0.033 μ F capacitor into an ordinary photoflash trigger coil. This provides a narrow, high-voltage pulse to fire the

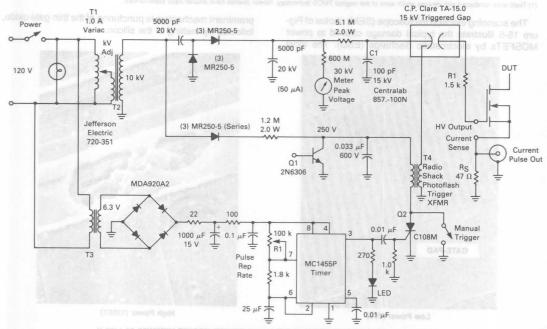


FIGURE 15-4 — ESD (ELECTRO STATIC DISCHARGE) PULSER

triggered gap. The +250 V across the 0.033 μF capacitor is derived by a separate rectifier string, and is regulated by the V(BR)CEO of an NPN power transistor, used as a high-voltage Zener. This voltage quickly saturates as the output control is advanced.

The high voltage supply charges a 100 pF ceramic transmitting-type capacitor, which has extremely low equivalent series inductance. This capacitor, along with the 1.5 k Ω series resistance, forms the standard human-body equivalent circuit specified by MIL-STD-883.

Discharge of the 100 pF capacitor into the DUT is accomplished by means of a triggered spark gap. This device, although somewhat expensive (= \$100), is nearly an ideal switch, without the voltage limitations, contact bounce, and drive requirements of reed relays. The trigger pulse initiates a plasma discharge between the probe and one electrode. This plasma is swept across the gap by the electric field, initiating arc breakdown.

Warning: diensa ent ,bleft ent ni zineve OZ

Caution is advised in the construction and operation of this circuit, as the potentials and stored energies in this circuit may be *lethal*. Every effort should be made to shield operators from the possibility of contact. Motorola cannot be responsible for claims resulting from the use, or misuse, of this circuit.

Test Results

Measurement of ESD sensitivity thresholds using the 100 pF-1.5 k circuit has produced the results shown below. An important conclusion from this data is that the ESD sensitivity decreases as the die size (and powerhandling capability) increase. Also, these devices fall at or below the 2,000 volt limit defined by Mil-Std-883 as that which classifies a device as static-sensitive. Power MOSFETs, then, should be handled with proper precautions

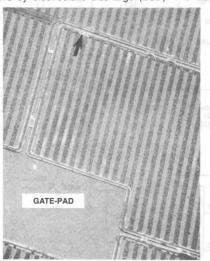
an elderay virgin at bottom needs a tow TABLE 5 — Test Results

Device	Ratings	Die Size (Mils ²)	C _{iss} (pF)	Sensitivity (Volts)
MTP5N05 ⁽¹⁾	5.0 A, 50 V, N-CH, Plastic	762	150	520 G23 sigmis
MTP15N05	15 A, 50 V, N-CH, Plastic	dopem 1502 dislumia	c dischar 007 rcuit, which at, is shown in Figure 15	s on your name A
MTM6N60	6.0 A, 600 V, N-CH, Metal	vol A 1992 lov evan	1400	1350
MTM8N60	8.0 A, 600 V, N-CH, Metal	0.0 enl 250 ² que equi-	2000 s/ gm/s	mple 0061 th a

(1) Tests were conducted with devices which were of the original TMOS technology. Newer devices have smaller input capacitances.

The scanning electron microscope (SEM) photos of Figure 15-5 illustrate the typical damage caused to power MOSFETs by electrostatic discharge (ESD). The most

prominant mechanism is puncturing of the thin gate oxide, followed by melting of the silicon.



Low Power (70X)



High Power (1200X)

FIGURE 15-5 — RESULTS OF ESD TESTING A 6.0 A POWER MOSFET MTM6N60 AT 1000 V.

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MOTOROLA INC.



Dear Valued Motorola Customer:

Prior to introducing TMOS Power FETs in 1980, Motorola spent three years in developing what was considered at that time the industry's most advanced power MOSFETs, but we weren't satisfied with that. We kept working on the product and since that time, major advancements in our technology were made. Now high volume and advanced technology allows us to offer you the broadest line of power MOSFETs of the highest quality possible at the best price. With voltage capability to 1000 Volts and current ratings as high as 100 Amperes, you can select exactly what you need.

Our latest technology utilizes high source site or cell density (over 1 million cells per square inch) for efficient utilization of silicon. This results in a smaller chip for a given $r_{DS(on)}$ or a lower $r_{DS(on)}$ for a given chip size — either way, price or performance is enhanced and our customers receive the benefits.

Motorola's commitment to quality is continuing to show significant results. The AOQ of TMOS Power FETs has been consistently reduced and now we guarantee an AOQ of 100 ppm, although currently the AOQ is well under 100 ppm. How we accomplish this is included in this manual.

As the world's largest manufacturer of power transistors we have the equipment, know-how, and capacity to serve your needs.

Power MOSFETs are a reality and Motorola is dedicated to becoming a leading supplier of power MOSFETs just as it has become the leading source for bipolar power — we intend to attain this leadership position by earning it.

It is our intent to offer superior performance, value, service, quality, and reliability.

We invite your inquiries.

Paul V. White,

Vice President and Director of Product Marketing,

Discrete and Special Technologies Group

TMOS Power MOSFETs

Metal Packages — TO-204

Table 1 — P-Channel





TO-204

CASE 1-04 and CASE 1-06

Table 2 — N-Channe

V(BR)DSS (Volts) Min		(Amps)	Device 01	I _D (Amps) Max	PD* (Watts) Max
500	6	1 8	MTM2P50	2	75
450	08	1.0	MTM2P45	180.0	
250	214	1.5	MTM3P25	3	
	3	2.5	MTM5P25	81.65	100
	2	4	MTM8P25	8	
200	3×11	2.5	MTM5P20	5	
	0.7	4	MTM8P20	8	125
180	381	2.5	MTM5P18	5	75
	0.7	4	MTM8P18	8	125
100	0.4	3	MTM8P10	800	75
	0.3	6	MTM12P10	12	
	0.15	10	MTM20P10	20	125
80	0.4	4	MTM8P08	8	75
	0.3	6	MTM12P08	12	
	0.15	10	MTM20P08	20	125
60	0.3	6	MTM12P06	12	75
65	0.14	12.5	MTM25P06	25	125
50	0.3	6	MTM12P05	12	75
150	0.2	10	MTM20P05	20	100
	0.14	12.5	MTM25P05	25	125
@ 25°C	QA	Ť.	20 18515		

V(BR)DSS (Volts) Min	rDS(or (Ohms) Max	(Amps)	Device	I _D (Amps) Max	P _D * (Watts) Max
1000	10	0.5	MTM1N100	1	75
	4	1.5	MTM3N100	3	125
	3	2.5	MTM5N100	5	150
950	810	0.5	MTM1N95	88.9	75
	4	1.5	MTM3N95	8.3	125
	813	2.5	MTM5N95	5	150
900	8	446	MTM2N90	2	75
	4	2	MTM4N90	4	125
	3	3	MTM6N90	6	150
850	8	1 10	MTM2N85	2	75
	0.4	2	MTM4N85	4	125
	83	3	MTM6N85	6	150
800	17	1.5	MTM3N80	3	75
	2	3	BUZ84	5.3	125
080	1.5	09100	BUZ84A	6	
750	8.7	1.5	MTM3N75	3	75
600	2.8	3	2N6823		
	2.5	1.5	MTM3N60	1 1	
	1.6	6	2N6826	6	150
	1.2	3	MTM6N60	6.0	
	0.5	4	MTM8N60	8	

^{* @ 25°}C

Device types shaded in Tables 1 through 6 are key industry standard devices recommended for new designs.

Table 2 — N-Channel — continued

V(BR)DSS (Volts) Min		(Amps)	Device	(Amps) Max	P _D * (Watts) Max
500	4	1	MTM2N50	2	75
	1.5	2	MTM4N50	4	
		3	2N6762**	4.5	
	0.85	4	IRF440	8	125
	0.8	3.5	MTM7N50	7	150
	0.5	7	IRF452	12	ed(RS) (elloV)
	0.4	- 60	IRF450	13	dill
	1	7.75	2N6770**	0/12	1000
	8	7.5	MTM15N50	115	250
450	1.5	2	MTM4N45	4	75
	0.85	4:9/1	IRF441 8.0	0.8	125
	0.8	3.5	MTM7N45	4.7	150
	0.4	7.008	IRF451 8.5	€13	
		7.5	MTM15N45	815	250
400	p 1	3	IRF330	5.5	75
		2.5	MTM5N40	€5	
		3.5	2N6760**	5.5	850
	0.55	5.8/4	IRF340	10	125
		4:814	MTM8N40	8.3	150
	0.3	8	IRF350	15	000
125		9	2N6768**	\$14	
		7.5	MTM15N40	15	250
350	1.5	3 7 1	IRF333	4.5	75
		85	2N6759	8.5	608
	1	0814	IRF331	5.5	
150	8	2.5	MTM5N35	a.5	
	0.3	8	IRF351	⊴ 15	150
		7.5	MTM15N35	0.6	250
250	0.45	5	MTM10N25	10	100
200	0.4		IRF230	9	75
			2N6758**		
		4	MTM8N20	8	
	0.18	10	IRF240	18	125
	0.16	7.5	MTM15N20	15	150

Table 2 — N-Channel — continued

V(BR)DSS (Volts) Min		(Amps)	Device	I _D (Amps) Max	P _D * (Watts) Max
200	0.12	16	IRF252	25	150
	0.085		IRF250	30	
		19	2N6766**		
	0.08	20	MTM40N20	40	250
150	0.22	10	IRF243	16	125
	0.18	16	IRF241	18	Cation()
	0.12	10	MTM20N15	20	150
	8	16	IRF253	25	500
	0.085	31-99	IRF251	30	450
	0.06	22.5	MTM45N15	45	250
100	0.18	8 9 8	IRF130	€14	75
	8	6	MTM12N10	12	
	8	9298	2N6756**	14	000
	0.15	10	MTM20N10	20	100
	0.11	15	IRF142	24	125
	0.085	8198	IRF140	7.27	
	0.08	20	IRF152	33	150
	0.075	12.5	MTM25N10E†	25	
	0.07	01900	MTM25N10	0.18	
	0.055	20	IRF150	40	08
	37	24	2N6764	38	
	0.04	27.5	MTM55N10	3155	250
80	12	2098	MTM55N08	0.3	08.
60	0.15	7.5	MTM15N06E†	15	75
	0.085	15	IRF141	27	125
	0.055	17.5	MTM35N06	35	150
	25	8098	MTM35N06E†	0.14	
		20	IRF151	40	25°C
	0.028	30	MTM60N06	60	250
50	0.2	6	MTM12N05	12	75
	0.055	17.5	MTM35N05	35	150
	0.035	29	MTM45N05E†	45	125
	0.028	30	MTM60N05	60	250
		25	MTM50N05E†	50	125

† Indicates E-FET device, with avalanche energy specified.

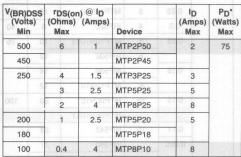
Device types shaded in Tables 1 through 6 are key industry standard devices recommended for new designs.

^{* @ 25°}C **Available at JTX and JTXV levels

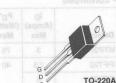
TMOS Power MOSFETs

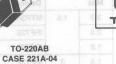
Plastic Packages — TO-220

Table 3 — P-Channel









V(BR)DSS (Volts) Min	rDS(or (Ohms) Max	(Amps)	Device	I _D (Amps) Max	P _D * (Watts) Max
100	0.3	6	MTP12P10	12	75
80	0.4	4	MTP8P08	8	
	0.3	6	MTP12P08	12	355
60	0.6	3.5	MTP7P06	7	
	0.3	6	MTP12P06	12	
	0.2	10	MTP20P06	20	100
50	0.6	3.5	MTP7P05	7	75
	0.3	6	MTD12D05	10	

Table	4 -	N-Channel

V(BR)DSS (Volts) Min	rDS(or (Ohms) Max	n) @ ID (Amps)	Device	I _D (Amps) Max	PD* (Watts) Max
1000	10	0.5	MTP1N100	8.0 1	75
	4	1.5	MTP3N100	3	
950	10	0.5	MTP1N95	40 1	
	4	1.5	MTP3N95	3	
900	8	1/98	MTP2N90	80 2	
	4	2019	MTP4N90	81.0 4	
850	8	1688	MTP2N85	8 0 2	
	4	Hao2ors	MTP4N85	50 4	
800	7	a(1.5)	MTP3N80	3	
750	4	531	MTP3N75	81.0	
600	12	0.5	MTP1N60	ar.o. 1	
	6	1001089	MTP2N60	2 0 2	
	2.5	1.5	MTP3N60	3	
	1.2	3	MTP6N60	6	125
550	12	0.5	MTP1N55	1	75
19 -	2.5	1.5	MTP3N55	3	
	1.2	3	MTP6N55	6	125
500	8	0.5	MTP1N50	ven sot bear	50
	4	1	MTP2N50	2	75

* @ 25°C	3.6	0.8
Device types shaded in Tables 1 through 6 are key industry standard devices	recommended for new o	designs.

V(BR)DSS (Volts) Min	rDS(on (Ohms) Max	(Amps)	Device	(Amps) Max	PD* (Watts) Max
500	3	1.5	IRF820	2.5	40
			MTP3N50	3	75
	2 000	IRF832	4		
	1.5		IRF830	4.5	
			MTP4N50	4	
	1.1	4	IRF842	7	125
	0.85	840	IRF840	8	
	0.8		MTP8N50		NA P
450	8	0.5	MTP1N45	NO. 1	50
4	4	PTONTS	MTP2N45	2	75
			IRF823	30.0	40
	3		IRF821	2.5	
		1.5	MTP3N45	3	75
	2	2.5	IRF833	4	120
	1.5	2	MTP4N45	90	
		2.5	IRF831	4.5	
	1.1	4	IRF843	80.7	125
	0.85		IRF841	8	
	0.8		MTP8N45		t inches
400	5	1	MTP2N40	2	50
	3.6	0.8	IRF710	1.5	20

V(BR)DSS (Volts) Min		(Amps)	Device	(Amps) Max	PD* (Watts) Max
400	3.3	1.5	MTP3N40	3	75
	2.5		IRF722	2.5	40
	1.8		IRF720	3	
	1.5	3	IRF732	4.5	75
C9 6	1		IRF730	aem les	
ps) (Watt	nA)	2.5	MTP5N40	5	
celli xi	0.55	5	IRF740	10	125
			MTP10N40		
350	5	1	MTP2N35	2	50
	1.5	3	IRF733	4.5	75
	1		IRF731	5.5	
		2.5	MTP5N35	5	
odr, s	0.55	5	IRF741	10	125
			MTP10N35	80	50
250	2	309019	MTP2N25	2	50
	0.45	5	MTP10N25	10	100
200	2.4	1.25	IRF612	2	20
	1.8	1	MTP2N20		50
	1.5	1.25	IRF610	2.5	20
'gq ('teW) (so	mA)1	2.5	MTP5N20	5	75
cult o	0.8	epin	IBF620	23 (1)	40
64 3	0.7	3.5	MTP7N20	7	75
75	0.6	5	IRF632	8	15
	0.4	328	IRF630	9	
6	5.4	4	MTP8N20	8	
	0.35	6	MTP12N20	12	100
125	0.33	10	IRF642	16	125
	0.22	840	IRF640	27.0	125
150	0.18	2.5	IRF621	18	40
50	0.6	5	IRF631		40
75	0.4	P2N45	THE RESERVE OF THE PERSON NAMED IN COLUMN TWO IS NOT THE PERSON NAMED IN COLUMN TWO IS NAMED IN COLUMN TW	9	75
40		- 558	MTP10N15	10	400
	0.25	7.5	MTP15N15	15	100
25	0.22	10	IRF643	16	125
400	0.18	_555	IRF641	18	
120	0.3	5	MTP10N12	10	75
	0.9	2.5	MTP5N12	5	50
386	1.3	1.5	MTP3N12	3	
100	0.8	3	MTP6N10	6	
		2	IRF512	3.5	20

V(BR)DS (Volts) Min	SS rDS(or (Ohms) Max	(Amps)	Device	(Amps) Max	(Watts
100	0.6		IRF510	4	20
	0.5	4	MTP8N10	8	75
			MTP8N10E†		
	0.4		IRF522	7 8	40
	0.33	5	MTP10N10	10	75
	0.3	4	IRF520	8	40
	0.25	5	MTP10N10E†	10	75
		8	IRF532	12	45
	0.18	de dari	IRF530	14	as
		6	MTP12N10	12	55
	0.15	10	MTP20N10	20	100
		4000000	MTP20N10E†		Mar.
	0.11	15	IRF542	24	81
	0.085	81767	IRF540	27	101
		12.5	MTP25N10	25	CON COL
	0.075		MTP25N10E†		125
80	0.8	2	MTP4N08	4	50
	0.5	4	MTP8N08	8	75
	0.33	5	MTP10N08	10	
	0.18	6	MTP12N08	12	rable
	0.15	10	MTP20N08	20	100
60	0.8	2	IRF513	3.5	20
	0.6	001/415	IRF511	4	1001
		2.5	MTP5N06	5	50
	0.4	3.5	MTP7N06	7	950
	8	4	IRF523	5-	40
	0.3	08/45/9	IRF521	8	006
	0.28	5	MTP10N06	10	75
	0.25	8	IRF533	12	088
	0.2	5	MTP10N06E†	10	
	8	6	MTP12N06	12	880
	0.18	8	IRF531	14	750
	0.16	7.5	MTP15N06	15	008
	0.15	6	MTP3055E†	12	40
	2 1	7.5	MTP15N06E†	15	75

* @ 25°C † Indicates E-FET devices with avalanche energy specified.

Device types shaded in Tables 1 through 6 are key industry standard devices recommended for new designs.



Table 4 — N-Channel — continued

V(BR)DSS (Volts) Min	rDS(on) @ ID (Ohms) (Amps) Max		Device	I _D (Amps) Max	P _D * (Watts) Max
60	0.085	15	IRF541	27	125
	0.08	12.5	MTP25N06	25	100
			MTP25N06E†	0.0	125
	0.055	17.5	MTP35N06E†	35	
50	0.6	2.5	MTP5N05	5	50
	0.28	5	MTP10N05	10	75
	0.16	7.5	MTP15N05	15	
	0.12	6	BUZ71A	12	40
	1 99 0		MTP12N05E†		
			IRFZ22		
6	0.1		BUZ71	12	
		7.5	MTP15N05E†	15	
			IRFZ20	1/0-	180/

V(BR)DSS (Volts) Min	rDS(or (Ohms) Max	(Amps)	Device	Ip (Amps) Max	PD* (Watts) Max
50	0.1	7	MTP14N05A	14	40
	0.08	0.08 8	MTP16N05A	16	
	0.07	12.5	MTP25N05	25	100
	PLEISOCHTT -	MTP25N05E†		75	
		eriaosiini	IRFZ32	0	er ———
	0.06	15	BUZ11A	70	
	0.05	MTP30N05E†	30	27	
		OFMONHI	IRFZ30	0	
sty stander	0.04	ns a rigue	BUZ11	typen shod	Davice
	0.035	29	MTP45N05E†	45	125
			IRFZ42	46	
	0.028	25	MTP50N05E†	50	LOU
			IRFZ40	51	

Plastic Packages — TO-218 UT bins AANOS-OT) aT #180M newoff lave. Lolpo. J lenns it 0-14 -- T elds T



Table 6 — N-Channel

V(BR)DSS (Volts) Min	rDS(on (Ohms) Max		Device	I _D (Amps) Max	P _D * (Watts) Max
1000	3	2.5	MTH5N100	5	150
950			MTH5N95	USI	
900		3	MTH6N90	6	
850	8		MTH6N85	100	
600	1.2		MTH6N60		
TAV	0.5	4	MTH8N60	8	
550	1.2	3	MTH6N55	6	
TM	0.5	4	MTH8N55	8	
500	0.8	3.5	MTH7N50	7	
TM	0.4	7	MTH13N50	13	
450	0.8	3.5	MTH7N45	7	
TM	0.4	7	MTH13N45	13	
400	0.55	4	MTH8N40	8	
COM.	0.3	7.5	MTH15N40	15	

Table 5 — P-Channel

V(BR)DSS (Volts) Min	rDS(or (Ohms) Max	(Amps)	Device	I _D (Amps) Max	PD* (Watts) Max	
200	0.7	4	MTH8P20	8	125	
180		75	MTH8P18	ē .		
100	0.15	10	MTH20P10	20		
80		85	MTH20P08			
60	0.14	12.5	MTH25P06	25		
50			MTH25P05			

^{* @ 25°}C

Device types shaded in Tables 1 through 6 are key industry standard devices recommended for new designs.

^{* @ 25°}C

[†] Indicates E-FET devices with avalanche energy specified.

Table 6 — N-Channel — continued

V(BR)DSS (Volts) Min	rDS(on) @ ID (Ohms) (Amps) Max		Device (mo)	I _D (Amps) Max	PD* (Watts) Max
350	0.55	4	MTH8N35	8	150
	0.3	7.5	MTH15N35	15	
200	0.16	SCHECKL	MTH15N20		
	0.08	15	MTH30N20	30	
150	0.12	10	MTH20N15	20	
	0.06	17.5	MTH35N15	35	
100	0.07	12.5	MTH25N10	25	
	0.04	20	MTH40N10	40	

V(BR)DSS (Volts) Min	rDS(on (Ohms) Max	(Amps)	Device	(Amps) Max	P _D * (Watts) Max
80	0.07	12.5	MTH25N08	3 0 25	00
	0.04	20	MTH40N08	40	125
60	0.055	17.5	MTH35N06	35	150
	0.028	20	MTH40N06	40	
50	0.055	17.5	MTH35N05	35	na T
	0.028	20	MTH40N05	40	
		25	MTH50N05E	50	125

Device types shaded in Tables 1 through 6 are key industry standard devices recommended for new designs.

Logic Level MOSFETs





Table 7 — N-Channel Logic Level Power MOSFETs (TO-204AA and TO-220AB) — aspailas and additional content of the second sec

V	(BR)DSS (Volts)	rDS(on) (Ohms)	(0)	I _D (Amps)	0.00	I _{D(cont)}	PD @	T _C = 25°C		Package
gq	Min	Max		(ne)801 880()	Device	Amps		Watts		TO-
	150	0.3	(agm	vest 5	MTM10N15L	10		75		204AA
GE W		- MTHISNESO	3.9		MTP10N15L					220AB
7.5	120	MTHSN95	-		MTM10N12L	exa.				204AA
		ODMARTA	67		MTP10N12L					220AB
	100	0.18		6	MTP12N10L	12				
		0.8		2 2	MTP3N10L	3				
	80	0.18	h.	6	MTP12N08L	12			j.q.,	
		0.8	D.	2 0	MTP3N08L	gl 3			301	
	60	0.08	-	12.5	MTM25N06L	25	Sevice	100	mirO)	204AA
		OCHOLLINI OCHOLLINI			MTP25N06L		200-014		- 10	220AB
		0.15	-	7.5	MTM15N06L	15	PaHTM	75		204AA
		26475753	2.0		MTP15N06L	ne ne	Seles ITM		10	220AB
		0.6		2	MTP4N06L	4 RO	SUCHIE	25		
	50	0.08	6	12.5	MTM25N05L	25	AR SHITM	100	8.0	204AA
		COLUMN TO THE STATE OF THE STAT	2.7		MTP25N05L	20			2000	220AB
		0.15		7.5	MTM15N05L	15		75		204AA
			.ongle		MTP15N05L	are key industry ap	a dguard		sbarte	220AB
		0.6		2	MTP4N05L	4		25		

Insulated Gate Bipolar Transistors (GEMFETs)

This relatively new series of power transistors combines the high input resistance of a MOSFET with the low internal on-resistance of a bipolar transistor to provide more efficient performance than either a MOSFET or bipolar device in low-frequency switching service. Recommended for motor drive circuits, home appliances, and other applications where high switching speed is not a requirement. All are N-Channel.

Table 8 — TO-204AA

VBR(CES) (Volts) Min	rCE(or (Ohms) Max	(Amps)	Device	(Amps) Max	PD* (Watts) Max
500	0.27	10	MGM20N50	20	100
	1.6	2.5	MGM5N50	5	50
450	0.27	10 08	MGM20N45	20	100
	1.6	2.5	MGM5N45	5	50

^{* @ 25°}C

TO-204AA







Table 9 — TO-220AB

VBR(CES) (Volts) Min	rCE(on (Ohms) Max	(Amps)	Device	(Amps) Max	PD* (Watts) Max	
500	0.27	10	MGP20N50	20	100	
	1.6	2.5	MGP5N50	5	50	
450	0.27	10	MGP20N45	20 00	100	
	1.6	2.5	MGP5N45	5 00	50	

^{* @ 25°}C

TMOS SENSEFETS**

DPAK

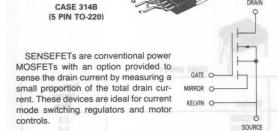


Table 10 - Case 314B

V(BR)DSS (Volts) Min	rDS(on (Ohms) Max		Device	I _D (Amps) Max	PD* (Watts) Max
50	0.028	25	MTP50N05M	50	125
60	0.04	20	MTP40N06M**	40	125
100	0.25	5	MTP10N10M**	10	75
	0.085	12.5	MTP25N10M	25	125
250	1.5	4	MTP4N25M	4	75
	0.45	2	MTP10N25M	10	100
500	1.5	2.5	MTP4N50M	5	75
	0.85	4	MTP8N50M	8	125

^{* @ 25°}C

These devices are planned for introduction.



Table 11 — Case 369A-03 Surface Mount Case 369-03 Insertion Mountable**

V(BR)DSS (Volts) Min	rDS(on (Ohms) Max	(Amps)	Device	ID (Amps) Max	PD* (Watts) Max
500	4	1 MTD2N50		2	20
400	5	0.5	MTD1N40	1001	
200	0.7	2	MTD4N20	4	
150	0.3	3	MTD6N15	6	
100	0.25		MTD6N10		
80			MTD6N08	0.0	
60	0.6	2	MTD4P06†	4	
	0.4	2.5	MTD5N06	5	
	0.15	4	MTD3055E	8	1
50	0.6	2	MTD4P05†	4	1
	0.4	2.5	MTD5N05	5	1
	0.1	5	MTD10N05E	10	1

^{@ 25°}C

^{**}Available from stock.

^{**} Add -1 to part number to order insertion mountable package † Indicates P-Channel

Small-Signal MOSFETs





Table 12 — Switches and Choppers — TO-205AD

V _(DSS) (Volts)	(Ohms)	S(on) @ ID	Amps)	Device			(Amps)	P _D @ T _C = 25°C (Watts)
240	6 10	220AB	0.5 0.5	VN2406B VN2410B			0.63 0.63	2.5 2.5
200 of (extraW) (extraA) xsiM	0.8 0.8 1.5 6.4	on) @ Ic (Amps)	2.25 2 1.5 0.25	2N6790 IRFF220 2N6784 MFE9200	"gill (ellalii) xelli	(Amps) (Amps)	3.5 3.5 2.25 0.4	20 20 15 1.8
170	6	2.5	0.5 0.5	VN1706B VN1710B	1007	20	0.63 0.63	2.5 2.5
001 150 05	12	10	0.1	MFE4150	100	20	0.250	79.0 6.25 084
03 100	0.3	2.5	3	IRFF120	50	8	г.в Эмамамы	8.1 20
90	4		1	2N6661			0.9	6.25
60	3 5		1 0.5	2N6660 MFE910			1.1	6.25 6.25
35	1.8		1	2N6659			1.4	6.25
30	1.2 2.5		1	VN0300B VP0300P			1.25 1.25	6.25 6.25

Table 13 — 4 Pin Dip — Case 370-01

PD @ TC = 25°C	1 Watt Max				U	CAS	E 370-01	stand to	and a digital of	dian
VBR(DSS) (Volts) Min	(Ohm Max	s)	on) @ Ip	(Amp)	Device			sebi ir	ID(Cont (Amp) Max	
200	0.8 epive 1.5	(aqmA)	Ohma) Nex	0.4 0.3	IRFD220 IRFD210				0.8 0.6	.elor
150	02/45012.4			0.3	IRFD213				0.45	h
100	0.6 0.6 0.6 0.6 0.7 0.6 0.6 0.2 0.6	8.5 2 3	9.3 0.7	0.6 0.8 -0.8 -0.3 0.25	IRFD120 IRFD110 IRFD9120 IRFD9110 IRFD1Z0	of (kgmA) Mex	Device	gi e (aqnu)	1.3 (no)2011 (no)2011 -0.7 -0.7	R)(DS (olta) (olta)
60	0.4 0.8 0.8			0.6 0.8 -0.8	IRFD123 IRFD113 IRFD9123			20	0.8 -0.8	
ě	-METDSNOS	2.5	0,4		128	225	MTP26N10M	12.5	0.085	



Table 14 — Plastic — TO-226AA Style 22

V _{(BR)DSS}	rDS(on) (Ohms	(Amp)	Device		ID(Cont) (Amp) Max	P _D @ T _C = 25°C Watts Max
240	6 HTMATTM 10 SECONS	0.5 0.5	VN2406L VN2410L	NTM.	0.158 0.12	0.4 0.4
200	6.4 6.4 14	0.25 0.25 0.2	BS107A MPF9200 BS107		0.25 0.4 0.25	0.6 0.5 0.6
180	140	0.01	MPF481	2007	0.02	0.35
170	6 914441H 10 24034	0.5 0.5	VN1706L VN1710L		0.158 0.12	0.4 0.4
150	12	0.1	MPF4150†		0.25	0.625
80	80	0.01	MPF480		0.08	0.35
60	5 5 5 5 7.5 7.5	0.5 - 0.2 0.2 0.5 0.5	2N7000 BS170P BS170 VN0610LL 2N7008 VN2222LL	36) Out (Annae)	0.5 -0.195 0.195 0.12 1 0.099	0.4 0.4 0.4 0.4 0.4 0.4
30	1.2 (Santa 2.5 (Santa	1.0 -1.0	- CONTRACTOR - CON	188	0.4 -0.2	0.4

†Depletion Mode



CASE 318-02 SOT-23

Table 15 — Surface Mount — Case 318-02 Style 10

V(BR)DSS (Volts) Min		n) @ ID nms) (Amp)	Device	IAPONES MEESTO	ID(Cont) (Amp) Max	P _D @ T _C = 25°C Watts Max	Package
100	6	0.1	BSS123	ZMORNO	0.17	0.2	318-02
60	5 7.5	0.2 0.5	MMBF170 2N7002		0.5 0.8	0.2	318-02 318-02





Table 14 - Plastic - TO-226AA Style 22

Table 16 — TMOS Product Matrix

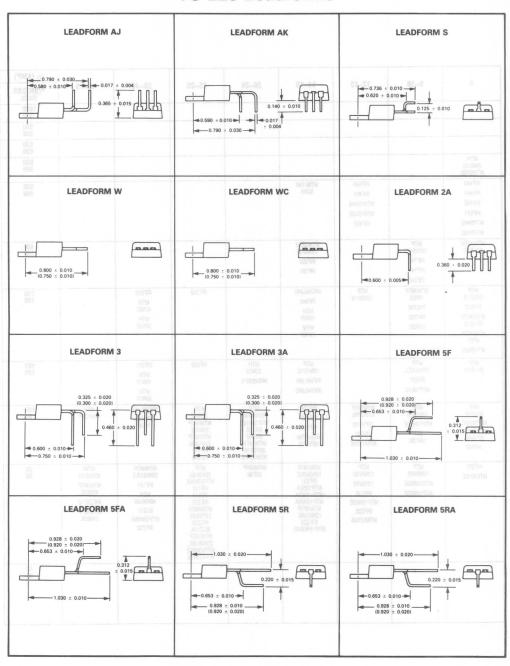
ID (AMP)	9 04 0 00	mo0101	0.0.00	1 1 0	2.20	2 20	4-4.9	E 6	7
V(BR)DSS Volts	0.01-0.49	(c 0.5-0.79	0.8-0.99	1–1.9	2–2.9 epiveG	3–3.9 (qmA)	4-4.9	5–6	7 (88)D88
1000 950		0.158		MTM/MTP 1N100/95	1809-2NA	MTM/MTP 3N100/95	MTM/MTH 8 5N100/95		240
900 850		89.0			MTM/MTP 2N90/85	0.25	MTM/MTP 4N90/85	MTM/MTH 6N90/85	
800 650		4.0			MPP9200	MTM/MTP 3N75/80	5.6 Al	BUZ84,A	
600 550		90.02		MTP 1N60/55	MTP 2N60/55	MTP 3N60/55 MTM3N60	Oh	MTH/MTP 6N60/55 MTM6N60	180
500 450		0.158		MTP 1N50/45	MTP 2N50/45	MTP 3N45/50	MTM/MTP 4N50/45		MTM/MTH 7N50/45
3.625		0.25			MTM2N50 MTM/MTP		2N6762 IRF830-33		IRF842 IRF843
0.35		80.0			2P50/45 IRF820,821,823		00		
400		- 2.6		IDETAG	2N7000	0.5	0110750	LITHIATTO	00
400 350		-0.195 0.195		IRF710	MTP 2N40/35 IRF722	MTP 3N40/45 IRF720	2N6759 MTP 4N35/40	MTM/MTP 5N40/35 2N6760	
0.4		0.12			2N7008		a.	IRF330,331,333 IRF730-33	
250 170	MFE9200 MPF9200	IRFD210 VN2406B	IRFD220	BS170 BS107	2N6784 MTP	IRFF220 IRFF222	MTP 4N18/20	MTP 5N20/18	MTP 7N20/18
\$1.6	BS107,A VN2406L VN2410L	S VN2410B			2N20/18 MTP	MTM/MTP 3P25	IRF620 C	MTM/MTP 5P18/20	
	VN1706B VN1710B MPF481				2N25 IRF610-12	2N6790	MTD4N20	MTM/MTP 5P25	
150 120	IRFD213 MPF4150	IRFD223			IRF610 IRF612	IRFF223 MTP3N12	MTP 5N12/15 IRF621	MTD6N12 MTD6N15	MTP 7N15/12
100 80	BSS123	IRFD120	2N6661	IRFD110	2N6661	2N6782	MTP	MTP	IRF522
80	MPF480	IRFD9110 IRFD1Z0	CASE 318-02 SOT-23	IRFD120 IRFD9120 IRFE110		IRF512 IRFF110	4N10/08,L IRF510	6N08/10 2N6788 IRFF120	
					Style 10	318-02	ount Ca		
	2510	Pa @ Tc =	DiConti				@ (no)@0		V(88)05S
60 50	2N7008 IRFD123	2N7000 BS1700	IRFD113 IRFD9123	IRFD123 MFE910	MPF6660	IRF513	IRF511 MTD4P05	IRFF123 MTP 5N06/05	IRF523 MTP 7P05/06
218-02	VN0610LL VN2222LL	MMBF170 MPF910	2N7002	2N6660 2N7008	\$123	88 0	MTD4P06	MTM/MTP 5P06/05	MTP7N05
318 02 318-02	BS170 BS170P	S.O BS170 S.O	8.0 8.0		/IBF170 7002	.2 NB)	MTD5N05 MTD5N06	Dia
40	VN0300L			VN0300B	MPF6659				
30	VP0300L			VN0300P 2N6659					

MTM Prefix — TO-204 MTP Prefix — TO-220AB MTH Prefix — TO-218AC MTD Prefix — DPAK MFE Prefix — TO-205AD (TO-39) MPF Prefix — TO-226AA (TO-92) IRF100 thru 400 Series — TO-204 IRF500 thru 800 Series — TO-220AB IRFD Prefix — Case 370-01 IRFF Prefix — TO-205AF

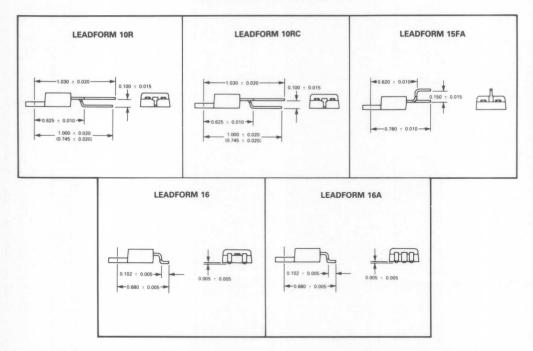
TO-220 Leadforms

	LEADFORM							
8	9–10	12–13	14-19	20–24	25–29	30-40	45–75	I _D (AMP) V(BR)DSS
	10 - 85 C]_[\neg	oran -	947,D		MALAY T		1000 950
		1		DOD 1	(et 0			900 850
								800 650
MTH 8N60/55 MTM8N60								600 550
IRF440 IRF441 IRF840 IRF841 MTP8N45 MTP8N50	LEADFORM:	IRF450 IRF451 MTH13N45 MTH13N50 IRF452	MTM/15N 50/45	LEADFORM W			LEADFORM W	500 450
MTM/MTH 8N40/35	MTP 10N35/40 IRF740 IRF741 IRF340		MTM/MTH 15N40/35 IRF350 IRF351	010.0	000 D + 000 D	Lesere	0100	400 350
MTP 8N20/18 IRF632 MTM/MTH 8P18/20 MTM/MTP 8P25	MTM/MTP 10N25 2N6758 IRF230 IRF630	MTP 12N20/18	IRF240,640 IRF642 MTH 15N20 MTM 15N20		IRF252	IRF250 MTM 40N20 MTH 30N20		250 180
MTM8N20	LEADFORMS		, A	LEADFORM 3			LEADFORMS	
MTP 8N12/15	MTP 10N15/12,L IRF631 MTP10N12		MTP 15N15/12 IRF241,641 IRF243,643	MTH 20N15 MTM20N15	IRF253	IRF251 MTM 45N12 MTH 35N15	0500 ± 655 0	150 120
MTP 8N10/08 MTP8N10E MTM/MTP 8P10/08 IRF520	MTP 10N10/08 MTP10N10E MTP 10N10M	MTM/MTP 12N10/08L 12P10/08 IRF532 MTM12N10	2N6756 IRF130 IRF530 MTH/MTM 15P08/10	MTP 20N10/08 MTP20N10E IRF142 IRF542 MTM/MTH 20P08/10 MTM20N10	MTM 25N10 MTM/MTP 25N10E MTH/MTP 25N10/08 IRF140 IRF540	IRF150,152 MTH40N 10/08	MTM 55N10/08	100
IRF521 MTD3055E	MTP 10N06/05 MTD10N05E MTP10N06E	MTP 12N06/05 12P06/05 IRF533 MTP12N05E	MTM/MTP 15N06/05E IRF531 MTP3055A MTP14N05A MTP16N05A	MTM/MTP 20P06	MTP 25N06/05 MTP25N06E IRF141 IRF541 IRFZ30	MTM/MTH 35N06/05,E IRF151 MTH 40N06/05	MTM 60N06/05 MTM/MTP 45N05E IRFZ40,42	60 50
	LEADFORM 5	IRFZ22 MTM12N05		LEADFORM S	MTM/MTH 25P06/05 IRFZ32 BUZ11A MTM/MTP 25N05/06L MTP25N05E MTM25N05	BUZ11 MTP30N05E IRFZ30	MTM/MTP 50N05E	
Equip	- 055 D J	5 = \$20.0-66 500.0	[mgm]	- 051.0 - 051.0 - 016.0 023.0	D.C = 255,0-bc	Seed line and	DIG0 = 0	40 30

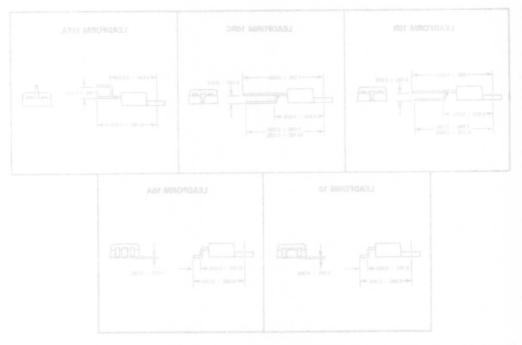
TO-220 Leadforms



TO-220 Leadforms (continued)



Ordering Information: To purchase a leadformed device, contact your local sales office and advise which leadform is required. The sales office will contact the factory and obtain a part number to be used to order the leadformed device.



Ordering Information: To purchase a leadformed device, contact your local sales office and advise which leadform is required. The sales office will contact the factory and obtain a part number to be used to order the leadformed device.

2N6660 MPF6660 2N6661 MPF6661

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

2.0 AMPERE

V-CHANNEL TMOS

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

These TMOS FETs are designed for high-speed switching applications such as switching power supplies. CMOS logic, nucroprocessor or TTL to-high current interface and line drivers.



Data Sheets

3

Viany Davice



CASE 79-02 TO-2050D

Data sheets are arranged in alphanumeric sequence except when information applies to more than one device, e.g., MTM5N35, MTM5N40, MTP5N35 and MTP5N40. Consult the table of contents for these part numbers.

MPFESSO



CASE 29-03

es to m	ore	PINSOSO MPESSSO 1	
ble of	-08		
	00		

THERMAL CHARACTERISTICS

2.5		
0.7		
+ 150		

The Payer Dissipation of the gastege may result in a lower continuous their durrent.
 Poles Vinte & 200 us Daily Date & 200s.

3

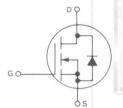
2N6660 MPF6660 2N6661 MPF6661

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

These TMOS FETs are designed for high-speed switching applications such as switching power supplies, CMOS logic, microprocessor or TTL-to-high current interface and line drivers.

- Fast Switching Speed $t_{on} = t_{off} = 5.0 \text{ ns Max}$
- Low On-Resistance 2.0 Ohm Typ 2N6660/2N6661 MPF6660/MPF6661
- Low Drive Requirement, VGS(th) = 2.0 V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices





MAXIMUM RATINGS

Rating	Symbol	2N6660 MPF6660	2N6661 MPF6661	Unit
Drain-Source Voltage	VDSS	60	90	Vdc
Drain-Gate Voltage	V _{DGO}	60	90	Vdc
Gate-Source Voltage	VGS	±	30	Vdc
Drain Current — Continuous (1) Pulsed (2)	I _D	2.0 3.0		Adc

THERMAL CHARACTERISTICS

THEMMAL OHAMAOTEM	01100			
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	6.25 50	2.5 20	Watts mW/°C
Total Power Dissipation	PD			
@ $T_A = 25^{\circ}C$		_	1.0	Watts
Derate above 25°C		_	8.0	mW/°C
Operating and Storage Temperature Range	TJ, T _{stg}	- 55 to + 150		°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.

(2) Pulse Width \leq 300 μ s Duty Cycle \leq 2.0%

2.0 AMPERE

N-CHANNEL TMOS FET

60, 90 VOLTS





CASE 79-02 TO-205AD

than, one device, e.g., MTM5N35, MTI

MPF6660 MPF6661



CASE 29-03 TO-226AE

1 41500 (2)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	es	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS	201100	THEORY	rat publication	rinus r ami	iais	
Drain-Source Breakdown Voltage (VGS = 0, ID = 10 μ A)	2N6660, MPF6660 2N6661, MPF6661	V(BR)DSS	60 90	48. +	=	Vdc
Zero Gate Voltage Drain Current (VDS = Maximum Rating, VGS	= 0)	IDSS	BD OE America	1-	10 m	μAdc
Gate-Body Leakage Current (VGS = 15 V, VDS = 0)	- tooy toglot	IGSS	-	nae o r	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (VDS = VGS, ID = 1.0 mA)	nj [©] tugel	V _{GS(th)}	0.8	1.4	2.0	Vdc
Drain-Source On-Voltage (VGS = 10 V, ID = 1.0 A) $(V_{GS} = 5.0 \text{ V}, I_{D} = 0.3 \text{ A})$	2N6660, MPF6660 2N6661, MPF6661 2N6660, MPF6660 2N6661, MPF6661	VDS(on)	= TAREMAT	 0.9 0.9	3.0 4.0 1.5 1.6	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, I _D = 1.0 Adc)	2N6660, MPF6660 2N6661, MPF6661	rDS(on)		H	3.0 4.0	Ohms
On-State Drain Current (VDS = 25 V, VGS = 10 V)		ID(on)	1.0	2.0	-	Amps
Forward Transconductance (V _{DS} = 25 V, I _D = 0.5 A)	12	9FS	170			mmhos
DYNAMIC CHARACTERISTICS	8.0					8.0
Input Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1.0	MHz)	C _{iss}		30	50	pF
Output Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1.0	MHz)	Coss	1-1	20	40	pF
Reverse Transfer Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1.0	MHz)	C _{rss}	- (0)	3.6	10 g	pF
SWITCHING CHARACTERISTICS*						
Turn-On Time (See Figure 1)		ton	_	_	5.0	ns
Turn-Off Time (See Figure 1)	RE 6 - CAPACITANCE	toff	<u>3</u> 01131	T. CHARACTER	5.0	ns
Diag Time		t _r	- 20		5.0	ns
Rise Time		tf			5.0	ns

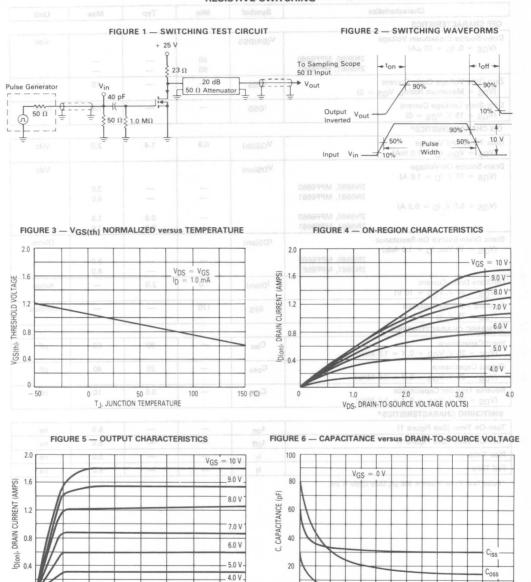
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V_{DS}, DRAIN-TO-SOURCE VOLTAGE (VOLTS)

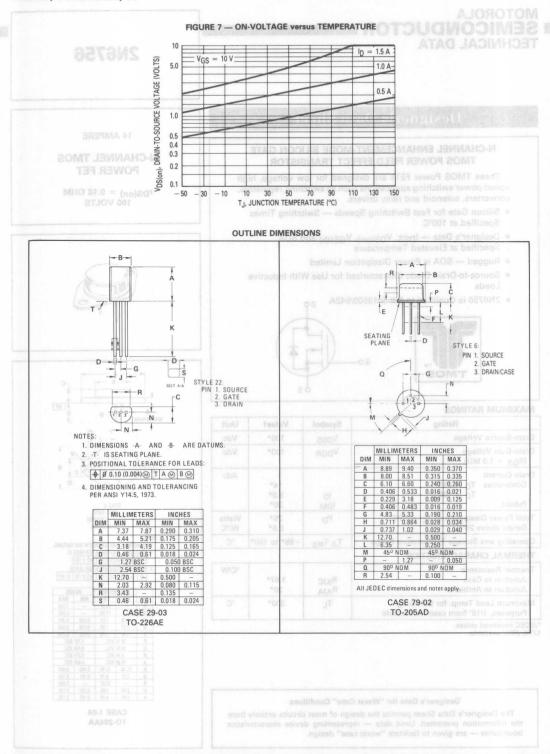
Crss

VDS, DRAIN-TO-SOURCE VOLTAGE (VOLTS)

RESISTIVE SWITCHING PAR = ATT SOITSHEETDARAHO LADIATORIES



0



MOTOROLA ■ SEMICONDUCTOR TECHNICAL DATA

2N6756

Designer's Data Sheet

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive
- 2N6756 is Qualified to Mil-S 19500/542A





MAXIMUM RATINGS

Rating	Symbol	Valuet	Unit
Drain-Source Voltage	V _{DSS}	100*	Vdc
Drain-Gate Voltage 234941 2849344.148 (RGS = 1.0 M Ω) XAM 3441 XAM 3441 IMQ	V _{DGR}	100*	Vdc
	I _D	14* 9.0* 30*	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75* 0.6*	Watts W/°C
Operating and Storage Temperature Range	TJ, Tstg	-55* to 150*	°C

THERMAL CHARACTERISTICS

Thermal Resistance MON 198 AND 198 Bulletin Bull	$R_{ heta JC}$ $R_{ heta JA}$	1.67* 30*	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for seconds	TL	300*	°C

Designer's Data for "Worst Case" Conditions

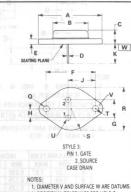
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.

14 AMPERE

N-CHANNEL TMOS POWER FET

 $r_{DS(on)} = 0.18 \text{ OHM}$ 100 VOLTS





	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	-	39.37	_	1.550
В	A2	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15	BSC	1.187 BSC	
G	10.92	BSC	0.430 BSC	
Н	5.46	BSC	0.215 BSC	
J	16.89	BSC	0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	-	26.67	-	1.050
U	2.54	3.05	0.100	0.120
٧	3.81	4.19	0.151	0.165

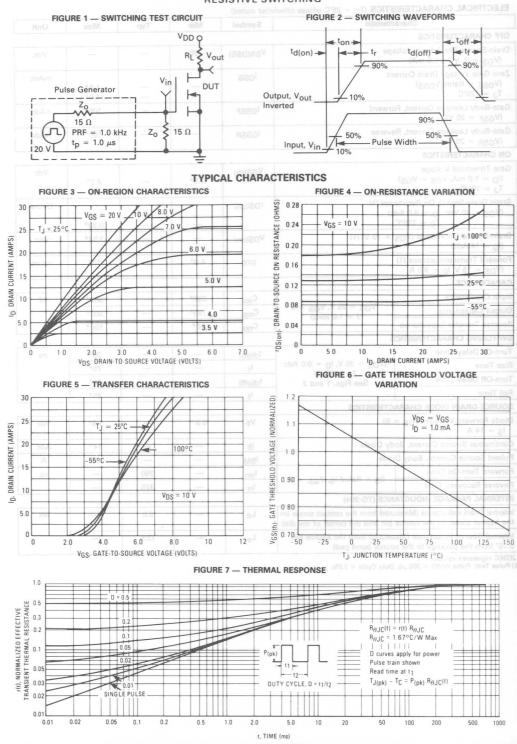
CASE 1-04 TO-204AA

^{*}JEDEC registered values. †JTX, JTXV available.

ELECTRICAL CHARACTERISTICS (To = 25°C unless otherwise noted)

Charact	eristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS	La sel se		o aa₁			
Drain-Source Breakdown Voltag (VGS = 0, ID = 1.0 mA)	e , l — — — (no)bl	V _{BR} (DSS)	100	-	_	Vdc
Zero Gate Voltage Drain Curren (V _{DSS} = Rated V _{DSS}) T _J = 125°C	tpot. Vous	IDSS	TUO —	10V	1.0*	mAdc
Gate-Body Leakage Current, For (VGSF = 20 V)	ward	IGSSF	1	1	100*	nAdc
Gate-Body Leakage Current, Re (VGSR = 20 V)	grad regers	IGSSR	15 0	\$ 0.5	100*	nAdc
ON CHARACTERISTICS	801		-	L		
Gate Threshold Voltage (I _D = 1.0 mA, V _{DS} = V _{GS}) T _J = 100°C	TERISTICS FIGURE 4 ON-RE	V _G S(th)	2.0* 1.5	N C#NRACT	4.0* 3.5 — 8	Vdc
Static Drain-Source On-Resistar ($V_{GS} = 10 \text{ Vdc}$, $I_{D} = 9.0 \text{ Adc}$ $T_{C} = 125^{\circ}\text{C}$		rDS(on)		NE TO	0.18* 0.33*	Ohms
Drain-Source On-Voltage (VGS (ID = 14 Adc)	= 10 V) (1)	V _{DS(on)}	VBB		2.52*	Vdc
Forward Transconductance (1) (V _{DS} = 15 V, I _D = 9.0 A)	81.0	9FS	4.0*		12*	mhos
CAPACITANCE	THE RIVE		A 0.9		1397	
Input Capacitance		Ciss	350*		800*	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0)$ f = 1.0 MHz)	Coss	150*	-	500*	
Reverse Transfer Capacitance	1 - 1.0 (4112)	C _{rss}	50*	-	150*	1
SWITCHING CHARACTERISTICS	0 00					
Turn-On Delay Time	F 6 S0 10 1	td(on)	0.9 0.6	0.11_	30*	ns
Rise Time	(V _{DS} = 36 V, I _D = 9.0 Adc	t _r	1033000	2001201-30100	75*	
Turn-Off Delay Time	$Z_0 = 15 \Omega$ See Figs. 1 and 2	td(off)	2.0112333	E CHARACTE	40*	RUDR
Fall Time	1 1 1 1 1 1 1 1 1	tf			45*	
SOURCE-DRAIN DIODE CHARA	CTERISTICS			14		
Diode Forward Voltage ($V_{GS} = I_S = 14 A$	0)	VF	0.9*	1	1.8*	Vdc
Continuous Source Current, Bo	dy Diode	Is	3900		14*	Adc
Pulsed Source Current, Body D	ode	ISM	-	- 1	30	Α
Forward Turn-On Time	(IS = Rated IS, VGS = 0)	ton		250		ns
Reverse Recovery Time	(IS - Nated IS, VGS = 0)	t _{rr}		325		
INTERNAL PACKAGE INDUCTA	NCE (TO-204)	3	V 01 -	30*		
Internal Drain Inductance (Measu the header closer to the source		Ld		5.0		nH
Internal Source Inductance (Me 0.25" from the package to the s		L _S	BT / 1	12.5	0.5	is o

^{*}JEDEC registered values.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



3

OPERATING AREA INFORMATION

FIGURE 8 - MAXIMUM RATED SWITCHING SAFE OPERATING AREA

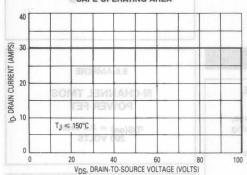
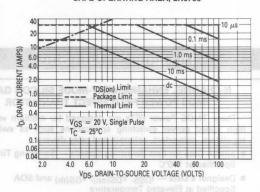


FIGURE 9 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6756



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (TC) of 25°C and a maximum junction temperature (TJ $_{\rm max}$) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (IDM) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D}(25^{\circ}C) \left[\frac{T_{Jmax} - T_{C}}{P_{D} \cdot R_{\theta JC} \cdot r(t)} \right]$$

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the device for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

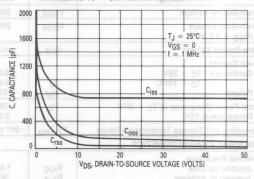
$$\frac{T_{\text{Jmax}} - T_{\text{C}}}{R_{\theta} J C}$$

Where

ID(25°C) = dc drain current at TC = 25°C from Figure 9 = Rated maximum junction temperature

T_{Jmax} = Device case temperature

T_C = Rated power dissipation at T_C = 25°C $R_{\theta JC}$ = Rated steady state thermal resistance r(t) = Normalized thermal response from Figure 7. FIGURE 10 — CAPACITANCE VARIATION



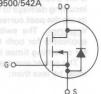
Designer's Data Sheet

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive
 Source-to-Drain Diode Characterized for Use With Inductive Source-to-Drain Diode Characterized for Us
- 2N6758 is Qualified to Mil-S 19500/542A





MAXIMUM RATINGS

Rating MATISAYAS — OF	Symbol	Value†	Unit
Drain-Source Voltage	VDSS	200*	Vdc
Drain-Gate Voltage (RGS = 1.0 MΩ)	VDGR	200*	Vdc
Gate-Source Voltage	VGS	± 20	Vdc
$ \begin{array}{lll} \text{Drain Current} & & & \\ \text{Continuous} & \text{T}_{\text{C}} = 25^{\circ}\text{C} & & \\ & \text{T}_{\text{C}} = 100^{\circ}\text{C} & & \\ \text{Pulsed} & & & \end{array} $	I _D	9.0* 6.0* 15*	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75* 0.6*	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stq}	-55* to 150*	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	$R_{ heta JC}$ $R_{ heta JA}$	1.67* 30*	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for seconds	TL	300*	°C

^{*}JEDEC registered values.

Designer's Data for "Worst Case" Conditions

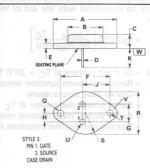
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

9.0 AMPERE

N-CHANNEL TMOS POWER FET

rDS(on) = 0.4 OHM 200 VOLTS





NOTES:

- DIAMETER V AND SURFACE W ARE DATUMS.
 POSITIONAL TOLERANCE FOR HOLE Q:
- ♦ φ 0.25 (0.010) ⊗ W V ®

 3. POSITIONAL TOLERANCE FOR LEADS:

	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	_	39.37	-	1.550
В	-	21.08	_	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15	BSC	1.18	7 BSC
G	10.92	BSC	0.43	BSC
Н	5.48	BSC	0.215	5 BSC
J	16.89	16.89 BSC		5 BSC
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	-	26.67	-	1.050
U	2.54	3.05	0.100	0.120
٧	3.81	4,19	0.151	0.165

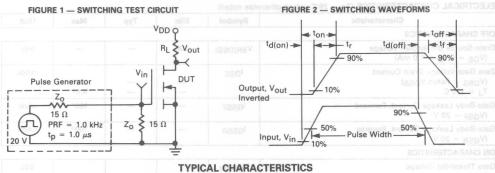
CASE 1-04 TO-204AA

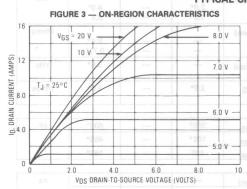
[†]JTX, JTXV available.

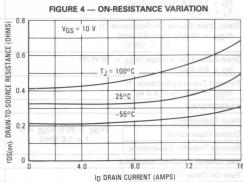
ELECTRICAL CHARACTERISTICS (To = 25°C unless otherwise noted)

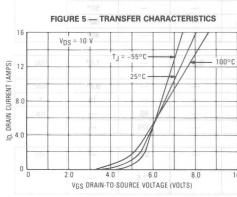
Charact	eristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS			0.00			
Drain-Source Breakdown Voltag (VGS = 0, ID = 1.0 mA)	e 1 4 (no)tr	V _{BR} (DSS)	200	-	_	Vdc
Zero Gate Voltage Drain Curren (V _{DSS} = Rated V _{DSS}) T _J = 125°C	t nov h	IDSS	Tua H	Y= F	1.0* 4.0*	mAdc
Gate-Body Leakage Current, For (VGSF = 20 V)	ward	IGSSF	-	1-1	100*	nAdc
Gate-Body Leakage Current, Re (VGSR = 20 V)	verse	IGSSR	- 1 42 1	300	100*	nAdc
ON CHARACTERISTICS			*	I.		
Gate Threshold Voltage (I _D = 1.0 mA, V _{DS} = V _{GS}) T _J = 100°C	TERNSTICS PIGURE 4 — ON-RI	V _{GS(th)}	2.0* 1.5	RAHO MOID	4.0* 3.5	Vdc
Static Drain-Source On-Resistar (VGS = 10 Vdc, I_D = 6.0 Add T_C = 125°C		rDS(on)	Ī	13/	0.4* 0.75*	Ohms
Drain-Source On-Voltage (VGS (ID = 9.0 Adc)		V _{DS(on)}	k † 1	-	3.6*	Vdc
Forward Transconductance (1) (V _{DS} = 15 V, I _D = 6.0 A)	0.5	9FS	3.0*		9.0*	mhos
CAPACITANCE		vi	10			1
Input Capacitance		Ciss	350*		800*	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0)$ f = 1.0 MHz)	Coss	100*		450*	
Reverse Transfer Capacitance	1 - 1.0 (4112)	C _{rss}	40*		150*	
SWITCHING CHARACTERISTICS	10 9	31	0.8	0.3	0.0	. N
Turn-On Delay Time	MIARO of	td(on)		OMTER LES ETAG	30*20	ns
Rise Time ATJOV GLOHEJAHT	(VGS ≅ 90, ID = 6.0 A	tr	_	_	50*	
Turn-Off Delay Time	$Z_0 = 15 \Omega$) See Figs. 1 and 2	td(off)	eon <u>a</u> maros	SPER_CHARL	50*	
Fall Time		tf	17 + 11	1-1	40*	
SOURCE-DRAIN DIODE CHARA	CTERISTICS		111			0.
Diode Forward Voltage (V _{GS} = I _S = 9.0 A	0)	V _F	0.8*	3000	1.6*	Vdc
Continuous Source Current, Bo	dy Diode	Is	1-4-1		9.0*	Adc
Pulsed Source Current, Body Di	ode	ISM	+ +		15	Α
Forward Turn-On Time	(Is = Rated Is, VGS = 0)	ton	1 + 1	65	-	ns
Reverse Recovery Time	(1S - hated IS, VGS = 0)	t _{rr}	+ 1	325	- 1	
NTERNAL PACKAGE INDUCTA	NCE (TO-204)					
nternal Drain Inductance (Measu the header closer to the source		Ld		5.0	1	nH
Internal Source Inductance (Me 0.25" from the package to the s		L _S	3.0 (VOLTS)	12.5	Ves DRAIN-TO	

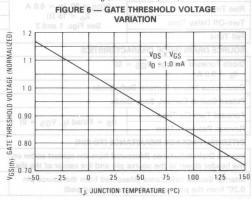
*JEDEC registered values.
(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

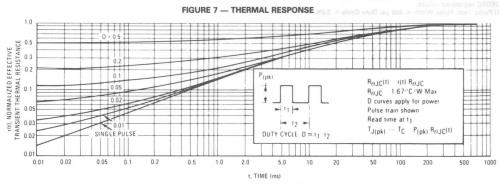












3

OPERATING AREA INFORMATION

FIGURE 8 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

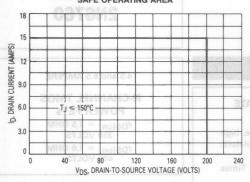
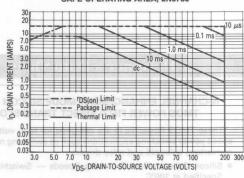


FIGURE 9 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6758



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D}(25^{\circ}C) \left[\frac{T_{Jmax} - T_{C}}{P_{D} \cdot R_{\theta JC} \cdot r(t)} \right]$$

Where

 $I_D(25^{\circ}C) = dc drain current at T_C = 25^{\circ}C from Figure 9$

T_{Jmax} = Rated maximum junction temperature

T_C = Device case temperature

PD = Rated power dissipation at T_C = 25°C

R_{BJC} = Rated steady state thermal resistance

= Normalized thermal response from Figure 7.

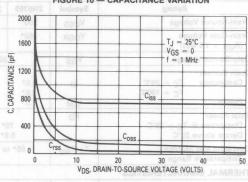
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{\mathsf{T}_{\mathsf{Jmax}} - \mathsf{T}_{\mathsf{C}}}{\mathsf{R}_{\theta}\mathsf{JC}}$$

FIGURE 10 — CAPACITANCE VARIATION





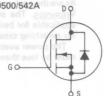
Designer's Data Sheet

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive
- 2N6760 is Qualified to Mil-S 19500/542A





MAXIMUM RATINGS

Rating	Symbol	2N6759	2N6760†	Unit
Drain-Source Voltage	V _{DSS}	350*	400*	Vdc
Drain-Gate Voltage (RGS = 1.0 MΩ)	V _{DGR}	350*	400*	Vdc
Gate-Source Voltage	VGS	-/ ±	20	Vdc
	I _D	4.5* 3.0* 7.0	5.5* 3.5* 8.0	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		5* .6*	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	- 55*	to 150*	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67* 30*	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for seconds	TL	300*	°C

*JEDEC registered values. †JTX, JTXV available.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries - are given to facilitate "worst case" design.

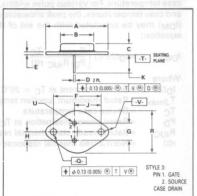
4.5 and 5.5 AMPERE

N-CHANNEL TMOS **POWER FETs**

rDS(on) = 1.5 OHM 350 VOLTS

rDS(on) = 1.0 OHM 400 VOLTS





NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI

. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH. . ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	_	39.37	_	1.550
В	_	21.08	_	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15	BSC	1.187 BSC	
G	10.92	BSC	0.430 BSC	
Н	5.48	BSC	0.215 BSC	
J	16.89	BSC	0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	-	26.67	1-	1.050
U	4.83	5.33	0.190	0.210
٧	3.84	4.19	0.151	0.165

CASE 1-06 TO-204AA

Characteristic		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS			Q 00V			
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 1.0 mA)	2N6759	V _{BR} (DSS)	350	_	_	Vdc
1000	2N6760		400			
Zero Gate Voltage Drain Current (VDSS = Rated VDSS, ID = 1.0 mA) TJ = 125°C		DSS		Y = r-	1.0*	mAdc
Gate-Body Leakage Current, Forward (VGSF = 20V)	Paravi	IGSSF		-	100*	nAdc
Gate-Body Leakage Current, Reverse	Input, Vin	IGSSR	-80	20-1	100*	nAdc
ON CHARACTERISTICS	April 1		-2-			
Gate Threshold Voltage	animalogras	V _G S(th)	ROVT			Vdc
Gate Threshold Voltage (ID = 1.0 mA, VDS = VGS) TJ = 100°C		*GS(th)	2.0* 1.5	ON CHARAC	4.0* 3.5	зяцен
Static Drain-Source On-Resistance (1)	2.0,	rDS(on)		Town N		Ohms
(VGS = 10 Vdc, ID = 3.0 Adc)	2N6759		01 = 32	1/10	1.5*	
$T_{C} = 125^{\circ}C$ (V _{GS} = 10 Vdc, I _D = 3.5 Adc)	2N6760		00-	1,2	3.3* 1.0*	
T _C = 125°C				7-10	2.2*	90 m T
Drain-Source On-Voltage (VGS = 10 V) (1)	2N6759 2N6760	V _{DS(on)}				Vdc
(I _D = 4.5 Adc) (I _D = 5.5 Adc)					7.0* 6.7*	
Forward Transconductance (1) (Vps = 15 V, Ip = 3.5 A)	80 8	g _{FS}	3.0*		9.0*	mhos
CAPACITANCE	- 1					3/1
Input Capacitance	$(V_{DS} = 25 V,$	Ciss	350*		800*	pF
Output Capacitance	$V_{GS} = 0$	Coss	50*		300*	Pr
Reverse Transfer Capacitance	f = 1.0 MHz)	C _{rss}	20*		80*	
SWITCHING CHARACTERISTICS	0 10	orss	20 20 20 20 20 20 20 20 20 20 20 20 20 2	ATHON ROBBIOS	NT WINGS AND	1
Turn-On Delay Time	t-1/>	1913001120		30*	ns	
Rise Time	$(V_{DS} = 175 \text{ V}, I_{D} = 3.5 \text{ Adc} Z_{O} = 15 \Omega)$ See Figs. 1 and 2	t _d (on)	001101027	SARAHO RE	35*	3800
Turn-Off Delay Time		td(off)	T- W		55*	
Fall Time		tf			35*	
SOURCE-DRAIN DIODE CHARACTERIS	TICS			W-	- T	- S01 -
Diode Forward Voltage (VGS = 0)	1103	V _{SD}				Vdc
Is = 4.5 A	2N6759	*50	0.70*	1.40*	, dc	
IS = 5.5 A	2N6760		0.75*		1.50*	
Continuous Source Current, Body Diode	2N6759	Is		1	4.5*	Adc
	2N6760		30	5.5*		
Pulsed Source Current, Body Diode	2N6759 2N6760	ISM		1 = 1/1/	7.0 8.0	Α
Forward Turn-On Time	(Is = Rated Is,	ton	-	250	K-1	ns
Reverse Recovery Time	V _{GS} = 0)	t _{rr}		420	1992	
INTERNAL PACKAGE INDUCTANCE	(TO-204)		E INDICES!	SOURCE VOLUM	V6s GATE-TO	
Internal Drain Inductance (Measured from		Ld	_	5	_	nH
screw on the header closer to the source pin and the center of the die)		VIII - THEREN	BAUDR	1 NH		
Internal Source Inductance (Measured from the source pin 0.25" from the package to the source bond pad)		L _S		12.5		
	lse Width ≤ 300 μs, [Outy Cycle ≤ 2.0	%.	180		
	- gr +					

3

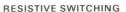
0.01 0.02

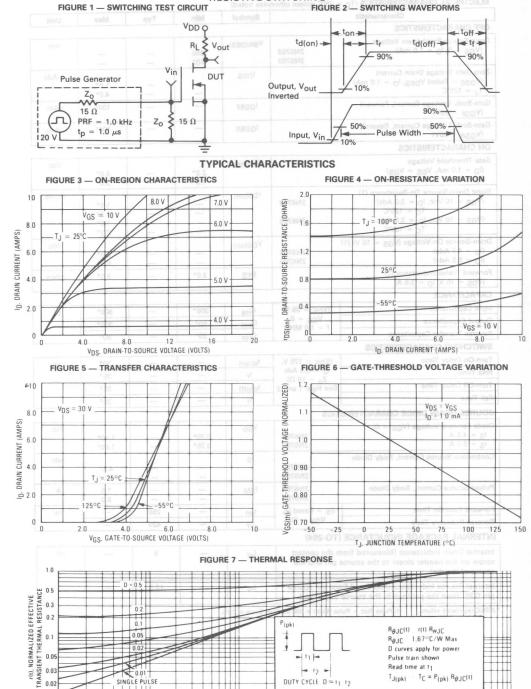
0.05 0.1

0.2

0.5

1.0





5.0

t, TIME (ms)

50

100 200

500 1000

3

OPERATING AREA INFORMATION

FIGURE 8 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6759

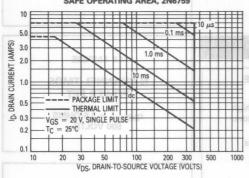


FIGURE 9 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

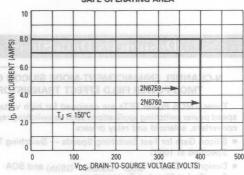
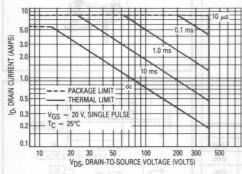


FIGURE 10 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6760



SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 8 and 10 are based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D}(25^{\circ}C) \left[\frac{T_{Jmax} - T_{C}}{P_{D} \cdot R_{\theta JC} \cdot r(t)} \right]$$

ure 7.

Where

 I_D (25°C) = dc drain current at T_C = 25°C from Figure 8 or 10

T_{Jmax} = Rated maximum junction temperature T_C = Device case temperature

PD = Rated power dissipation at T_C = 25°C
R_{BJC} = Rated steady state thermal resistance
r(t) = Normalized thermal response from Fig-

FIGURE 11 — CAPACITANCE VARIATION

2000

1600

1600

VGS = 0

f = 1 MHz

Ciss

Coss

VDS, DRAIN-TO-SOURCE VOLTAGE (VOLTS)

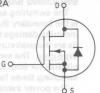
Designer's Data Sheet

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- 2N6762 is Qualified to 19500/542A





MAXIMUM RATINGS

Rating OUAR	Symbol	Valuet	Unit
Drain-Source Voltage	V _{DSS}	500*	Vdc
Drain-Gate Voltage (RGS = 1.0 M Ω)	V _{DGR}	500*	Vdc
Gate-Source Voltage	VGS	± 20	Vdc
Drain Current Continuous $T_C = 25^{\circ}C$ $T_C = 100^{\circ}C$ Pulsed	I _D	0.04	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75* 0.6*	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55* to 150*	°C

THERMAL CHARACTERISTICS

THEINIAL CHARACTERISTICS	71.1	ST SE	
Thermal Resistance Junction to Case Junction to Ambient	R_{θ} JC R_{θ} JA	1.67* 30*	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for seconds	TL	300*	°C

^{*}JEDEC registered values.

Designer's Data for "Worst Case" Conditions

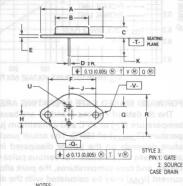
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

4.5 AMPERE

N-CHANNEL TMOS POWER FET

rDS(on) = 1.5 OHMS 500 VOLTS





1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

ALL RULES AND NOTES ASSOCIATED WITH
REFERENCED TO-204AA OUTLINE SHALL APPLY.

	MILLIN	METERS	INC	HES		
DIM	MIN	MAX	MIN	MAX		
A	_	39.37	_	1.550		
В	740	21.08	14	0.830		
C	6.35	8.25	0.250	0.325		
D	0.97	1.09	0.038	0.043		
E	1.40	1.77	0.055	0.070		
F	30.15	30.15 BSC		1.187 BSC		
G	10.92	10.92 BSC		BSC		
H	5.46	5.46 BSC		BSC		
J	16.89	16.89 BSC		BSC		
K	11.18	12.19	0.440	0.480		
Q	3.84	4.19	0.151	0.165		
R	_	26.67	-	1.050		
U	4.83	5.33	0.190	0.210		
V	3.84	4 19	0.151	0.165		

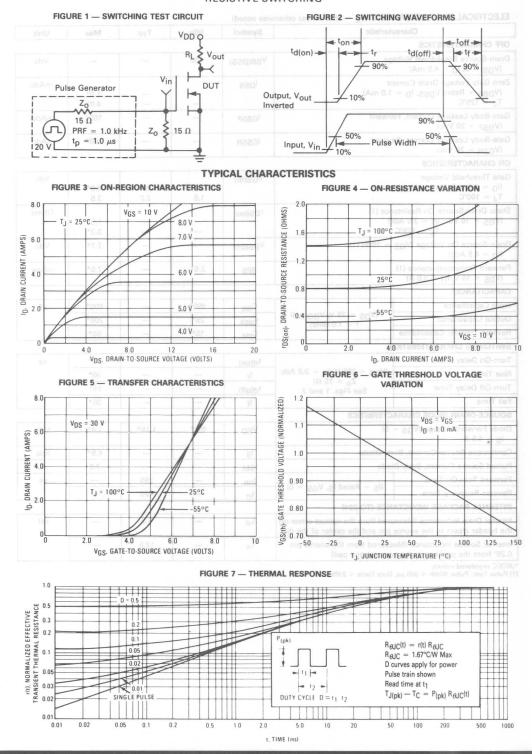
CASE 1-06 TO-204AA

tJTX, JTXV available.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characte	ristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS	est-mo? say		4			
Drain-Source Breakdown Voltage (VGS = 0, ID = 4.0 mA)	208 - 11010	V _{BR} (DSS)	500	-	_	Vdc
Zero Gate Voltage Drain Current (VDSS = Rated VDSS, ID = 1.0 mA) TJ = 125°C		IDSS	TUO	, (=r-	1.0* 4.0*	mAdc
Gate-Body Leakage Current, Forw (VGSF = 20 Vdc)	rard	IGSSF	gar		100*	nAdc
Gate-Body Leakage Current, Reve (VGSR = 20 Vdc)	rse and him augni	IGSSR	-		24 100*	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (I _D = 1.0 mA, V _{DS} = V _{GS}) T _J = 100°C		VGS(th)	2.0* 1.5	2.7	4.0* 3.5	
Static Drain-Source On-Resistance (1) (VGS = 10 Vdc, ID = 3.0 Adc) TC = 125°C		rDS(on)		A DL = 50A	1.5* 3.3*	Ohms
Drain-Source On-Voltage (VGS = (ID = 4.5 Adc)	10 V) (1)	V _{DS(on)}		-5	7.7*	Vdc
Forward Transconductance (1) (V _{DS} = 15 V, I _D = 3.0 A)	25	9FS	2.5*		7.5*	mhos
CAPACITANCE	8.0 8					
Input Capacitance		Ciss	350*		800*	pF
Output Capacitance	(V _{DS} = 25 V, V _{GS} = 0 f = 1.0 MHz)	Coss	25*		200*	
Reverse Transfer Capacitance	1 1.0 11112/	C _{rss}	15*		60*	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	0 gl	td(on)	(STION) 30AN	by to someon vide	30*	ns
Rise Time ATJOV GJOHANNE	V _{DS} = 225 V, I _D = 3.0 Adc	t _r	_		30*	
Turn-Off Delay Time	$Z_0 = 15 \Omega$) See Figs. 1 and 2	td(off)	GULL GELS LONG	Period Traction	55*	N. S.
Fall Time	The second	tf	/// -	- 1	30*	0.8
SOURCE-DRAIN DIODE CHARACT	TERISTICS					
Diode Forward Voltage ($V_{GS} = 0$ $I_{S} = 4.5 \text{ A}$		V _{SD}	0.7*	1.15*	1.4*	Vdc
Continuous Source Current, Body	Diode	Is			4.5*	Adc
Pulsed Source Current, Body Dio	de	ISM		-	7.0	Α
Forward Turn-On Time	//a - Peterd la Van O	ton		250		ns
Reverse Recovery Time (I _S = Rated I _S , V _{GS} = 0)		t _{rr}	3035	420	1-001 = 11	10.4
INTERNAL PACKAGE INDUCTAN	CE (TO-204)		3088	7///		
Internal Drain Inductance (Measure the header closer to the source p		L _d		5.0	-	nH
Internal Source Inductance (Meas 0.25" from the package to the sou		L _S	TAGE (VOITS)	12.5	LO VES-GAT	. 0.

*JEDEC registered values. (1) Pulse Test: Pulse Width $\leq 300~\mu s$, Duty Cycle $\leq 2.0\%$.



3

OPERATING AREA INFORMATION

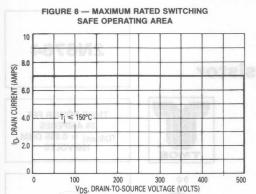
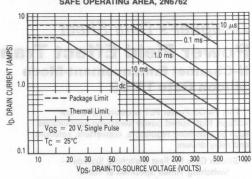


FIGURE 9 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6762



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (Tc) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (IDM) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D}(25^{\circ}C) \left[\frac{T_{Jmax} - T_{C}}{P_{D} \cdot R_{\theta JC} \cdot r(t)} \right]$$

Where

ID(25°C) = dc drain current at TC = 25°C from Figure 9

T_{Jmax} = Rated maximum junction temperature

= Device case temperature

PD = Rated power dissipation at T_C = 25°C = Rated steady state thermal resistance

 $R_{\theta}JC$ = Normalized thermal response from Figure 7.

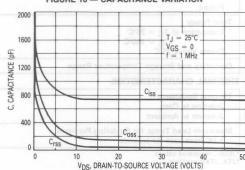
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{\mathsf{T}_{\mathsf{Jmax}} - \mathsf{T}_{\mathsf{C}}}{\mathsf{R}_{\theta \mathsf{JC}}}$$

FIGURE 10 - CAPACITANCE VARIATION



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

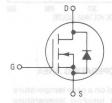
This TMOS Power FET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- 2N6764 is Qualified to Mil-S 19500/543A



2N6764

TMOS POWER FET
38 AMPERES
rDS(on) = 0.055 OHM
100 VOLTS





CASE 197A-02 TO-204AE

MAXIMUM RATINGS ADS prints was set as a contract.

Rating 10 10-110 bas no-111 Rating	duhy cycles.	Symbol	Valuet	Unit
Drain-Source Voltage	frain current	VDSS	100*	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	griwoilot er	V _{DGR}	100*	Vdc
Gate-Source Voltage		VGS	± 20	Vdc
Drain Current Continuous $T_C = 25^{\circ}C$ $T_C = 100^{\circ}C$ $T_C = 100^{\circ}C$ Pulsed	from Figure 9 seraturo	ID OT 10 MONTH	38* 24* 70*	Adc spanish b = (2 dc) ad F = versus T
Total Power Dissipation @ T _C = 25°C T _C = 100°C Derate above 25°C	istance	PD Parel ipation at To e thermal rea nal response	150* 60*	Watts W/°C
Operating and Storage Temperature Range		T _J , T _{stg}	-55* to 150*	°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	0.83*	
Junction to Ambient	$R_{\theta}JA$	30*	
Maximum Lead Temp. for Soldering Purposes,	TL	300*	°C
1/16" from case for seconds			

^{*}JEDEC registered values. †JTX, JTXV available.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Charac	teristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (VGS = 0, ID = 1 mA)	ge	V _{BR} (DSS)	100	_	_	Vdc
Zero Gate Voltage Drain Curren	t 800 80	IDSS				mAdc
(V _{DSS} = Rated V _{DSS}) T _J = 125°C			_ ₹8		1* 4*	X 05
Gate-Body Leakage Current, Fo (VGSF = 20 V)	rward and and	IGSSF			100*	nAdc
Gate-Body Leakage Current, Re (VGSR = 20 V)	verse	IGSSR			100*	nAdc
ON CHARACTERISTICS	3					MI
Gate Threshold Voltage		V _{GS(th)}	V8 -			Vdc
(I _D = 1 mA, V _{DS} = V _{GS})	52.0 至		2*		4*	
T _J = 100°C	(1)		1.5		3.5	Oh
Static Drain-Source On-Resistar (VGS = 10 Vdc, ID = 24 Add		rDS(on)		23	0.055*	Ohms
T _C = 125°C	0 9	0.0	8 _ 8	- 1	0.094*	9.
Drain-Source On-Voltage (VGS (ID = 38 Adc)		V _{DS(on)}	onitalantse	resises Ohe	2.09*	Vdc
Forward Transconductance(1) (V _{DS} = 15 V, I _D = 24 A)		9FS	9*	_	27*	mhos
CAPACITANCE	T T T T T T T T T T T T T T T T T T T		NV T			7
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0 f = 1 MHz)	Ciss	1000*	V8	3000*	pF
Output Capacitance		Coss	500*		1500*	
Reverse Transfer Capacitance	T = T (VITIZ)	C _{rss}	150*	-	500*	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	1 8	t _d (on)			35*	ns
Rise Time	(V _{DS} ≈ 24 V, I _D = 24 Adc	t _r		1	100*	
Turn-Off Delay Time	$Z_0 = 4.7 \Omega$) See Figs. 9 and 10	td(off)		178 20	125*	4
Fall Time	Occings o und to	tf		777	100*	
SOURCE-DRAIN DIODE CHARACT	TERISTICS				Sk.	
Diode Forward Voltage (VGS = IS = 38 A	0)	V _F	0.95*	COURCE VOC	1.9*	Vdc
Continuous Source Current, Bo	dy Diode	Is	asi je nato	ned o c han	38*	Adc
Pulsed Source Current, Body D		ISM	_	_	70	А
Forward Turn-On Time		ton	_	85	_	ns
Reverse Recovery Time	(I _S = Rated I _S , V _{GS} = 0)	t _{rr}		200		
NTERNAL PACKAGE INDUCTAN	CE (TO-204)					positive and
	sured from the contact screw on	Ld	-	5		nH
Internal Source Inductance (Measured from the source pin 0.25" from the package to the source bond pad)		L _S		12.5	70:4	

TYPICAL CHARACTERISTICS

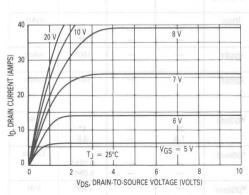
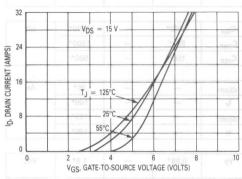


Figure 1. On-Region Characteristics

Figure 2. On-Resistance Variation



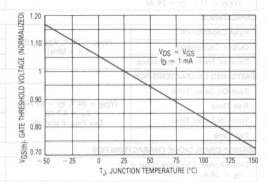


Figure 3. Transfer Characteristics

Figure 4. Gate Threshold Voltage Variation

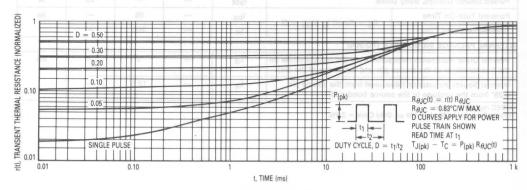


Figure 5. Thermal Response

SAFE OPERATING AREA INFORMATION

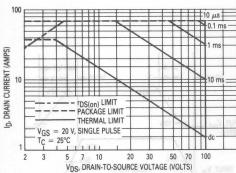


Figure 6. Maximum Rated Forward Biased Safe **Operating Area**

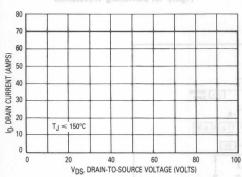


Figure 7. Maximum Rated Switching Safe **Operating Area**

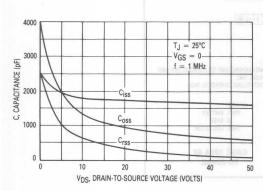


Figure 8. Capacitance Variation

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 6 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (IDM) may be calculated with the aid of the following

$$I_{DM} = I_{D}(25^{\circ}C) \left[\frac{T_{J(max)} - T_{C}}{P_{D^{\bullet}}R_{\theta J}C^{\bullet r(t)}} \right]$$

Where

ID(25°C) = dc drain current at T_C = 25°C from Figure

T_{Jmax} = Rated maximum junction temperature

= Device case temperature TC = Rated power dissipation at T_C = 25°C

PD $R_{\theta JC}$ = Rated steady state thermal resistance

= Normalized thermal response from Figure 5

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 7, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{\mathsf{T}\mathsf{J}(\mathsf{max}) - \mathsf{T}\mathsf{C}}{\mathsf{R}_{\theta}\mathsf{J}\mathsf{C}}$$

RESISTIVE SWITCHING

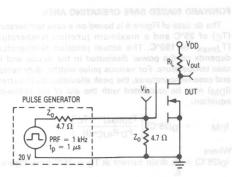


Figure 9. Switching Test Circuit

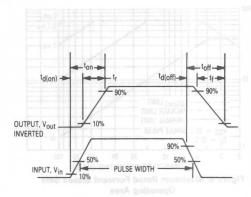
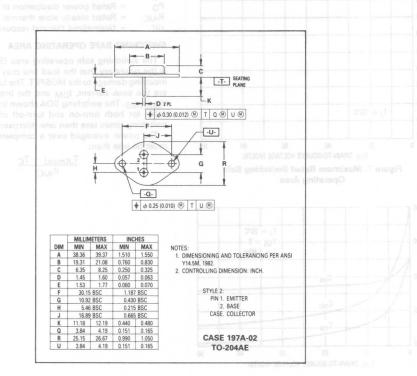


Figure 10. Switching Waveforms



MOTOROLA SEMICONDUCTOR I

Designer's Data Sheet

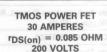
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

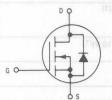
This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- 2N6766 is Qualified to Mil-S 19500/543A





2N6766





CASE 197A-02 TO-204AE

MAXIMUM RATINGS

1200*	Rating	Costs	(shey)	Symbol	Valuet	Unit
Drain-Source Voltage	180*	6210		V _{DSS}	200*	Vdc
Drain-Gate Voltage (RGS = 1 MΩ)		Innati		V _{DGR}	200*	Vdc
Gate-Source Voltage		27	abA E7 = gl	VGS	± 20	Vdc
Drain Current Continuous T _C = 25°C	-	fd(aff)	4.7 (1) (1 and 2	Z _O = See Sigs	30* smfT	Adc
$T_C = 100^{\circ}C$				I _D	19* 60*	all Time
Total Power Dissipation @ T _C = 25°C T _C = 100°C	- *8.0	ą¥.		P _D	150* 60*	Watts
Derate above 25°C				dy Diode		W/°C
Operating and Storage Temper	rature Range	lant		T _J , T _{stg}	-55* to 150*	⊕⊃rric oC ssin

THERMAL CHARACTERISTICS

Thermal Resistance			amit yre	°C/W
Junction to Case Junction to Ambient		$R_{\theta JC}$	0.83* 30*	
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for seconds	(ei bi shi lo se	pin and ^T the cen	300*	olo nel ^o C de ello

^{*}JEDEC registered values. †JTX, JTXV available.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (VGS = 0, ID = 1 mA)	V _{BR} (DSS)	200	-	_	Vdc
Zero Gate Voltage Drain Current (V _{DSS} = Rated V _{DSS}) T _J = 125°C	IDSS	heet	Data S Leter	1* 4*	mAd
Gate-Body Leakage Current, Forward (VGSF = 20 V)	IGSSF	nent-M	папсеп	100*	nAd
Gate-Body Leakage Current, Reverse (VGSR = 20 V)	IGSSR	_	SOM	100*	nAd
ON CHARACTERISTICS	m	d for mediu	T is designa	Power HE	s TMOS
Gate Threshold Voltage (I _D = 1 mA, V _{DS} = V _{GS}) T _J = 100°C	VGS(th)	1.5	er switchin stors <u>.</u> sonve	-	Vdd
Static Drain-Source On-Resistance(1) $(V_{GS} = 10 \text{ Vdc}, I_D = 19 \text{ Adc})$ $T_C = 125^{\circ}\text{C}$	rDS(on)), VGS(th) 8	Switching Specifi ed at 1 SS- VDS ion		Ohm Swittshii Signer
Drain-Source On-Voltage (V _{GS} = 10 V) ⁽¹⁾ (I _D = 30 Adc)	V _{DS(on)}	ipera <u>tu</u> rs tion Limited	evat <u>ed</u> Ten wer Dissips	2.1	Vdd

CAPACITANCE

Input Capacitance		Ciss	1000*	_	3000*	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0)$ f = 1 MHz)	Coss	450*	_	1200*	
Reverse Transfer Capacitance	aadV	C _{rss}	150*	_	500*	Omin-Soura

9FS

9*

mhos

SWITCHING CHARACTERISTICS

Forward Transconductance(1)

 $(V_{DS} = 15 \text{ V}, I_{D} = 19 \text{ A})$

Turn-On Delay Time		t _{d(on)}	_		35*	ns
Rise Time	(V _{DS} ≈ 95 V, I _D = 19 Adc	t _r	_	_	100*	ite-Source
Turn-Off Delay Time	$Z_0 = 4.7 \Omega$ See Figs. 1 and 2	t _d (off)	_	-	125*	
Fall Time	cl cl	tf	_	- 51	100*	

SOURCE-DRAIN DIODE CHARACTERISTICS

Diode Forward Voltage (V _{GS} = 0) I _S = 30 A		V _F	0.9*	25	1.8*	Vdc
Continuous Source Current, Body Diode		IS	_		30*	Adc
Pulsed Source Current, Body Diode		ISM	Range	ounteragme	60	OperAing a
Forward Turn-On Time	(I _S = Rated I _S , V _{GS} = 0)	ton	_	80	RETURNAL	ns
Reverse Recovery Time		t _{rr}	_	200	and the state	Thaymal Sa

INTERNAL PACKAGE INDUCTANCE (TO-204)

Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	Ld	Purposes,	c Soldering	ad Temp. fo	nH Haximum Le
Internal Source Inductance (Measured from the source pin 0.25" from the package to the source bond pad)	L _S		12.5	equit - b	most "8f\f emaiges 3968

^{*}JEDEC registered values.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

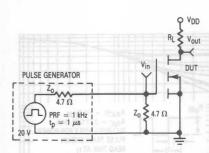


Figure 1. Switching Test Circuit

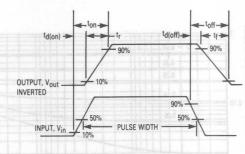


Figure 2. Switching Waveforms

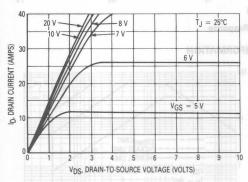


Figure 3. On-Region Characteristics

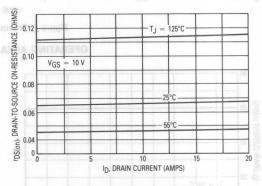


Figure 4. On-Resistance Variation

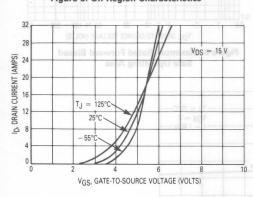


Figure 5. Transfer Characteristics

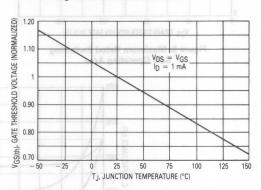


Figure 6. Gate-Threshold Voltage Variation

TYPICAL CHARACTERISTICS

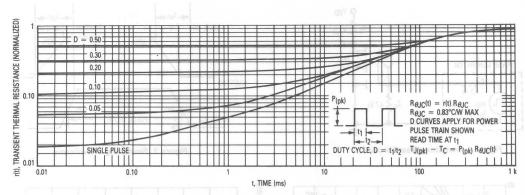
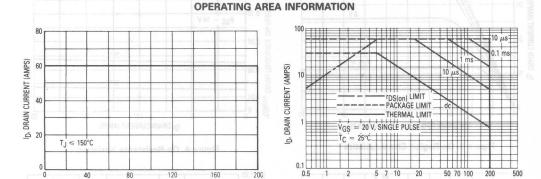
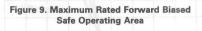


Figure 7. Thermal Response



V_{DS}, DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 8. Maximum Rated Switching
Safe Operating Area



VDS, DRAIN-TO-SOURCE VOLTAGE (VOLTS)

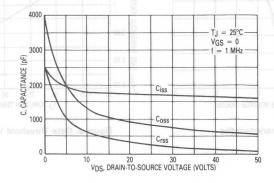


Figure 10. Capacitance Variation

TYPICAL CHARACTERISTICS (continued)

OPERATING AREA INFORMATION (continued)

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D}(25^{\circ}C) \left[\frac{T_{J}(max) - T_{C}}{P_{D} \cdot R_{\theta} J C^{\circ}r(t)} \right]$$

Where

 $I_D(25^{\circ}C) = dc drain current at T_C = 25^{\circ}C from Figure$

T_{Jmax} = Rated maximum junction temperature

T_C = Device case temperature

 P_D = Rated power dissipation at $T_C = 25^{\circ}C$ $R_{\theta JC}$ = Rated steady state thermal resistance

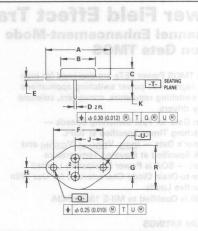
r(t) = Normalized thermal response from Figure 7

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{\mathsf{T}_{\mathsf{Jmax}} - \mathsf{T}_{\mathsf{C}}}{\mathsf{R}_{\theta}\mathsf{JC}}$$



DIMENSIONING AND TOLERANCING PER ANSI

Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

> STYLE 2: PIN 1. EMITTER 2. BASE CASE. COLLECTOR

	MILLIM	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
A	38.36	39.37	1.510	1.550	
В	19.31	21.08	0.760	0.830	
C	6.35	8.25	0.250	0.325	
D	1.45	1.60	0.057	0.063	
E	1.53	1.77	0.060	0.070	
F	30.15	BSC	1.187 BSC		
G	10.92	BSC	0.430 BSC		
Н	5.46	5.46 BSC		BSC	
J	16.89	16.89 BSC		BSC	
K	11.18	12.19	0.440	0.480	
Q	3.84	4.19	0.151	0.165	
R	25.15	26.67	0.990	1.050	
U	3.84	4.19	0.151	0.165	

CASE 197A-02 TO-204AE

MOTOROLA ■ SEMICONDUCTOR **TECHNICAL DATA**

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

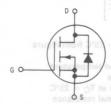
- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- 2N6768 is Qualified to Mil-S 19500/543A



TMOS



2N6768





CASE 1-06 TO-204AA

MAXIMUM RATINGS

Rating		Symbol	Value†	Unit
Drain-Source Voltage		VDSS	400*	Vdc
Drain-Gate Voltage (RGS = 1 MΩ)	rigure o, s without stal limits	VDGR	400*	Vdc
Gate-Source Voltage	,egatiov n	wob V _G S I and	bns ± 20	Vdc
Drain Current Continuous $T_C = 25^{\circ}C$ $T_C = 100^{\circ}C$	evices for	icrosequind.	14* 9* 25*	
Total Power Dissipation @ T _C = 25°C T _C = 100°C Derate above 25°C		P _D	150* 60* 1.2*	Watts W/°C
Operating and Storage Temperature Range		T _J , T _{stg}	-55* to 150*	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	$R_{ heta}$ JC $R_{ heta}$ JA	0.83* 30*	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for seconds	TL	300*	°C

^{*}JEDEC registered values. †JTX, JTXV available.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS	SWITCHING	SALISISSE				
Drain-Source Breakdown Voltage (VGS = 0, I _D = 1 mA)		VBR(DSS)	400		_	Vdc
Zero Gate Voltage Drain Curren (VDSS = Rated VDSS, VGS = TJ = 125°C		IDSS	100 \$ 100	Ξ	1* 4*	mAdc
Gate-Body Leakage Current, Fo (VGSF = 20 V)	rward	IGSSF	TUQ	Vin-	100*	nAdc
Gate-Body Leakage Current, Re (VGSR = 20 V)	verse 180 AVELO	IGSSR	-		100*	nAdc
ON CHARACTERISTICS			0.0	13.5	1001	200 ([7])
Gate Threshold Voltage (ID = 1 mA, VDS = VGS) TJ = 100°C	INPUT, Vin 2 10%	V _{GS(th)}	2* 1.5	=	4* 3.5	Vdc
Static Drain-Source On-Resistar (VGS = 10 Vdc, I_D = 9 Adc) T_C = 125°C	nce(1)	rDS(on)	_ 20	y Test Circ	0.3* 0.66*	Ohms
Drain-Source On-Voltage (V _{GS} = 10 V) ⁽¹⁾ (I _D = 14 Adc)		V _{DS(on)}	IYY -	_	5.6*	Vdc
Forward Transconductance ⁽¹⁾ (V _{DS} = 15 V, I _D = 9 A)		9FS	8*	_	24*	mhos
CAPACITANCE	1		VY	-1/1	Va VDS =	80/
Input Capacitance	V 07 = 80V - 08.0 H	C _{iss}	1000*	1	3000*	pF a
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0)$ f = 1 MHz)	Coss	200*	1	600*	
Reverse Transfer Capacitance	T = T WHZ	C _{rss}	50*	1	200*	es - (T - 28
SWITCHING CHARACTERISTICS	(E) 00				18/	
Turn-On Delay Time		td(on)			35*	ns
Rise Time	$(V_{DS} \approx 180 \text{ V}, I_{D} = 9 \text{ Adc})$	tr	7		65*	
Turn-Off Delay Time	$Z_0 = 4.7 \Omega$ See Figs. 1 and 2	td(off)		-	150*	1
Fall Time		tf			75*	-3
SOURCE-DRAIN DIODE CHARACT	TERISTICS	9 : 10	8 1	8 8	1 3	1 0
Diode Forward Voltage (VGS = (IS = 14) A	0)	V _{SD}	0.85*	O SOURCE VOL	1.7*	Vdc
Continuous Source Current, Bo	dy Diode	Is	_	- Honger	14*	Adc
Pulsed Source Current, Body D	ode	ISM	_	_	25	А
Forward Turn-On Time	(le - Beted le Vee - 0)	ton	Zecht I	175	1-1	ns
Reverse Recovery Time	$(I_S = Rated I_S, V_{GS} = 0)$	t _{rr}		600	-	8/
NTERNAL PACKAGE INDUCTAN	CE (TO-204)		27(0)	1/ o'88 - =	TITI	701
Internal Drain Inductance (Meas the header closer to the source	sured from the contact screw on pin and the center of the die)	L _d	1-1	5	-	nH s
Internal Source Inductance (Me 0.25" from the package to the s		L _S		12.5		10
*JEDEC registered values. (1) Pulse Test: Pulse Width \leq 300 μ s,	Duty Cycle ≤ 2.0%.					1 2

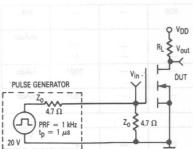


Figure 1. Switching Test Circuit

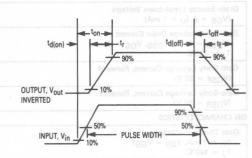


Figure 2. Switching Waveforms

TYPICAL CHARACTERISTICS

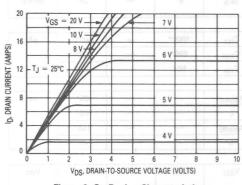


Figure 3. On-Region Characteristics

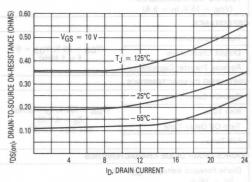


Figure 4. On-Resistance Variation

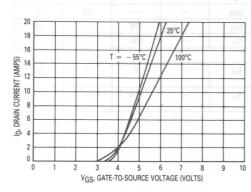


Figure 5. Transfer Characteristics

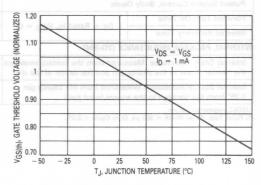


Figure 6. Gate-Threshold Voltage Variation

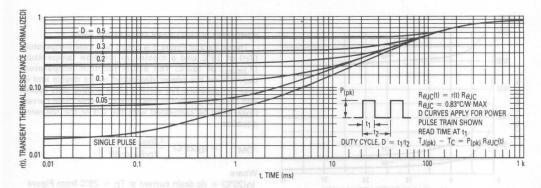


Figure 7. Thermal Response

OPERATING AREA INFORMATION

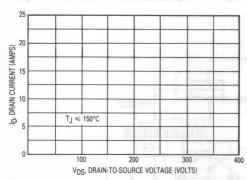


Figure 8. Maximum Rated Switching Safe Operating Area

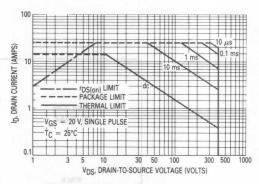


Figure 9. Maximum Rated Forward Biased
Safe Operating Area

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is appli-

cable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:



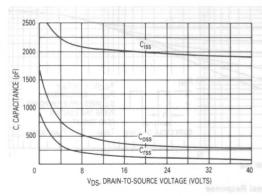


Figure 10. Capacitance Variation

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D}(25^{\circ}C) \left[\frac{T_{J(max)} - T_{C}}{P_{D} \cdot R_{B} \cdot IC^{\bullet}r(t)} \right]$$

Where

 $I_D(25^{\circ}C) = dc drain current at T_C = 25^{\circ}C from Figure$

9.

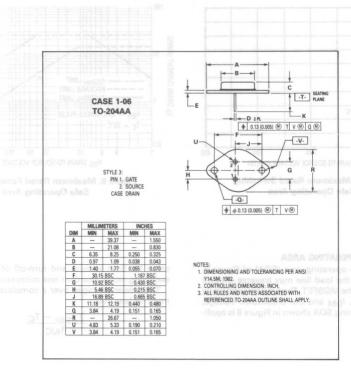
T_{Jmax} = Rated maximum junction temperature

T_C = Device case temperature

 P_D = Rated power dissipation at $T_C = 25^{\circ}C$

 $R_{\theta JC}$ = Rated steady state thermal resistance

Normalized thermal response from Figure 7



MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

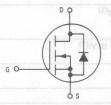
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- 2N6770 is Qualified to Mil-S 19500/543A





2N6770





CASE 1-06 TO-204AA

MAXIMUM RATINGS

	Rating	Seno	= 58 V VGS = 0	Symbol	Valuet	Unit
Drain-Source Voltage	*08	Cent		VDSS	500*	Vdc
Drain-Gate Voltage (RGS = 1 MΩ)				V _{DGR}	500*	Vdc W
Gate-Source Voltage		(80)07	10 V In = 2.75 Ads	VGS	± 20	Vdc
Drain Current Continuous T _C = 25°C	-	(No)b3	(o = 4.7 ft) Figs. 7 and 2	Sel	12****** V	Adc
$T_{C} = 100^{\circ}C$				I _D	7.75* 25*	
Total Power Dissipation @ T _C = 25°C T _C = 100°C	*8.0	osv		PD	150* 60*	Watts Watts
Derate above 25°C				Body Diede	1.2*	W/°C
Operating and Storage Temperatu	re Range	Istw		TJ, Tstg	-55* to 150*	Puls O' Source

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient			0 - 804 81 0818	R_{θ} JC R_{θ} JA	0.83* 30*	NOS RECENTAGES
Maximum Lead Temp. for Soldering Purp 1/16" from case for seconds	ooses,	Pri	the contact screw on he center of the die)	TL mesel	300*	°C

*JEDEC registered values. †JTX, JTXV available. 3

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Charac	teristic	Symbol	Min	Тур	Max	Unit
FF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 4 mA)		V _{BR} (DSS)	500	Data S	s'nen	Vdc
Zero Gate Voltage Drain Currer (VDSS = Rated VDSS, VGS = TJ = 125°C		IDSS	foct	B-bl	1* 1* 4*	mAdo
Gate-Body Leakage Current, Fo (VGSF = 20 V)	rward	IGSSF	W-Inon	NOS	100*	nAdd
Gate-Body Leakage Current, Re (VGSR = 20 V)	verse	IGSSR	ned for hig	are design	*001 Rower FE	nAdd
N CHARACTERISTICS		rious	pplications	switching a	rewog bes	qe rigiri
Gate Threshold Voltage (ID = 1 mA, VDS = VGS) TJ = 100°C	SOMT	VGS(th)	2* 1.5	2.7 2.2	4* 3.5	Vdc
Static Drain-Source On-Resistar $(V_{GS} = 10 \text{ Vdc}, I_D = 7.75 \text{ Ac}$ $T_C = 125^{\circ}\text{C}$		rDS(on)	0 00 0. V <u>GS((h)</u> 9 en <u>utu</u> naq	ss. <u>Vo</u> Ster evat <u>ed</u> Tan	0.4* 0.88*	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) ⁽¹⁾ (I _D = 12 Adc)		V _{DS(on)}	ized for Use	Character	6* and	Vdc
Forward Transconductance ⁽¹⁾ (V _{DS} = 15 V, I _D = 7.75 A)	1	9FS	8* -00	eer e- tiM	b=24* D	mho
APACITANCE	8.0					
Input Capacitance		Ciss	1000*	_	3000*	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0 $ f = 1 MHz)	Coss	200*	_	600*	
Reverse Transfer Capacitance	Voss	C _{rss}	50*	_	200*	
WITCHING CHARACTERISTICS	RadV				(Qn)loV	ets8-nii
Turn-On Delay Time		[†] d(on)	_		35*	ns
Rise Time	$(V_{DS} \approx 210 \text{ V}, I_{D} = 7.75 \text{ Adc} $ $Z_{O} = 4.7 \Omega)$	tr	_	_	50*	711/06-81
Turn-Off Delay Time	See Figs. 1 and 2	td(off)	_	- 0	150*	
Fall Time	Ql .	tf	_	_ 3°	70*	- September 1
OURCE-DRAIN DIODE CHARACT	TERISTICS					- 11
Diode Forward Voltage ($V_{GS} = (I_S = 12) \text{ Å}$	0)	V _{SD}	0.8*	- 3°	1.6*	Vdc
Continuous Source Current, Bo	dy Diode	Is	_	_	12* ªVo	Ado
Pulsed Source Current, Body D	iode T	ISM	-sange-	emp <u>era</u> ture	25 bn	Α
Forward Turn-On Time	(lo - Patad la Vac - 0)	ton	_	200	MARACTER	ns
Reverse Recovery Time	$(I_S = Rated I_S, V_{GS} = 0)$	t _{rr}	_	700	sistan_e	mal.Re
ITERNAL PACKAGE INDUCTAN	CE (TO-204)				o Case to Ambient	notionu
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L _d	Purpores.	soldsing	ead Temp 1	nH
Internal Source Inductance (Measured from the source pin 0.25" from the package to the source bond pad)		L _S	_	12.5	ed vermes.	sitrigen 3 nys VXTL

⁽¹⁾ Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

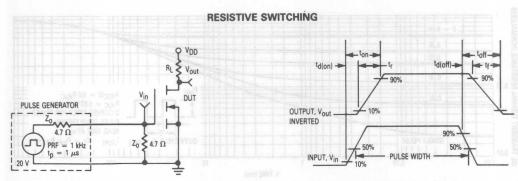


Figure 1. Switching Test Circuit

Figure 2. Switching Waveforms

TYPICAL CHARACTERISTICS

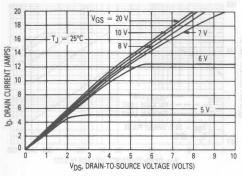


Figure 3. On-Region Characteristics

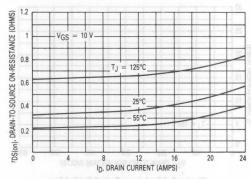


Figure 4. On-Resistance Variation

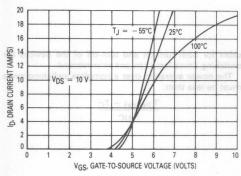


Figure 5. Transfer Characteristics

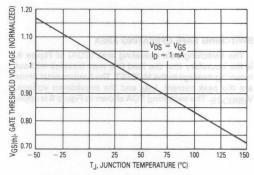


Figure 6. Gate Threshold Voltage Variation



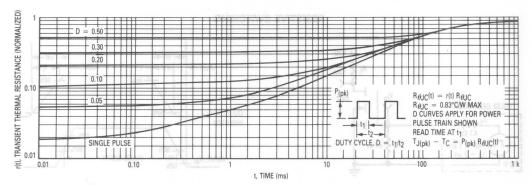


Figure 7. Thermal Response

OPERATING AREA INFORMATION

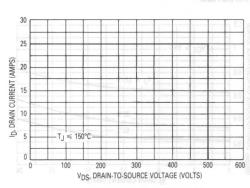


Figure 8. Maximum Rated Switching Safe Operating Area

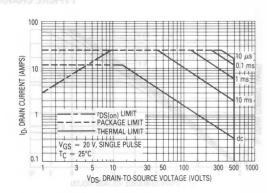


Figure 9. Maximum Rated Forward Biased Safe Operating Area

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is appli-

cable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

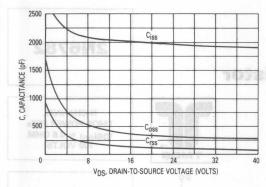


Figure 10. Capacitance Variation

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D}(25^{\circ}C) \left[\frac{T_{J(max)} - T_{C}}{P_{D} \cdot R_{\theta J} C \cdot r(t)} \right]$$

Where

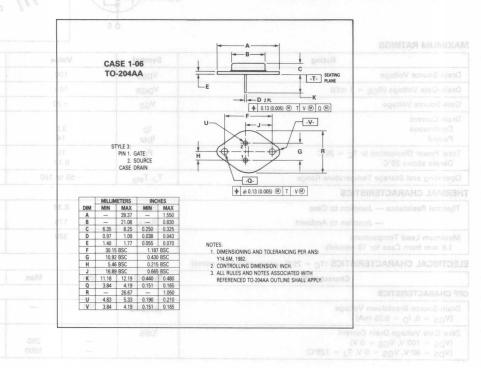
I_D(25°C) = dc drain current at T_C = 25°C from Figure 9.

T_{Jmax} = Rated maximum junction temperature

T_C = Device case temperature

 P_D = Rated power dissipation at T_C = 25°C $R_{\theta JC}$ = Rated steady state thermal resistance

r(t) = Normalized thermal response from Figure 7



Advance Information

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

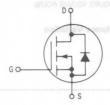
... designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoids, relay drivers, inverters, choppers, audio amplifiers, and high energy pulse circuits.

- Silicon Gate for Fast Switching Speeds
- Low Drive Current Required
- Easy Paralleling
- No Second Breakdown
- Excellent Temperature Stability

2N6782



N-CHANNEL TMOS POWER FETS rDS(on) = 0.6 OHM 100 VOLTS





MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	100	Vdc
Drain-Gate Voltage (RGS = 1 m Ω)	V _{DGR}	100	Vdc
Gate-Source Voltage	V _{GS}	±20	Vdc
Drain Current Continuous Pulsed	I _D	3.5 14	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	15 0.12	Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stg}	-55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	R _θ JC	8.33	°C/W
 Junction to Ambient 	$R_{\theta JA}$	175	
Maximum Lead Temperature 1.6 mm from Case for 10 seconds	TL ST	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	(80.1 - 18.85			
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)	V _{(BR)DSS}	100	-	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$) ($V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125^{\circ}\text{C}$)	IDSS	=	250 1000	μAdo

(continued)

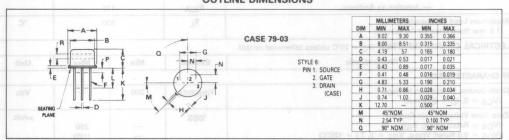
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS			mation	e Inton	ldVanc
Gate-Body Leakage Current, Fore (VGS = 20 Vdc, VDS = 0)	ward Mojalan	IGSSF	Effe	100	nAdc
Gate-Body Leakage Current, Rev (VGS = -20 Vdc, VDS = 0)		IGSSR	nemesi	- 100	nAdc
ON CHARACTERISTICS*			475	MALE DATE	G ROUTH
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 0.5 mA)	Bt.	V _{GS(th)}	beeq 2 agin ,	high Poitage	Vdc
Static Drain-Source On-Resistand (VGS = 10 Vdc, ID = 2.25 Add	The same of the sa	rDS(on)	rs, choppers, pircuit s	0.6 1.08	
Drain-Source On-Voltage (VGS = (ID = 3.5 Adc)	= 10 V)	V _{DS(on)}	- b	eviup 2.1 mem	SevVdc vo.
Forward Transconductance (V _{DS} = 5 V, I _D = 2.25 Adc)	X-1)	gFS	1 valie		mhos
DYNAMIC CHARACTERISTICS	(T-1/2-0)				
Input Capacitance		Ciss	60	200	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	40	100	
Reverse Transfer Capacitance		C _{rss}	10	25	KENDIN RATE
SWITCHING CHARACTERISTICS*	Symbol		Boting		
Turn-On Delay Time	ssav	td(on)	_	15	ov soms
Rise Time 000	$(V_{DD} \approx 34 \text{ V}, I_D = 2.25 \text{ Rated } I_D$	tr	(0)	25	stloV utsD-ris
Turn-Off Delay Time	R _{gen} = 50 ohms)	td(off)	_	25	ate Source Ves
Fall Time		tf	-	20	Inemial nist
SOURCE DRAIN DIODE CHARACT	ERISTICS*				Pursed
Diode Forward Voltage	05	V _{SD}	0.75	1.5	Vdc
Forward Turn-On Time	$(I_S = Rated I_{D(on)})$ $V_{GS} = 0)$	ton	_	Negligible	avodins ad
Reverse Recovery Time	otal LT	t _{rr}	sture Range	200	3 been ns in its

*Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



MOTOROLA

Advance Information

2N6784

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

... designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoids, relay drivers, inverters, choppers, audio amplifiers, and high energy pulse circuits.

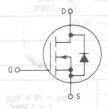
- Silicon Gate for Fast Switching Speeds
- Low Drive Current Required
- Easy Paralleling

3

- No Second Breakdown
- Excellent Temperature Stability



N-CHANNEL TMOS POWER FET rDS(on) = 1.5 OHMS 200 VOLTS





MAXIMUM RATINGS

Rating			Symbol		Value Value	Unit
Drain-Source Voltage	(molts)		V _{DSS}		200 amily yala	□ n0-Vdc
Drain-Gate Voltage (RGS = 1 m Ω)	y)	ni bated in	VDGR	naVi l	200	Vdc
Gate-Source Voltage	(Hojb)	(an	do 03 VGS ag		±20 amiT yala	O 110 Vdc
Drain Current Continuous Pulsed	32		I _D	ENISTIC	2.25 9 AGOIQ MU	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	uo1	(na	(ls = dated lp		15 0.12 m // aD-ma	Watts W/°C
Operating and Storage Temperature Range	197		T _J , T _{stg}		-55 to 150	Я езто°СЯ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	8.33	°C/W
— Junction to Ambient	R_{θ} JA	175	
Maximum Lead Temperature 1.6 mm from Case for 10 seconds	TL	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	IVIII	IVIAX	Unit
DFF CHARACTERISTICS	As A			
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)	V(BR)DSS	200		Vdc
Zero Gate Voltage Drain Current (Vps = Rated Vps, Vgs = 0) (Vps = 0.8 Rated Vps, Vgs = 0, Tj = 125°C)	IDSS	_	250 1000	μAdc

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

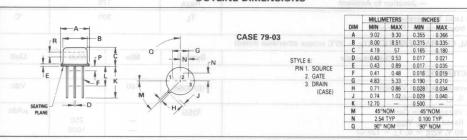


ELECTRICAL	CHARACTERISTICS -	- continued (Tc =	25°C unless otherwise noted)	
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Characteristic		Symbol	Min	Max	Unit
FF CHARACTERISTICS			nouse	intorm	1Vance
Gate-Body Leakage Current, Forw (VGS = 20 Vdc, VDS = 0)	ard Totala	IGSSF	Effec	100	nAdc
Gate-Body Leakage Current, Reve (V _{GS} = -20 Vdc, V _{DS} = 0)	rse	IGSSR	-ineme	-100	nAdc
N CHARACTERISTICS*				ALINIA MA	DEF HOUSE
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 0.5 mA)		V _{GS(th)}		igh v Araga, as switching	
Static Drain-Source On-Resistance (VGS = 10 Vdc, I _D = 1.5 Adc)	T _A = 25°C T _A = 125°C	rDS(on)		1.5 2.81	Ohms on one of a second
Drain-Source On-Voltage (V _{GS} = (I _D = 2.25 Adc)	10 V)	V _{DS(on)}	_	3.37	Vdc W
Forward Transconductance (V _{DS} = 5 V, I _D = 1.5 Adc)	A (-1)	9 _{FS}	0.9	2.7	mhos
YNAMIC CHARACTERISTICS	A)				
Input Capacitance	8.0	Ciss	60	200	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	20	80	
Reverse Transfer Capacitance	. , , , , , , , , , , , , , , , , , , ,	C _{rss}	5	25	WITAR MUM
WITCHING CHARACTERISTICS*	Symbol		pnire?	1	
Turn-On Delay Time	\$80V	td(on)	_	15	uloV ens 28-n
Rise Time	$(V_{DD} \approx 75 \text{ V}, I_{D} = 1.5 \text{ A},$	t _r		20	n-Gata Voltage
Turn-Off Delay Time	R _{gen} = 50 ohms)	td(off)	_	30	s-Source Valta
Fall Time		tf	-	20	m:Current
OURCE DRAIN DIODE CHARACTE	RISTICS*				peals
Diode Forward Voltage	a9	V _{SD}	0.7	= 1.5 none	Masic Vdc _o 9 is
Forward Turn-On Time	$(I_S = Rated I_{D(on)})$ $V_{GS} = 0)$	ton	_	Negligible	ns
Reverse Recovery Time	BIEL TA	t _{rr}	290 (Typ)	age T <u>ar</u> mperati	prie bains alles

^{*}Pulse Test Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Advance Information

2N6788

Power Field Effect Transistor

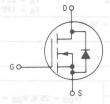
N-Channel Enhancement-Mode Silicon Gate TMOS

... designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoids, relay drivers, inverters, choppers, audio amplifiers, and high energy pulse circuits.

- Silicon Gate for Fast Switching Speeds
- Low Drive Current Required
- Easy Paralleling
- No Second Breakdown
- Excellent Temperature Stability



N-CHANNEL TMOS POWER FET rDS(on) = 0.3 OHM 100 VOLTS





MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	100	Vdc
Drain-Gate Voltage (RGS = 1 m Ω)	VDGR	100	Vdc
Gate-Source Voltage	(a arto (VGS nag)9	±20	Vdc
Drain Current Continuous Pulsed	I _D	6 24	Adc
Total Power Dissipation (a T _C = 25°C Derate above 25°C Derate above 25°C	(mp)Gl PD	20 égadeV bi 0.16 emit eC e	Watts W/°C
Operating and Storage Temperature Range	TJ, T _{sta}	-55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	6.25	°C/W
— Junction to Ambient	$R_{\theta}JA$	175	
Maximum Lead Temperature 1.6 mm from Case for 10 seconds	TL	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
DFF CHARACTERISTICS			THE	
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)	V(BR)DSS	100		Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 80 V, VGS = 0, TJ = 125°C)	IDSS	=	250 1000	μAdc

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

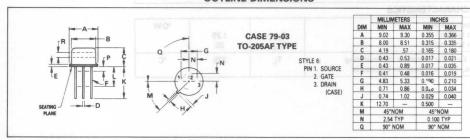


ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
FF CHARACTERISTICS		31	Shee	ir's Data	esigne
Gate-Body Leakage Current, Forw (VGS = 20 Vdc, VDS = 0)	vard	GSSF	юПЗ	100	nAdc
Gate-Body Leakage Current, Reve (VGS = -20 Vdc, VDS = 0)	erse	IGSSR	entrent	- 100	nAdc
N CHARACTERISTICS*			-	AND STREET	In the second
Gate Threshold Voltage (VDS = VGS, ID = 1 mA)	o recorder	V _{GS(th)}	2	Fower PETS are	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 3.5 Adc)	e T _A = 25°C T _A = 125°C	rDS(on)	elay drivers ig Speeds -	0.3	Ohm O
Drain-Source On-Voltage (V _{GS} = (I _D = 6 Adc)	10 V) berhae	V _{DS(on)}	(on) , V GS(1.8 — 8.1 emperature	Vdc
Forward Transconductance (VDS = 5 V, ID = 3.5 Adc)	tive Loads	g _{FS}	1.5	4.5	mhos
YNAMIC CHARACTERISTICS					
Input Capacitance		C _{iss}	200	600	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	100	400	
Reverse Transfer Capacitance		C _{rss}	20	100	
WITCHING CHARACTERISTICS*				SEM	DAN IN CHINA
Turn-On Delay Time	JINU ESBORIS II	td(on)		40	ns
Rise Time	$(V_{DD} \simeq 35 \text{ V}, I_{D} = 3.5 \text{ A})$	t _r		70	
Turn-Off Delay Time	R _{gen} = 50 ohms)	t _d (off)	-	40	
Fall Time		tf		70	
OURCE DRAIN DIODE CHARACTE	RISTICS*	ál		0 Te = 2000	Continuous is
Diode Forward Voltage	8.6	V _{SD}	0.8	91.8 oT	Vdc
Forward Turn-On Time	$(I_S = Rated I_D(on))$ $V_{GS} = 0)$	ton		Negligible	ns
Reverse Recovery Time	anaw GS GV	t _{rr}	- J 0a	230	ns

^{*}Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



2N6823

Designer's Data Sheet

Power Field Effect Transistor

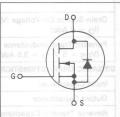
N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FETs **3 AMPERES** rDS(on) = 2.8 OHMS 600 VOLTS



MAXIMUM RATINGS

Rating	Symbol	2N6823	Unit
Drain-Source Voltage	V _{DSS}	600	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	600	Vdc
Gate-Source Voltage	V _{GS}	± 20	Vdc
Drain Current Continuous @ T _C = 25°C T _C = 100°C	I _D	3 2.5 15	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	100 0.8	Watts W/°C
Operating Junction Temperature Range	TJ	-65 to 150	°C
Storage Temperature Range	T _{stg}	-65 to 175	°C



CASE 1-06 TO-204AA

THERMAL CHARACTERISTICS

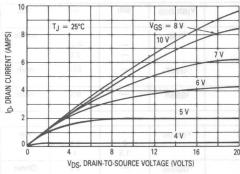
Thermal Resistance Junction to Case Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.25 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	z T _L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Charac	eteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	III B	V(BR)DSS	600	- T	Vdc	
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0	, T _J = 125°C)	IDSS	=	0.25 2.5	mAdc	
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	a voru	· IGSSF	72	500	nAdc	
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	60 00	IGSSR		500	nAdc	
ON CHARACTERISTICS*	8.0					
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C		VGS(th)	2 1.5	4.5	Vdc	
Static Drain-Source On-Resistance (VGS = 10 Vdc, I _D = 3 Adc)		rDS(on)	On-Region C	2.8	Ohms	
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 3 Adc) (I _D = 2.5 Adc, T _J = 100°C)		V _{DS(on)}	=	8.4 15	Vdc	
Forward Transconductance (V _{DS} = 15 V, I _D = 2 A)		9FS	1.5	7.5	mhos	
DYNAMIC CHARACTERISTICS	Vos = 0			A 62 - 90 A		
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 11	Ciss	400	1000	pF	
Output Capacitance		Coss	40	200		
Reverse Transfer Capacitance		C _{rss}	10	100		
SWITCHING CHARACTERISTICS* (TJ	= 100°C)					
Turn-On Delay Time	(V _{DD} = 125 V, I _D = 2 A R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(on)	N-1	50	ns	
Rise Time		tr	1	100		
Turn-Off Delay Time		td(off)	179/1	180		
Fall Time		tf	1-70	80		
Total Gate Charge	$(V_{DS} = 0.8 \text{ Rated } V_{DSS}, \\ I_D = \text{Rated } I_D, V_{GS} = 10 \text{ V}) \\ \text{See Figure 12}$	Qg	16 (Typ)	20	nC	
Gate-Source Charge		Qgs	8 (Typ)	-		
Gate-Drain Charge		Q _{gd}	8 (Typ)	1 10 0 10 01		
SOURCE DRAIN DIODE CHARACTERIS	TICS*				•	
Forward On-Voltage	(lo = 3 A	V _{SD}	0.7	1.5	Vdc	
Forward Turn-On Time	(I _S = 3 A, V _{GS} = 0)	ton	Limited	by stray inc	nductance	
Reverse Recovery Time		t _{rr}	- 1	500	ns	
NTERNAL PACKAGE INDUCTANCE	al a					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L _d	5 (Typ)		nH	
Internal Source Inductance (Measured from the source pin, 0. to the source bond pad)	25" from the package	L _S	12.5 (Typ)		2	

Figure 5. On-Resistance venue Brain Current

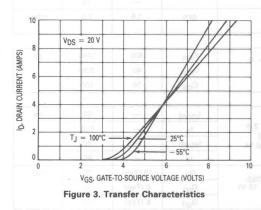
TYPICAL ELECTRICAL CHARACTERISTICS



1.1 VOS = VGS ID = 1 mA VO

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



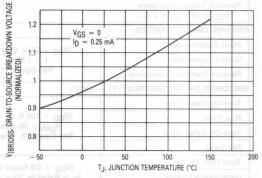
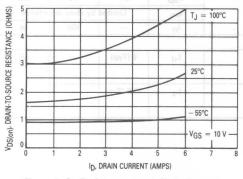


Figure 4. Breakdown Voltage Variation
With Temperature



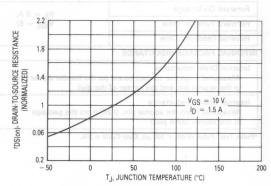


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

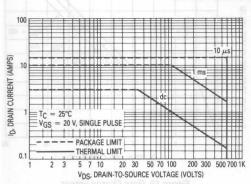


Figure 7. Maximum Rated Forward Biased Safe Operating Area

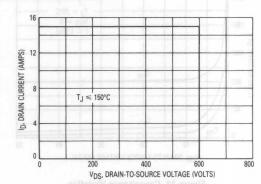


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

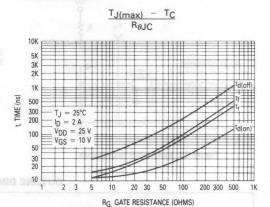


Figure 9. Resistive Switching Time Variation versus Gate Resistance

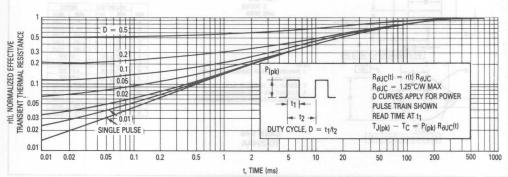
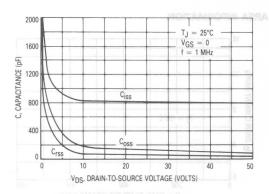


Figure 10. Thermal Response



TJ = 25°C VDD = 480 VDD = 300 VDD = 300 VDD = 100 VDD = 100 ODD = 100 VDD =

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING ARRA DMITARRIO BRAZ GRAWROS

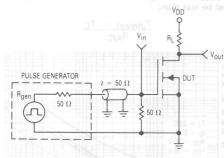


Figure 13. Switching Test Circuit

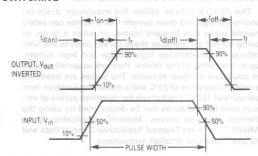
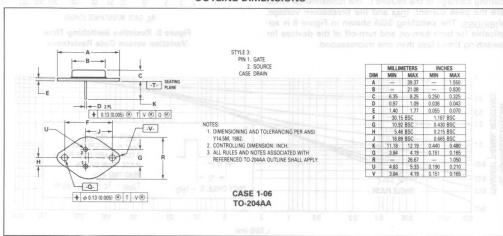


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

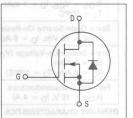
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



2N6826

TMOS POWER FETS 6 AMPERES rDS(on) = 1.6 OHM 600 VOLTS



MAXIMUM RATINGS

00 Rating 8V	Coss	Symbol	2N6826	Unit
Drain-Source Voltage	Cras	V _{DSS}	600	Vdc
Drain-Gate Voltage $(R_{GS} = 1 M\Omega)$	count.	V _{DGR}	600	Vdc
Gate-Source Voltage	2173 (62)	VGS	±20	Vdc
Drain Current Continuous @ $T_C = 25^{\circ}C$ $T_C = 100^{\circ}C$	(Ito)b ¹		5 ET . 6 6 3 14 9 7 4	Adc
Pulsed	22 0	IDM	30	
Total Power Dissipation @ T _C = 25° Derate above 25°C	OC ₈₈	PD	150	Watts W/°C
Operating Junction Temperature Rai	nge by D	TJ	-65 to 150	°C
Storage Temperature Range		T _{stg}	-65 to 175	°C



CASE 1-06 TO-204AA

THERMAL CHARACTERISTICS CONTROL OF THE CHARACTERISTICS

THE THE STATE OF T			
Thermal Resistance Junction to Case Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Char	acteristic			Symbol	Min	Max	Unit
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)				V _{(BR)DSS}	600	0.5	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS} , V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS} , V_{GS} =	0, T _J = 12	5°C)	ransi	IDSS	M3 b	0.25 2.5	mAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	rd		8	IGSSF	105 me	500	nAdc
Gate-Body Leakage Current, Rever (VGSR = 20 Vdc, V _{DS} = 0)	se		oltage,	IGSSR	are design	500 Power PET	nAdc
ON CHARACTERISTICS*	RT VIGER	-alug	witching re	ns such as sv	oussilggs gr	rer switchin	voq bese
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C	4040445		ing Times	VGS(th)	1.5	4.5	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 6 Adc)		no	mbegs AU	rDS(on)	(no <u>1</u> 80 V	1.6	Ohm
Drain-Source On-Voltage (VGS = $(I_D = 6 \text{ Adc})$) ($I_D = 4 \text{ Adc}$, $T_J = 100^{\circ}\text{C}$)	10 V)	Loads	avisoubni	V _{DS} (on)	haracterized	9.6 13.6	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 4 A)			-	9FS	2	10	mhos
DYNAMIC CHARACTERISTICS							
Input Capacitance	()/	DS = 25 V, V _{GS}	- n	Ciss	750	1500	pF
Output Capacitance	Units	f = 1 MHz	Symbol	Coss	75	400	
Reverse Transfer Capacitance	abV	See Figure 11		C _{rss}	25	150	/ estucid-
SWITCHING CHARACTERISTICS* (T.	= 100°C)	800	RadV			0.64	-Gate Voin
Turn-On Delay Time				t _d (on)		80	ns
Rise Time		DD = 125 V, ID =		tr		150	Source
Turn-Off Delay Time	Se	R _{gen} = 50 ohms e Figures 9, 13 an	s) id 14	td(off)	_	200	Current stimuous
Fall Time		à.		tf	- 1	100	
Total Gate Charge	(Vr	os = 0.8 Rated V	MO	Qg	55 (Typ)	65	nC
Gate-Source Charge		Rated ID, VGS =		Qgs	25 (Typ)	28 nonsqua	rvods ete
Gate-Drain Charge	31	See Figure 12	- 7	Q _{gd}	30 (Typ)	fion Travel	not palte
SOURCE DRAIN DIODE CHARACTER	STICS*	-65 to 176	r fa T			ecell witten	on Tamos
Forward On-Voltage		(I _S = 6 A,	-	V _{SD}	0.7	1.4	Vdc
Forward Turn-On Time	W3*	$V_{GS} = 0$		ton	Limited	by stray ind	uctance
Reverse Recovery Time			SueFF	t _{rr}	_	1000	ns
NTERNAL PACKAGE INDUCTANCE		30	AL971			Jagaday	4 of ubital
Internal Drain Inductance (Measured from the contact scree to the source pin and the center		ader closer		L _d	5 (Typ)	for n case	nH
Internal Source Inductance (Measured from the source pin, to the source bond pad)).25" from th	ne package		L _S	12.5 (Typ)	_	

^{*}Pulse Test: Pulse Width \leqslant 300 $\mu\text{s},$ Duty Cycle \leqslant 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

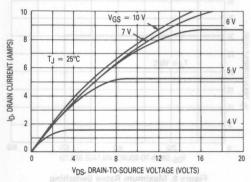


Figure 1. On-Region Characteristics

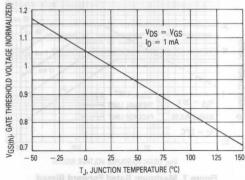


Figure 2. Gate-Threshold Voltage Variation With Temperature

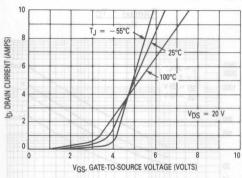


Figure 3. Transfer Characteristics

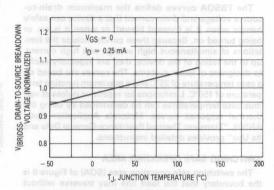


Figure 4. Breakdown Voltage Variation
With Temperature

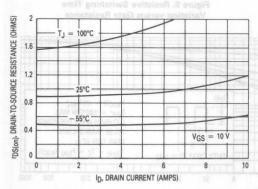


Figure 5. On-Resistance versus Drain Current

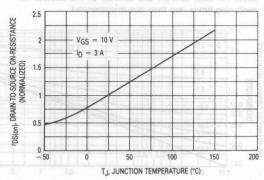


Figure 6. On-Resistance Variation
With Temperature

Figure 7. Maximum Rated Forward Biased
Safe Operating Area

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BRIDSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

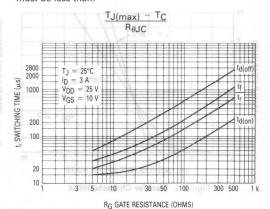


Figure 9. Resistive Switching Time Variation versus Gate Resistance

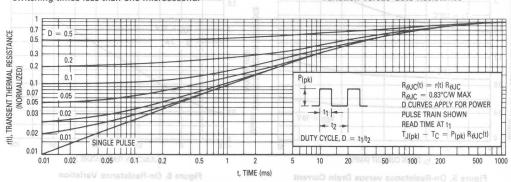


Figure 10. Thermal Response

VDS = 200 V

90

300 V

480 V

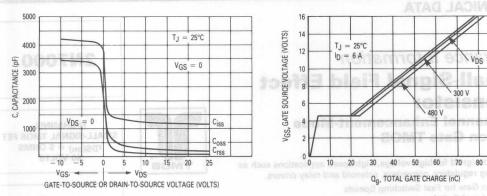


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus **Gate-to-Source Voltage**

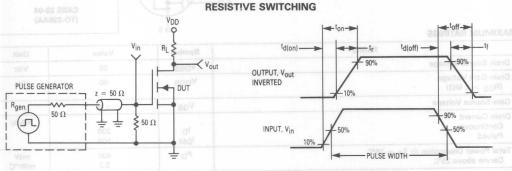
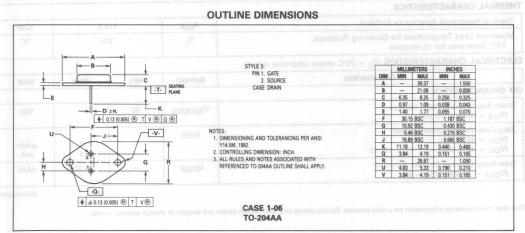


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms



2N7000

Advance Information

Small-Signal Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

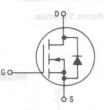
... are designed for high voltage, high speed applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds

- Logic Level Switch
 CMOS Logic Interface
 Bipolar Darlington Replacement
- Lamp Relay Driver or Buffer
- Analog Signal Switching



N-CHANNEL **SMALL-SIGNAL TMOS FET** rDS(on) = 5 OHMS 60 VOLTS





MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	60	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	60 ROTARS	Vdc
Gate-Source Voltage	VGS	±40	Vdc
Drain Current Continuous Pulsed	I _D	200	mAdc
Total Power Dissipation @ T _A = 25°C Derate above 25°C	PD	400 3.2	mW mW/°C
Operating and Storage Temperature Range	T _J , T _{sta}	-55 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Ambient	$R_{\theta JA}$	312.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/16" from case for 10 seconds	TL	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	309002 5	Symbol	Min	Max	Unit
FF CHARACTERISTICS	Michael Service	800	No.		3
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 10 μA)		V(BR)DSS	60	0 1 2	Vdc
Zero Gate Voltage Drain Current (VDS = 48 V, VGS = 0) (VDS = 48 V, VGS = 0, T_J = 125°C)	EP DOMENSION OF THE TOTAL WIND DOMESTIC ON THE TOTAL WIND THE TOTAL THE TOTAL WORLD WIND THE TOTAL WORLD WORLD WIND THE TOTAL WORLD	IDSS	30	1	μAdc mA
Gate-Body Leakage Current, Forward (VGSF = 15 Vdc, VDS = 0)	Y249A ZJANS SWITTED FAMOS OT GEORGISHON	IGSSF	1-14	-10	nAdc

(continued)

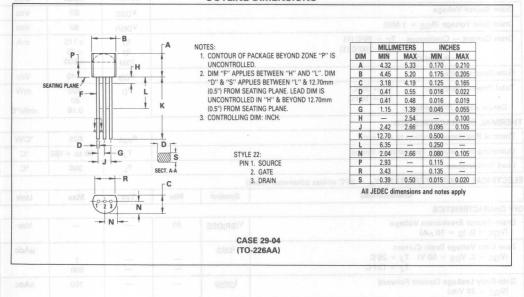
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
N CHARACTERISTICS*					
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA)		VGS(th)	0.8	otni e	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 0.5 Adc) (VGS = 10 Vdc, ID = 0.5 V, T_C = 125°C)		rDS(on)	16	5 9	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V, I _D = 0.5 Adc) (V _{GS} = 4.5 V, I _D = 75 mA)		V _{DS(on)}	nce <u>r</u> ner	2.5 0.4	Vdc
On-State Drain Current (VGS = 4.5 V, VDS = 10 V)		I _{D(on)}	75	84.1 (B) 191	mA
Forward Transconductance (V _{DS} = 10 V, I _D = 200 mA)	eaw y	9fs	100	ch as line de	μmhos
YNAMIC CHARACTERISTICS		anone.	ilidela onotio	dollar aco	Marcel Passes
Input Capacitance		Ciss	_	60	pF d
Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz	Coss	TT-	25	rface Nau
Reverse Transfer Capacitance		C _{rss}	1982 50	5	allable in
WITCHING CHARACTERISTICS*					
Turn-On Delay Time	V _{DD} = 15 V, I _D = 500 mA	ton		10	ns
Turn-Off Delay Time	Rgen = 25 ohms, R _L = 25 ohms	toff	_	10	

^{*}Pulse Test Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

OUTLINE DIMENSIONS



2N7002

Advance Information

Small-Signal Field Effect Transistor

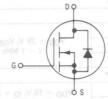
N-Channel Enhancement-Mode Silicon Gate TMOS

This TMOS FET is designed for high-speed switching applications such as line drivers, relay drivers, CMOS logic, or microprocessor interface applications.

- General Purpose Switch
- Hybrid Assemblies
- Surface Mount Package
- Available in 8 mm Tape and Reel



N-CHANNEL SMALL-SIGNAL TMOS FET rDS(on) = 7.5 OHM 60 VOLTS





CASE 318-02 SOT-23

MAXIMUM RATINGS

Rating SMOISMSMIG SMLITUO	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	60	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	60	Vdc
Drain Current — Continuous $T_C = 25^{\circ}C$ (1) $T_C = 100^{\circ}C$ (1) — Pulsed (2)	I _D I _D	± 115 ± 75 ± 800	mA
Gate-Source Voltage MA DA MID TO DAY THE MEMORE ENTER A TO MID IS	V _{GS}	± 40	Vdc
Total Power Dissipation $T_C = 25^{\circ}C$ and the property of t	л P _D	200 80 0.16	mW/°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Ambient		- 0 -	$R_{\theta JA}$	625	°C/W
Operating and Storage Temperature Range	STYLE 22:	2 1777	TJ	-55 to +150	°C
Lead Temperature	PIK 1 SOURCE 2 CATE	AA.1588	TL	300	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
FF CHARACTERISTICS	•		M G	2	
Drain-Source Breakdown Voltage (VGS = 0, ID = 10 μ A)	V _{(BR)DSS}	60	art [J] is	_	Vdc
Zero Gate Voltage Drain Current (VGS = 0, VDS = 60 V) TJ = 25°C	IDSS	_	_	1	μAdo
T _J = 125°C		_	_	500	
Gate-Body Leakage Current Forward (VGS = 20 Vdc)	IGSSF	_	_	100	nAdo
Gate-Body Leakage Current Reverse (VGS = -20 Vdc)	IGSSR	_	-	- 100	nAdd

(1) The Power Dissipation of the package may result in a lower continuous drain current.

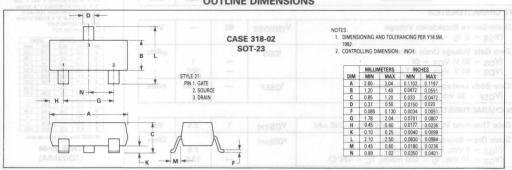
(2) Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Characteristic	Symbol	Min	Тур	Max	Unit
ON CHARACTERISTICS*				was dead	i o me
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μA)	VGS(th)	t bol/i-tri	nceme	2.5	Vdc
On-State Drain Current (V _{DS} ≥ 2 V _{DS(on)} , V _{GS} = 10 V)	I _D (on)	500	-80	ate-TW	mA
Static Drain-Source On-State Voltage (VGS = 10 V, I _D = 500 mA) (VGS = 5 V, I _D = 50 mA)	as doVDS(on) as	speed appli pid a <u>nd</u> rela	sitage, high rters, solem	3.75 1.5	Vdc o
	rDS(on)		- ds	7.5 13.5 7.5 13.5	Ohms no sidali ani silamo
Forward Transconductance (V _{DS} ≥ 2 V _{DS(on)} , I _D = 200 mA)	9 _{FS}	80	-	AUG 1 5511	mmhos
DYNAMIC CHARACTERISTICS				SONU	MUM RAT
Input Capacitance (VDS = 25 V, VGS = 0, f = 1 MHz)	Ciss	-	go	50	pF
Output Capacitance (VDS = 25 V, VGS = 0, f = 1 MHz)	Coss	-	(i) in 1	25	pF
Reverse Transfer Capacitance (VDS = 25 V, VGS = 0, f = 1 MHz)	C _{rss}	_	_	5 90000	pF
SWITCHING CHARACTERISTICS*	-150- -150-				andunum
Turn-On Delay Time $(V_{DD} = 30 \text{ V, } I_{D} \cong 200 \text{ m}$	A, td(on)	-	cycle	20	ns
Turn-Off Delay Time $R_G = 25 \Omega$, $R_L = 150 \Omega$)	td(off)	_		20	wod ns
BODY-DRAIN DIODE RATINGS					
Diode Forward On-Voltage (I _S = 11.5 mA , V _{GS} = 0 V)	V _{SD}	_	- 80	- 1.5	MAY CHA
Source Current Continuous (Body Diode)	oge Is	g Purposes,	to Solderin	- 115 www.agmaT	mA head mumi
Source Current Pulsed	ISM		_	-800	mA



TECHNICAL DATA

Small-Signal Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

... are designed for high voltage, high speed applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Relay Driver

3

- Telecommunication Switch
- Available on Radial Tape and Reel
- Automatic Insertable
- Available in Amo Pack

TMOS

2N7008

N-CHANNEL **SMALL-SIGNAL TMOS FET** rDS(on) = 7.5 OHMS 60 VOLTS





OUTLINE DIMENSIONS

UNCONTROLLED.

2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" B" "S" APPLIES BETWEEN "L" & 12.70mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70mm (0.5") FROM SEATING PLANE.

3. CONTROLLING DIM: INCH.

-	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
В	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
Н	-	2.54		0.100
1	2.42	2.66	0.095	0.105
K	12.70		0.500	-
L	6.35	-	0.250	-
N	2.04	2.66	0.080	0.105
P	2.93	-	0.115	-
R	3.43	-	0.135	-
S	0.39	0.50	0.015	0.020

CASE 29-04 (TO-226AA)

MAXIMUM RATINGS

08 Rating —	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	60	Vdc
Drain-Gate Voltage (RGS = 1 m Ω)	VDGR	60	Vdc
Gate-Source Voltage	VGS	± 40	Vdc
Drain Current Continuous Pulsed	I _D	150 1000	mAdc
Total Power Dissipation (a T _A = 25°C Derate above 25°C	PD	400 3.2	mW mW/°C
Operating and Storage Temperature Range	TJ, T _{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Ambient	$R_{\theta JA}$	312.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/16" from case for 10 seconds	TL	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS				
Drain-Source Breakdown Voltage (VGS = 0, ID = 100 μ A)	V(BR)DSS	60	_	Vdc
Zero Gate Voltage Drain Current (Vps = 50 V, Vgs = 0) (Vps = 50 V, Vgs = 0, Tj = 125°C)	IDSS	_ 58	1 500	μAdc
Gate-Body Leakage Current, Forward (VGSF = 30 Vdc, VDS = 0)	IGSSF	-	- 100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$)	V _{GS(th)}	1	2.5	Vdc
Static Drain-Source On-Resistance (VGS = 5 Vdc, ID = 50 mAdc) (VGS = 10 Vdc, ID = 500 mAdc, TC = 125°C)	rDS(on)	1-1	7.5 13.5	Ohm

^{*}Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

Characte	Sy	mbol	Min	Max	Unit		
CHARACTERISTICS* (continued)							
Drain-Source On-Voltage		Physical Company	VD	S(on)			Vdc
(V _{GS} = 5 V, I _D = 50 mA) (V _{GS} = 10 V, I _D = 500 mA)						1.5 3.75	1
On-State Drain Current			1-		500	3.75	
$(V_{GS} = 10 \text{ V}, V_{DS} \ge 2 \text{ V}_{DS(on)})$			l iD	(on)	500		mA
Forward Transconductance (VDS ≥ 2 VDS(on), ID = 200 mA)			OCTAIN	9fs	80	N-CHANI TMOS F	μmhos
NAMIC CHARACTERISTICS		doticus boos	a daid as	antinu de	ist and top min	ata al EUD S7	MAT SLIT
nput Capacitance		CMOS legic		iss	as lin o drive	50	pFIII
Output Capacitance		$V_{GS} = 0$,		oss	HOV POIN-OH	25	mic oprope
	f = 1 I	MHz				2101	display de
Reverse Transfer Capacitance			nyl an i	rss	= nel b	Spidal	Ne2 tast 6
VITCHING CHARACTERISTICS*			Т.	HOM.	5.0 Ohme	20	Land mode
Turn-On Delay Time	V _{DD} = 30 V, I _I		me	on	mysoV Ina	20	ns
	Rgen = 25 ohms,	NE = 130 OII	1113	off	idena) pnini	20	breverini .
ulse Test Pulse Width ≤ 300 μs, Duty Cy	cie ≤ 2%.		1			vices	Many De
1.8 T _A = 25°C			'				25°C/
1.6			V	DS = 10 V		-55°C/	
	VGS	= 10 V	0.8		20000	1//	125°C
13		9 V				1//	
1.4 1.2 1 0.8 0.6 0.4		8V 5	0.6			11/	
		7 V				///	
0.8			0.4				
0.6		6 V-	8	1		- N	
0.4			à 0.2 ├──			SE SYL	
0.2		4 V -	80				
0 1 2 3 4 5	6 7 8	9 10	0	1 2	3 4 5	6 7	8 9 1
V _{DS} , DRAIN SOURCE VO					SS, GATE SOURCE		
Figure 1. Ohmi	c Region			Figu	ire 2. Transfe	er Characte	ristics
2.2	2/113	1 6	1.2				
V _{GS} = 10 V	MA I	NIZE NIZE	1.15				V _{DS} = V _{GS}
1.8 ID = 200 mA		J. B.	1.1	1			ID = 1 mA
(i) 1.6		Z	1.05				
(NORWALIZED) 1.6 1.4 1.2	TOM	TAG	1				
NO 10		10/	0.95				
≥ 1.2		JOH JOH	0.9				
		Veskith, THRESHOLD VOLTAGE (NORMALIZED)	0.85			000	
2.4 2.2 V _{GS} = 10 V 2 1.8 1.8 1.6 1.6 1.6 1.6 0.8		F	0.8	Total de		500	
5 0.6 0.4	6 1 -	#38(#	0.75	1082 1983		100	31 14
-60 -20 +20	+60 +100	+ 140	0.7 L - 60	- 20	0 + 20	+60	+ 100 + 14
T, TEMPERATU					T, TEMPERATI		Source Voltage
Figure 3. Temperature vers On-Resist				Tempera			shold Voltage
SSRO ARRO BEAUTIES							

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

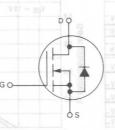
BS170

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

This TMOS FET is designed for high-voltage, high-speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor or TTL-to-high voltage interface and high voltage display drivers.

- \bullet Fast Switching Speed $t_{on} = t_{off} = 6.0$ ns Typ
- Low On-Resistance 5.0 Ohms Max
- Low Drive Requirement, VGS(th) = 3.0 V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices





MAXIMUM RATINGS

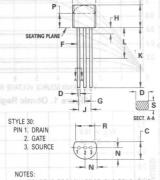
Rating	Symbol	Value	Unit
Drain-Source Voltage	VDSS	60	Vdc
Gate-Source Voltage	VGS	± 20	Vdc
Drain Current — Continuous (1)	ID	0.5	Adc
Total Power Dissipation @ T _C = 25°C	PD	0.83	Watts
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.

60 VOLTS

N-CHANNEL TMOS FET





- CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
- ONDOWNOLLIS

 O'M" "APPLIES BETWEEN "H" AND "L". DIM
 "O" & "S". APPLIES BETWEEN "L" & 12.70mm
 (0.5") FROM SEATING PLANE. LEAD DIM IS

 UNCONTROLLED IN "H" & BEYOND 12.70mm
 (0.5") FROM SEATING PLANE.

 O'MTROLLING DIM: INCH.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
В	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
Н	_	2.54	_	0.100
J	2.42	2.66	0.095	0.105
K	12.70	-	0.500	1-
L	6.35	-	0.250	-
N	2.04	2.66	0.080	0.105
Р	2.93	_	0.115	-
R	3.43	_	0.135	-
S	0.39	0.50	0.015	0.020

CASE 29-04 TO-226AA

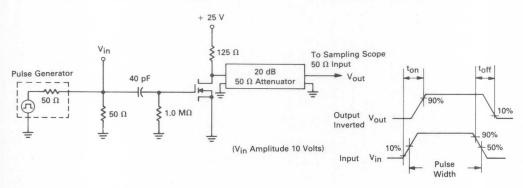
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristics		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					4	
Drain-Source Breakdown Voltage (VGS = 0, I _D = 100 μA)	8/ 1	V(BR)DSS	60	90	-	Vdc
Gate-Body Leakage Current (VGS = 15 V, VDS = 0)		IGSS	-	0.01	10	nAdc
ON CHARACTERISTICS*				-	-	
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1.0 mA)	8.0	V _{GS(th)}	0.8	2.0	3.0	Vdc
On-State Drain Current (V _{DS} = 25 V, V _{GS} = 0 V)	0.0	ID(off)			0.5	μΑ
Static Drain-Source On-Resistance (V _{GS} = 10 V, I _D = 200 mA)		rDS(on)	700	1.8	5.0	Ohms
Forward Transconductance OT MARC 2017 (VDS = 10 V, ID = 250 mA)		9FS	_ 30	200	DIUL LT—	mmhos
DYNAMIC CHARACTERISTICS						
Input Capacitance (VDS = 10 V, VGS = 0, f = 1.0 MHz)	URE 6 — CAF	C _{iss}	80 41 81831	60 TU	9TUO 3RU	pF
SWITCHING CHARACTERISTICS*		V 01 =				
Turn-On Time (I _D = 0.2 A) See Figure 1	08	ton vae		4.0	10	ns
Turn-Off Time (I _D = 0.2 A) See Figure 1		t _{off} V ⁰⁸		4.0	10	ns
*Pulse Test: Pulse Width ≤ 300 us. Duty Cycle ≤ 2	10/	E lune				18

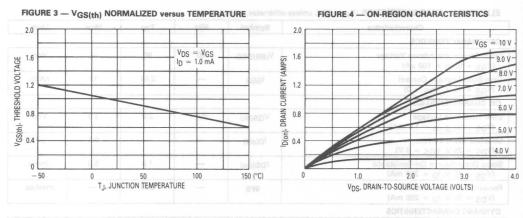
RESISTIVE SWITCHING

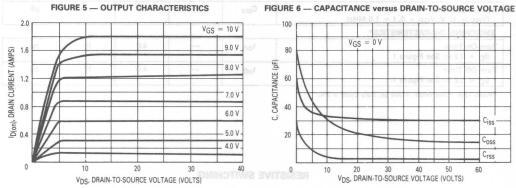
FIGURE 1 — SWITCHING TEST CIRCUIT

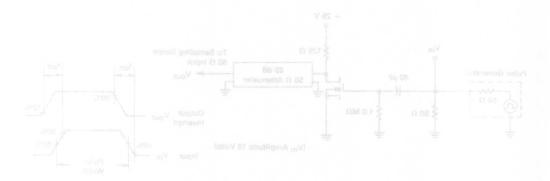
FIGURE 2 — SWITCHING WAVEFORMS











MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Advance Information

Small-Signal Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

This TMOS FET is designed for high-voltage, highspeed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor or TTL-tohigh voltage interface and high-voltage display drivers.

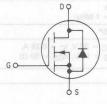
- Low On-Resistance 6 Ohms Typ
- Surface Mount Package





N-CHANNEL SMALL-SIGNAL TMOS FET rDS(on) = 6 OHMS 100 VOLTS

BSS123





CASE 318-02 SOT-23

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	VDSS	100	Vdc
Gate-Source Voltage	VGS	±20	Vdc
Drain Current Continuous (1) Pulsed (2)	I _D	0.17 0.68	Adc
Total Power Dissipation FR5 Board 1" x 0.75" x 0.062" Derate above 25°C Ambient	PD	550 4.4	mW mW/°(
Operating Temperature	TJ	-55 to +125	°C
Storage Temperature	T _{stq}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS				7	
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 10 μA)	V(BR)DSS	100) -	Vdc
Zero Gate Voltage Drain Current (VGS = 0, VDS = 100 V) $T_J = 25^{\circ}C$ $T_J = 125^{\circ}C$	IDSS	Ξ	=	15 60	nAdc
Gate-Body Leakage Current (VGS = 20 Vdc, VDS = 0)	IGSS		_	50	nAdc

(1) The Power Dissipation of the package may result in a lower continuous drain current.

(2) Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

(continued)

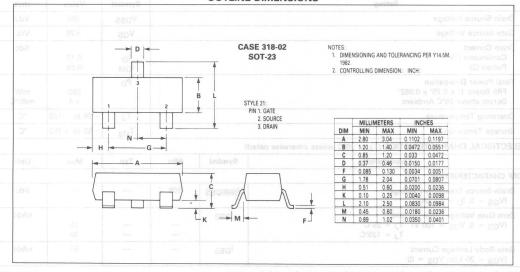
This document contains information on a new product. Specifications and information herein are subject to change without notice.

$\textbf{ELECTRICAL CHARACTERISTICS} \ \ - \ \ \textbf{continued} \ \ (T_A = 25^{\circ}\text{C unless otherwise noted})$

Characteristic		Symbol	Min	Тур	Max	Unit
ON CHARACTERISTICS*						
Gate Threshold Voltag (VDS = VGS, ID = 1		V _{GS(th)}	0.8	ormat	2.8	Vdc
Static Drain-Source Or (V _{GS} = 10 Vdc, I _D =		rDS(on)	_	5	6	Ohms
Forward Transconductance (V _{DS} = 25 V, I _D = 100 mA)		9FS	80	ot Tr	Effe	mmhos
YNAMIC CHARACTERIS	STICS	abo	rent-Mc	neonar	ing for	-Chani
Input Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz)		C _{iss}	_	20	T 97sD	pF
Output Capacitance (Vps = 25 V, Vgs = 0, f = 1 MHz)			gh-voltage.			
Reverse Transfer Capa (VDS = 25 V, VGS =		C _{rss}	utt or 171. 1998 display			
SWITCHING CHARACTE	RISTICS*					vers
Turn-On Delay Time	$(V_{CC} = 30 \text{ V}, I_{C} = 0.28 \text{ A},$	td(on)	_ 0	20	eista <u>n</u> ca —	ns
Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GS} = 50 \Omega$	td(off)	_	40	gonala 4 atto	ns
REVERSE DIODE		•			•	
Diode Forward On-Voltage (I _D = 0.34 A, V _{GS} = 0 V)		V _{SD}	_	_	1.3	V

^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS III Power FETs are designed for low voltage, high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

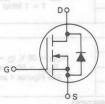
- Silicon Gate for Fast Switching Speeds
- Low rDS(on) 0.04 Ω max and 0.06 Ω max
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- High Peak Current Capabilities 75 and 90 A
- Low Drive Requirement VGS(th) = 4 V max

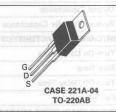


TMOS POWER FETS 25 and 30 AMPERES rDS(on) = 0.04 and 0.06 OHMS 50 VOLTS

BUZ11

BUZ11A





MAXIMUM RATINGS

	Rating			Symbol	BUZ11	BUZ11A	Unit
Drain-Source Voltage			1/2/10	VDSS	of Body Die	50	Vdc
Drain-Gate Voltage (RGS = 20	kΩ)	6	ATTSUB	VDGR		50	Vdc
Gate-Source Voltage		MSI	11208	VGS	tdy Diade	20	uo Vdc
Drain Current — Continuous	-		ATTSUB	ID	30	25	А
— Pulsed		col	(sutsV hotel	IDM	120	100	art brawn
Total Power Dissipation @ T _C = 25°C Derate above 25°C		PD	75 mT visvo		Watts W/°C		
Operating and Storage Temperature Range		T _J , T _{stq}	-55 to 150		°C		

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	R _θ JC R _θ JA	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	yele ≤ 296.	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
FF CHARACTERISTICS		8			
Drain-Source Breakdown Voltage (VGS = 0, ID = 1 mA)	V(BR)DSS	50		1-13	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 50 Volts, V _{GS} = 0) (V _{DS} = 50 Volts, V _{GS} = 0, T _J = 125°C)	A 2010/10 S MIO 10	=	Lu -	250 1000	μAdc
Gate-Body Leakage Current, Forward ($V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$)	IGSSF	_	10	100	nAdc
Gate-Body leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	7 1	10	100	nAdc

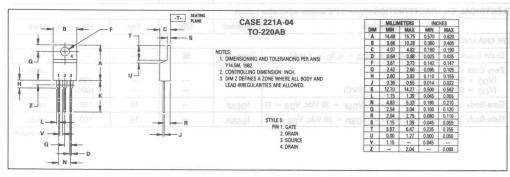
(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characte	ristic		Symbol	Min	Тур	Max	Unit
N CHARACTERISTICS*							
Gate Threshold Voltage (VDS = VGS, ID = 10 mA)	10.	ransist	V _{GS(th)}	2.1	3	1 4	Vdc
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 15 Adc)		BUZ11 BUZ11A	rDS(on)	cemer S –	nadni OMT	0.04 0.06	Ohm
Drain-Source On-Voltage ($V_{GS} = 10 \text{ N}$) ($I_{D} = 15 \text{ Adc}$) ($I_{D} = 15 \text{ Adc}$)	n	BUZ11 BUZ11A	V _{DS(on)}	are d u sign vitel vin g a	0.54 0.83	405-41 Po	Vdc
Forward Transconductance (VDS = 25 V, ID = 15 A)		drivers.	9FS	s, schanol	ethis 8	egu <u>la</u> rons Sate for Fi	mhos
YNAMIC CHARACTERISTICS	and ivin		xam fi	80.0 bns	XEM D M	(ar) = 0.0	SUL MO
Input Capacitance			C _{iss}	noneque.	900	2000	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	_	800	1100	Induct	
Reverse Transfer Capacitance	90 - 1 11127		C _{rss}	es75 s	300	400	ligh Pe
WITCHING CHARACTERISTICS*			Metal A. B.	(MS/SU	3 Million	OHD SOUTH	ALC: NO
Turn-On Delay Time	I HA		td(on)	_	_	45	ns
Rise Time	$(V_{DD} = 30)$		t _r	_	_	110	1
Turn-Off Delay Time	R _{gen} = 8 See Figure		td(off)	_	_	230	
Fall Time			tf	_	_	170	
OURCE DRAIN DIODE CHARACTERIST	ICS*					RATINGS	MUMUN
Diode Forward Voltage (VGS = 0, IS	= 2 Rated Is)	BUZ11 BUZ11A	V _{SD}	Racing	=	2.6 2.4	Vdc
Continuous Source Current, Body Dio	de aagv	BUZ11 BUZ11A	IS	_ ((GS = 20 k	30 25	Adc
Pulsed Source Current, Body Diode	SBV	BUZ11 BUZ11A	ISM	_	- Liouni	120 100	ASour sin Curr
Forward Turn-On Time	(Is = Rat	ed Value)	ton	_	260	elu9	ns
Reverse Recovery Time	VGS	= 0)	t _{rr}	25°C_	200	Diaziguti	tal Powe
ITERNAL PACKAGE INDUCTANCE	(TO-220)					U EN STOC	0.01050
Internal Drain Inductance (Measured from the contact screw of (Measured from the drain lead 0.25)		Control of the contro	Ld	eginer enge	3.5 4.5	TD/A SANS	nH NMAL
Internal Source Inductance	Rala		L _S	inai da nA a	7.5	_	- HOHERTO

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

(Measured from the source lead 0.25" from package to source bond pad)





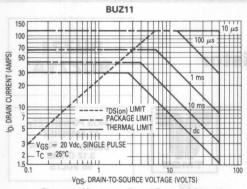


Figure 1. Maximum Rated Forward Biased Safe Operating Area

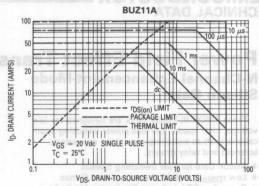


Figure 2. Maximum Rated Forward Biased Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 1 and 2 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T.Imax) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (IDM) may be calculated with the aid of the following equation:

Where

 $I_D(25^{\circ}C)$ = the dc drain current at $T_C = 25^{\circ}C$ from Figure 1 or 2

T_{J(max)} = rated maximum junction temperature TC

= device case temperature

= rated power dissipation at T_C = 25°C $R_{\theta JC}$ = rated steady state thermal resistance

= normalized thermal response from Figure 3

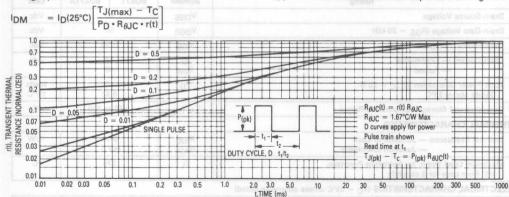


Figure 3. Thermal Response

RESISTIVE SWITCHING

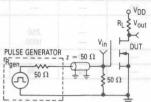


Figure 4. Switching Test Circuit

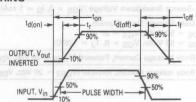


Figure 5. Switching Waveforms

MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Power Field Effect Transistor

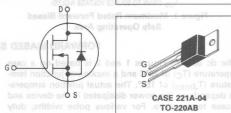
N-Channel Enhancement-Mode Silicon Gate

These TMOS III Power FETs are designed for low voltage, high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ 0.10 Ω max and 0.12 Ω max
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement VGS(th) = 4 V max



TMOS POWER FETS 12 AMPERES rDS(on) = 0.10 and 0.12 OHMS 50 VOLTS





MAXIMUM RATINGS medi etata ybasia beta =

Rating	Symbol	BUZ71 B	BUZ71A	Unit
Drain-Source Voltage	V _{DSS}	(X8050 (3735)		Vdc
Drain-Gate Voltage (RGS = 20 k Ω)	V _{DGR}	50		Vdc
Gate-Source Voltage	V _{GS}	±20		Vdc
Drain Current — Continuous — Pulsed	I _D	12 48		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	40 0.32		Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stq}	-55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction toAmbient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

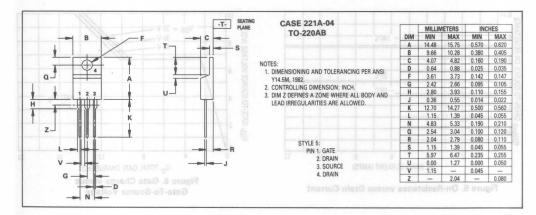
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

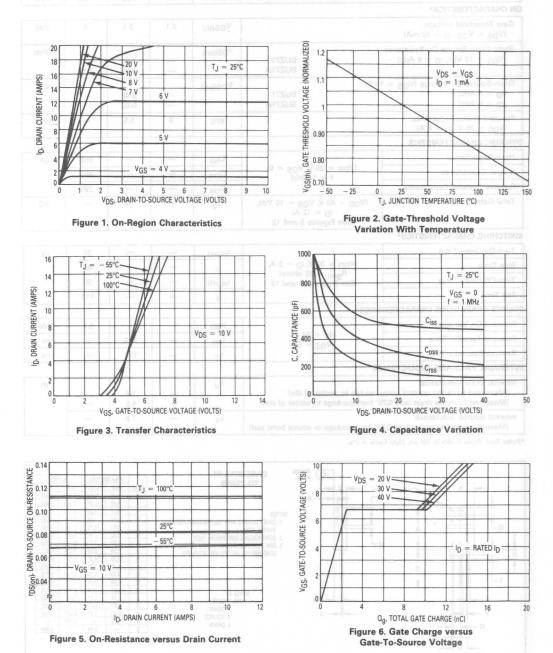
Symbol	IVIII	Тур	IVIAX	Unit
E RUITAIRE	ia.		•	
V(BR)DSS	50	_	_	Vdc
IDSS	RL & Vost	ni ^V =	250 1000	μAdc
IGSSF	-[**]	10-1	100	nAdc
IGSSR	-	10	100	nAdc
	V(BR)DSS IDSS	V(BR)DSS 50 IDSS IGSSF	V(BR)DSS 50 — IDSS — — — — — — — — — — — — — — — — — —	V(BR)DSS 50 — — IDSS — — 250 — 1000 IGSSF — 10 100

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Charact	teristic 201121413	AL CHARACT	Symbol	Min	Тур	Max	Unit
ON CHARACTERISTICS*							
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 10 mA)			V _{GS(th)}	2.1	3.1	4	Vdc
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 6 Adc)		BUZ71 BUZ71A	rDS(on)		0.08 0.10	0.10 0.12	Ohm
Drain-Source On-Voltage (V _{GS} = 1 (I _D = 6 Adc) (I _D = 6 Adc)	0 V)	BUZ71 BUZ71A	V _{DS(on)}	-	0.48 0.60		Vdc
Forward Transconductance (V _{DS} = 25 V, I _D = 6 A)	E		9FS	3	5.5	7//	mhos
DYNAMIC CHARACTERISTICS						1	70 5
Input Capacitance	18.0 2		Ciss	1-1	-	650	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	Y} =	80 V	450		
Reverse Transfer Capacitance	0 10 - 10 - 15 0		C _{rss}	8 -8	3-4	280	
Total Gate Charge REMET MORTONUL agastov blondes of T-assign	$I_D = 12 A$			OURC <u>E v</u> olti a Charact	14	. Tgura 1	nC
SWITCHING CHARACTERISTICS*	235283600						
Turn-On Delay Time	T-1-1-30	01	td(on)		-	30	ns
Rise Time	$(V_{DD} = 30 \text{ V}, R_{gen} = 50)$		t _r	1 + ///	1-38	85	
Turn-Off Delay Time	See Figures 1	1 and 12	td(off)	I + N	生物	90	
Fall Time 220	XA		tf	-	$\mathbb{N} + \mathbb{I}$	110	41
SOURCE DRAIN DIODE CHARACTERI	STICS*	3 6					101
Forward On-Voltage		B	V _{SD}			2.2	Vdc
Forward Turn-On Time	(Is = 24 VGS =		ton		120	-	ns
Reverse Recovery Time	1 33	8	t _{rr}		110		ns
NTERNAL PACKAGE INDUCTAN	CE	21			A		
Internal Drain Inductance (Measured from the contact screv (Measured from the drain lead 0.2			L _d		3.5 4.5		nH
Internal Source Inductance (Measured from the source lead 0.2	MU SQF	MO SUP		mot vocine Characte	7.5	Figure 3	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.





3

RATED SAFE OPERATING AREA INFORMATION

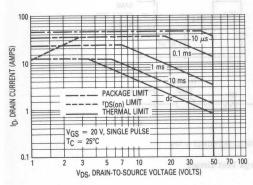


Figure 7. Maximum Rated Forward Biased Safe Operating Area

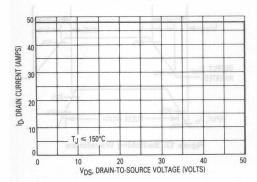


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 7 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_J(max)) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D}(25^{\circ}C) \left[\frac{T_{J}(max) - T_{C}}{P_{D} \cdot R_{\theta J}C \cdot r(t)} \right]$$

where

I_D(25°C) = the dc drain current at T_C = 25°C from Figure 7

 $T_{J(max)}$ = rated maximum junction temperature T_{C} = device case temperature

 P_D = rated power dissipation at $T_C = 25^{\circ}C$

R_θJC = rated steady state thermal resistance

r(t) = normalized thermal response from Figure 9

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

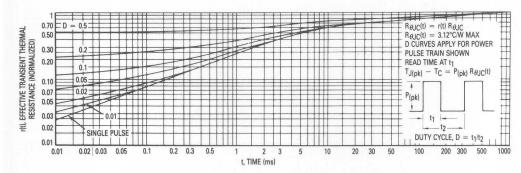


Figure 9. Thermal Response



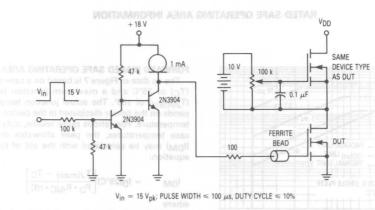


Figure 10. Gate Charge Test Circuit

RESISTIVE SWITCHING and brawned based mumbook X arugid

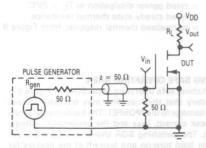


Figure 11. Switching Test Circuit

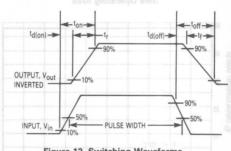
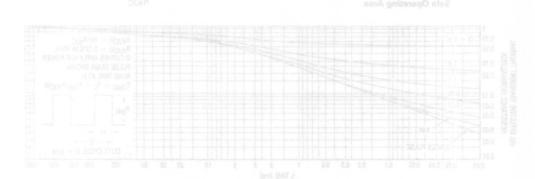


Figure 12. Switching Waveforms



MOTOROLA SEMICONDUCTOR **TECHNICAL DATA**

Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate

This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, motor controls, solenoid and relay

- Silicon Gate for Fast Switching Speeds
- Low rDS(on) 0.4 Ω max
 Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement VGS(th) = 4 V max



TMOS POWER FET 7 AMPERES rDS(on) = 0.4 OHMS 200 VOLTS





MAXIMUM RATINGS

Rating not	Symbol	Value Thomas	Unit
Drain-Source Voltage	V _{DSS}	200	Vdc
Drain-Gate Voltage (RGS $=$ 20 k Ω)	VDGR	200	Vdc
Gate-Source Voltage	VGS	± 20	Vdc
Drain Current — Continuous (T _C = 25°C) — Pulsed	I _D	7 28	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	40 0.32	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	R_{θ} JC R_{θ} JA	3.12 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS				ARR	
Drain-Source Breakdown Voltage (VGS = 0, I _D = 1 mA)	V _{(BR)DSS}	200	1-		Vdc
Zero Gate Voltage Drain Current (Vps = 200 Volts, Vgs = 0) (Vps = 200 Volts, Vgs = 0, Tj = 125°C)	IDSS	=	=	250 1000	μAdd
Gate-Body Leakage Current, Forward ($V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$)	IGSSF	_	10	100	nAdo
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	_	10	100	nAdd

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

- n - I				
E				
S(th)	2.1	3	4	Vdc
S(on)	HO MET O	adiad	0.4	Ohm
S(on)		3.2	elas	Vdc
9FS	2.2	3.5	U	mhos
1	S(on)	S(on) —	S(on) — 3.2	S(on) — 3.2 —

Input Capacitance	Valer	Ciss	rro <u>le,</u> si	100_10/0	600	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	_		160	
verse Transfer Capacitance		C _{rss}	paade B	SWITCHING	80	
Total Gate Charge	(V _{DS} = 160 V, V _{GS} = 10 Vdc, I _D = 7 A)	Q_g	no it egia	15	P :HAD	nC

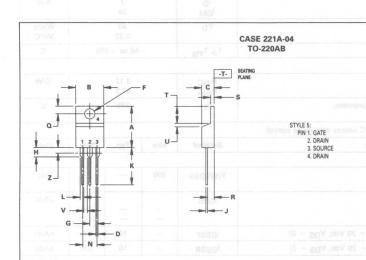
SWITCHING CHARACTERISTICS*

Turn-On Delay Time	HA	td(on)	= District	V Inte	20	ns
Rise Time	$(V_{DD} = 30 \text{ V}, I_{D} = 3 \text{ A}, V_{GS} = 10 \text{ V},$	t _r		_	60	
Turn-Off Delay Time	R _{gen} = 50 ohms)	td(off)	_	_	90	
Fall Time		tf	_	_	55	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage		V _{SD}	_	_	1.7	Vdc	0
Forward Turn-On Time	$(I_S = 14 \text{ A}, V_{GS} = 0)$	ton	Ration	120	_	ns	
Reverse Recovery Time	and de	t _{rr}	-	325	ej_stlo\	ns	6

*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.



- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: INCH.

 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

-3	MILLIN	MILLIMETERS		HES
DIM	MIN	MAX	MIN	MAX
Α	14.48	15.75	0.570	0.620
В	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
Н	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
٧	1.15	-	0.045	-
Z	VOH J	2.04	-D5A	0.080

TYPICAL ELECTRICAL CHARACTERISTICS

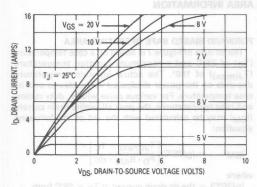


Figure 1. On-Region Characteristics

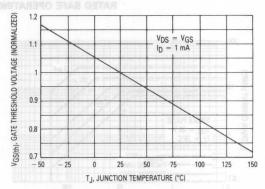


Figure 2. Gate-Threshold Voltage Variation With Temperature

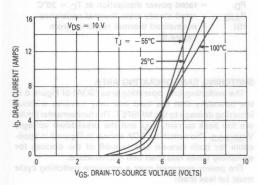


Figure 3. Transfer Characteristics

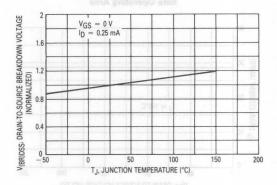


Figure 4. Breakdown Voltage Variation With Temperature

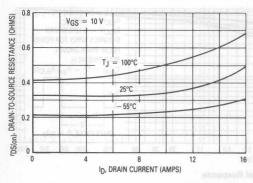


Figure 5. On-Resistance versus Drain Current

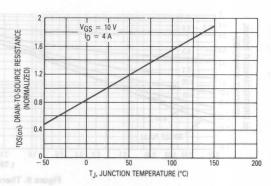


Figure 6. On-Resistance Variation With Temperature

RATED SAFE OPERATING AREA INFORMATION

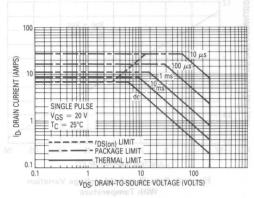


Figure 7. Maximum Rated Forward Biased Safe Operating Area

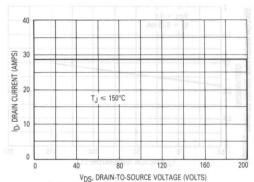


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 7 is based on a case temperature (T_C) of 25°C and a maximum junction temperature ($T_J(max)$) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D}(25^{\circ}C) \left[\frac{T_{J(max)} - T_{C}}{P_{D} \cdot R_{\theta JC} \cdot r(t)} \right]$$

where

 $I_D(25^{\circ}C) = \text{the dc drain current at T}_C = 25^{\circ}C \text{ from Figure 7}$

T_{J(max)} = rated maximum junction temperature

T_C = device case temperature

 P_D = rated power dissipation at $T_C = 25^{\circ}C$ $R_{\theta JC}$ = rated steady state thermal resistance r(t) = normalized thermal response from

Figure 9

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{\mathsf{TJ}(\mathsf{max}) - \mathsf{TC}}{\mathsf{R}_{\theta}\mathsf{JC}}$$

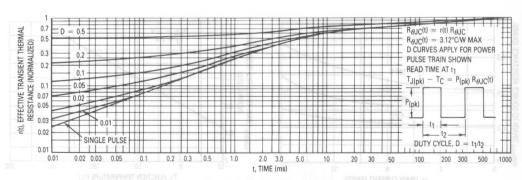


Figure 9. Thermal Response

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

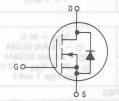
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, motor controls, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement VGS(th) = 4 V max





7-8



BUZ84

BUZ84A

TMOS POWER MOSFETs

5.3 and 6 AMPERES

rDS(on) = 1.5 and 2 OHMS

800 VOLTS

MAXIMUM RATINGS

B. Rating — —	Symbol	BUZ84	BUZ84A	Unit
Drain-Source Voltage	VDSS	008 BU284		Vdc
Drain-Gate Voltage (R _{GS} = 20 kΩ)	VDGR	800		Vdc
Gate-Source Voltage	VGS	#83U8 ±20		Vdc
Drain Current Continuous $T_C = 25^{\circ}C$ $T_C = 100^{\circ}C$	ID ID	5.3 3.3 A 8	6 3.8	Adc
Pulsed 0001 —	IDM	21 (0	80 V 24	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	125 1		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	R _O JC R _O JA	1 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
FF CHARACTERISTICS	™ (no)b [†]			Yout	S pa
Drain-Source Breakdown Voltage (VGS = 0, ID = 1 mA)	V _{BR} (DSS)	800	_	->-\	Vdc
Zero Gate Voltage Drain Current (V _{DSS} = 800 V, V _{GS} = 0) T _J = 125°C	IDSS	Ξ	=	0.25	mAdo
Gate-Body Leakage Current, Forward (VGSF = 20 V)	IGSSF	, - 1	-	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 V)	IGSSR	-	-	100	nAdc

VGS(th)

(I_D = 10 mA, V_{DS} = V_{GS}) See the MTM5N90 Designer's Data Sheet for a complete set of design curves for this device.

Design curves of the MTM6N85 are applicable for this device.

Gate Threshold Voltage

(continued)

Vdc

CASE 1-06 TO-204AA

2.1

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteris	Symbol	Min	Тур	Max	Unit	
N CHARACTERISTICS — continued	undalan.	over"I" drawn	.442	blo	THE RES	Ch 7, 84, 8 40
Static Drain Source On-Resistance ⁽¹⁾ (VGS = 10 Vdc, I _D = 3 Adc)	BUZ84 BUZ84A	rDS(on)	101110:	ine-do	2 1.5	Ohms
Forward Transconductance ⁽¹⁾ (V _{DS} = 25	5 Vdc, ID = 3 A)	9FS	1.8	OHT	61 5 0	mhos
APACITANCE						
Input Capacitance	$(V_{DS} = 25 V,$	Ciss	de <u>sig</u> ner	2000	5000	pF
Output Capacitance	$V_{GS} = 0$	Coss	unverters	200	350	is, riigi
Reverse Transfer Capacitance	f = 1 MHz)	C _{rss}	-6191	80	140	ils, solo
WITCHING CHARACTERISTICS			ig Speed	t Switchin	88 107 8	on Gat
Turn-On Delay Time	(VDS = 30 V,	td(on)	a position	50	90	ns
Rise Time	I _D = 2.5 Adc BUZ84	t _r	_	100	140	ductive
Turn-Off Delay Time	$I_D = 2.6 \text{ Adc BUZ84A}$ $Z_O = 50 \Omega, V_{GS} = 10 \text{ V}$	td(off)	F (##) 88	320	430	Drive
Fall Time	See Figs. 1 and 2	tf	_	100	140	
OURCE-DRAIN DIODE CHARACTERISTICS	S & O					-
Diode Forward Voltage ($V_{GS} = 0$) ($I_{S} = (I_{S} = 0)$)	V _{SD}	T =	-gnii	1.45 1.5	Vdc	
Continuous Source Current, Body Diode	BUZ84 BUZ84A	agy Is	= ,,	20.80	5.3	Adc
Pulsed Source Current, Body Diode	BUZ84 BUZ84A	ISM	=	_	21 24	A
Forward Turn-On Time	(I _S = 5.3 A,	ton	Lin	nited by st	ray induct	ance
Reverse Recovery Time	$V_{GS} = 0$	Mol trr	T -	1200	Podend	ns
NTERNAL PACKAGE INDUCTANCE	125 V	99	25°C	= 3T @ r	roit, gizarC	Power
Internal Drain Inductance (Measured from the contact screw on source pin and the center of the die.)	R T LT	ire Range	5 Heregme T	d Stolege	nH	
Internal Source Inductance (Measured from the source pin 0.25" for source bond pad.)	LSA LS	586	12.5	ut sonste Inei/Imag	nal Ras	

(1) Pulse Test = Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

RESISTIVE SWITCHING

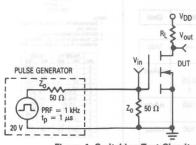


Figure 1. Switching Test Circuit

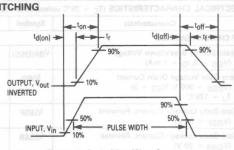


Figure 2. Switching Waveforms

TMOS POWER FET

14 AMPERES

rDS(on) = 0.18 OHM

100 VOLTS

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate TMOS

This TMOS Power FET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low r_{DS(on)} to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





GO

MAXIMUM RATINGS

081 R	ating		Symbol	Value	Unit
Drain-Source Voltage		V _{DSS}	100	Vdc	
Drain-Gate Voltage (RGS = 20 kΩ)		(don)	VDGR	100	
Gate-Source Voltage		(Ne)al	VGS	± 20	Vdc
Drain Current Continuous, T _C = 25°C		10	ID	14	Adc
$T_C = 100^{\circ}C$ Peak, $T_C = 25^{\circ}C$			Rated Vossi	9 8.0 56	-
Total Power Dissipation @ Total Power Dissipation @ Total Power 25°C	T _C = 25°C	bgØ	PD	75 0.6	Watts W/°C
Operating and Storage Tem	perature Ran	ge	T _J , T _{stg}	-55 to 150	°C

THERMAL CHARACTERISTICS

TETWAL STATE OF THE TIES				
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 30	°C/W	
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 Seconds	TL	300	°C	

See the MTM12N08 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTM12N10 are applicable for this series of product.

STYLE 3: PIN 1. GATE 2. SOURCE CASE DRAIN

NOTES:

1. DUAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:

| ★ | Φ 0.25 (0.010) ● | W | V ● |

3. POSITIONAL TOLERANCE FOR LEADS:

| ★ | Φ 0.30 (0.012) ● | W | V ● | Q ●

	MILLIA	AETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A		39.37	-	1.550
В	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15	30.15 BSC		BSC
G	10.93	10.92 BSC		BSC
H	5.46 BSC		0.215	BSC
J	16.89	16.89 BSC		BSC
K	11.18	12.19	0.440	0.480
0	3.81	4.19	0.151	0.165
R	-	26.67		1.050
U	2.54	3.05	0.100	0.120
٧	3.81	4.19	0.151	0.165

ELECTRICAL CHARACTERISTICS (T _C = 25°C unless otherwise noted)	UDUCTOR MARKAGE	

Characteristic			Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA)			V _{(BR)DSS}	100	lall	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0$) ($V_{DS} = 0.8\ Rated\ V_{DSS},\ V_{GS} = 0$,	T _J = 125°C)		IDSS	emeons 201	0.2	mAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)			IGSSF	- henniseh	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	n der		GSSF	switc h ing ap	sw 100 sec	nAdc
ON CHARACTERISTICS*					.8.	elay driver
Gate Threshold Voltage (VDS = VGS, ID = 0.25 mA)			V _{GS(th)}	esseoJ-nO	for 1 & t Sw to Minimiz	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 8 Adc)	. 00		rDS(on)	P Dissipation	0.18	Ohm
On-State Drain Current (V _{GS} = 10 V) (V _{DS} \ge 2.5 Vdc)			I _{D(on)}	14	Dads T	Adc
Forward Transconductance (V _{DS} ≥ 2.5 V, I _D = 8 A)				4	_	mhos
YNAMIC CHARACTERISTICS		9				
Input Capacitance			Ciss	_	800	pF
Output Capacitance		$V_{DS} = 25 \text{ V, } V_{GS} = 0,$ f = 1 MHz)	Coss	_	500	OMUM RI
Reverse Transfer Capacitance		Symbol	C _{rss}	-uniteP	150	
WITCHING CHARACTERISTICS*	V 007	SSGA			Voltage	ain-Source
Turn-On Delay Time	100	ласу	td(on)	T - I	30	V m ns
Rise Time	(V _{DD} ≈ 36 V	, I _D = 8 Apk,	t _r	_	75	(RGS = 20
Turn-Off Delay Time	R _{gen} =	15 Ohms)	td(off)		40	source started
Fall Time		Ci.	tf	_	45	ain Current
Total Gate Charge	8		Ωg	17 (Typ)	30	nC
Gate-Source Charge		Rated V _{DSS} , I _D = Rated I _D)	Qgs	8 (Typ)		Peak, Tc =
Gate-Drain Charge	W 403 Storas	ib diates by	Q_{gd}	9 (Typ)	hiss pand (ital Power I
OURCE DRAIN DIODE CHARACTERIST	ICS*	T .T	20	and an extreme	. T 70 I	
Forward On-Voltage	(I _S = F	Rated ID	V _{SD}	1.4 (Typ)	2.3(1)	Vdc
Forward Turn-On Time	V _{GS} = 0)		ton	Limited by st	ray inductan	се
Reverse Recovery Time		Baje Raja	t _{rr} and	325 (Typ)	ut -	ns
NTERNAL PACKAGE INDUCTANCE	300	JT.	poses,	Soldering Pur	ad Temp. for	al mumbia
Internal Drain Inductance (Measured closer to the source pin and the center		crew on the header	L _d	5 (Typ)	ise fo <u>r 5</u> Sec	nH®1
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)			L _S	12.5 (Typ)	BDesignate's land	the IHn 112NI on ourves of t

3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Power Field Effect Transistor N-Channel Enhancement-Mode

N-Channel Enhancement-Mode Silicon Gate TMOS

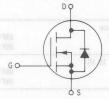
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low rDS(on) to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



IRF140 IRF141 IRF142

TMOS POWER FETS 24 and 27 AMPERES rDS(on) = 0.085 OHM 60 and 100 VOLTS rDS(on) = 0.11 OHMS 100 VOLTS





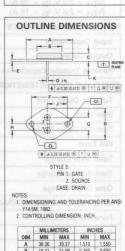
MAXIMUM RATINGS

Datin-		Comphal		IRF	RF Unit	
Rating		Symbol	140	141	142	Unit
Drain-Source Voltage	Comm	VDSS	100	60	100	Vdc
Drain-Gate Voltage (RGS = 20 kΩ)	Cres	VDGR	100	60	100	Vdc
Gate-Source Voltage		VGS		± 20		Vdc
Drain Current Continuous, T _C = 25°C T _C = 100°C Peak, T _C = 25°C	4 (tio)b ³	MD) 31	1.7 Oh	7 7 08	24 15 96	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	gO.	PD	Daniel	125 1		Watts W/°C
Operating and Storage Temperature Range	ge 200	TJ, Tstg	= 05	55 to 1	50	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	R ₀ JC	1	°C/W
— Junction to Ambient	$R_{\theta}JA$	30	
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL (0	300	°C

See the MTM25N10 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.



100	MILLIN	MILLIMETERS		HES	
DIM	MIN	MAX	MIN	MAX	
A	38.36	39.37	1.510	1.550	
В	19.31	21.08	0.760	0.830	
C	6.35	8.25	0.250	0.325	
D	1.45	1.60	0.057	0.063	
E	1.53	1.77	0.060	0.070	
F	30.15	30.15 BSC		1.187 BSC	
G	10.92	10.92 BSC		0.430 BSC	
Н	5.46	5.46 BSC		BSC	
J	16.89	BSC	0.665	BSC	
K	11.18	12.19	0.440	0.480	
Q	3.84	4.19	0.151	0.165	
R	25.15	26.67	0.990	1.050	
U	3.84	4.19	0.151	0.165	

ELECTRICAL CHARACTERISTICS (To = 25°C unless otherwise noted)

CALL ALL C	naracterist	ic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS		na era disensi sen era era era	T box	.33211	Lials	10.00.00.00
Drain-Source Breakdown Voltag	е	THE RESERVE THE	V(BR)DSS	OF STREET ST	PIOI I	Vdc
$(V_{GS} = 0, I_D = 0.25 \text{ mA})$		IRF140, IRF142 IRF141	st-Mode	100	sol n il i	hanne
Zero Gate Voltage Drain Currer (VDS = Rated VDSS, VGS =			IDSS		0.2	mAdc
(VDS = 0.8 Rated VDSS, VGS		= 125°C)		are designin	eTER PETS	se TMOS
Gate-Body Leakage Current, Fo (VGSF = 20 Vdc, VDS = 0)	ward		IGSSF	switching all s, converters	100	nAdc
Gate-Body Leakage Current, Re (VGSR = 20 Vdc, VDS = 0)	/erse		IGSSR	ching Speak	100	nAdc
N CHARACTERISTICS*	80	MY .	10-08/10/00	1.302801-00	STURSTAND	eT bessys
Gate Threshold Voltage (Vps = Vgs, Ip = 0.25 mA)	5	96	VGS(th)	Dissigation aracterized	A L Nower in Diode Ch	Vdc
Static Drain-Source On-Resistar (VGS = 10 Vdc, I _D = 15 Add		IRF140, IRF141 IRF142	rDS(on)	=	0.085 0.11	Ohm
On-State Drain Current (VGS = $(V_{DS} \ge 2.3 \text{ Vdc})$ (VDS $\ge 2.6 \text{ Vdc})$	10 V)	IRF140, IRF141 IRF142	I _{D(on)}	27 24	_	Adc
Forward Transconductance (VDS \geq 2.3 V, ID = 15 A) (VDS \geq 2.6 V, ID = 15 A)	8.0	IRF140, IRF141 IRF142	9FS	6.0 6.0	20/01	mhos
YNAMIC CHARACTERISTICS	shall	301		renit	o d	
Input Capacitance		149 141 142	Ciss	_	1600	pF
Output Capacitance	abV	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	_	800	echue 8-ni
Reverse Transfer Capacitance	beV	VDGR 100 80 100	C _{rss}	_	300	in-Gate Vo
WITCHING CHARACTERISTICS*					193	1 03 - SDI
Turn-On Delay Time	009	03.1 SOV	td(on)		30	ns
Rise Time	540A	$(V_{DD} \approx 30 \text{ V, I}_{D} = 15 \text{ Apk,}$	t _r	_	60	in Current
Turn-Off Delay Time		R _{gen} = 4.7 Ohms)	t _d (off)	_	080	
Fall Time		ag 50°	tf		30	= 37 ,kss
Total Gate Charge	O'EVV	- PU 125	Qq	40 (Typ)	60	nC
Gate-Source Charge	D" \	(V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 10 Vdc, I _D = Rated I _D)	Qgs	17 (Typ)	Stocker Ten	has online
Gate-Drain Charge	,	GS = 10 vac, ID = nated ID/	Q _{qd}	23 (Typ)	resent to A G	AND LABOR
OURCE DRAIN DIODE CHARACT	ERISTICS*	1 1 1		rion to Page	ward accept	reisoff lower
Forward On-Voltage		(IS = Rated ID,	V _{SD}	1.5 (Typ)	2.3(1)	Vdc
Forward Turn-On Time	1)-	V _{GS} = 0)	ton	Limited by s	tray inductar	ice mumb
Reverse Recovery Time			t _{rr}	450 (Typ)	Se for 3 Seco	ns
ITERNAL PACKAGE INDUCTAN	E Jasife eta	dasign curvis for the product on this di	lo res strigmo	as Sheat for a c	G a'vengirer I (e MTM25N1
Internal Drain Inductance (Meas closer to the source pin and the		the contact screw on the header the die)	L _d	5 (Typ)	_	nH
Internal Source Inductance (Me package to the source bond package)		m the source pin, 0.25" from the	L _S	12.5 (Typ)	_	nH

^{*}Pulse Test: Pulse Width \leqslant 300 μs , Duty Cycle \leqslant 2%. (1) Add 0.2 V for IRF140 and IRF141.

MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

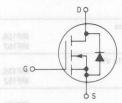
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IRF150 IRF151 IRF152

TMOS POWER FETS 33 and 40 AMPERES rDS(on) = 0.055 OHM 60 and 100 VOLTS rDS(on) = 0.08 OHMS 100 VOLTS





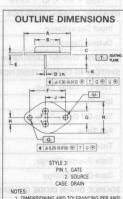
MAXIMUM RATINGS

D. C	IRF		Unit				
agos Rati	ng		Symbol	150	151	152	Unit
Drain-Source Voltage		8200	VDSS	100	60	100	Vdc
Drain-Gate Voltage (RGS = 20 kΩ)		5817	VDGR	100	60	100	Vdc
Gate-Source Voltage	-	(no)to ³	VGS		± 20		Vdc
Drain Current Continuous, $T_C = 25^{\circ}C$ $T_C = 100^{\circ}C$ Peak, $T_C = 25^{\circ}C$		ing the state of t	20 Apk. ID(am)	2	0 5 60	33 20 132	Adc
Total Power Dissipation @ Total Power Dissip	c = 25°C	_b O	PD	sets8	150 1.2	eaV)	Watts W/°C
Operating and Storage Temp	erature Ran	ige	T _J , T _{stg}	G(7)	55 to 1	50	°C

THERMAL CHARACTERISTICS

HENIVIAL CHANACTERISTICS			
Thermal Resistance — Junction to Case — Junction to Ambient	R _θ JC R _θ JA	0.83	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	300	°C

See the MTM55N08 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTM55N10 are applicable for this series of product.



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

2. CONTROLLING DIMENSION: INCH.

	MILLIN	MILLIMETERS		HES	
DIM	MIN	MAX	MIN	MAX	
A	38.36	39.37	1.510	1.550	
В	19.31	21.08	0.760	0.830	
C	6.35	8.25	0.250	0.325	
D	1.45	1.60	0.057	0.063	
E	1.53	1.77	0.060	0.070	
F	30.15 BSC		1.187 BSC		
G	10.92	10.92 BSC		0.430 BSC	
Н	5.46	5.46 BSC		0.215 BSC	
J	16.89	BSC	0.665	BSC	
K	11.18	12.19	0.440	0.480	
Q	3.84	4.19	0.151	0.165	
R	25.15	26.67	0.990	1.050	
U	3.84	4.19	0.151	0.165	

ELECTRICAL	CHARACTERISTICS	/To -	25°C unloss othe	(hoted poted)
FLECT BICAL	CHARACTERISTICS	IIC =	25°C unless othe	erwise noted)

Characteristic			Symbol	Min	Max	Unit	
OFF CHARACTERISTICS			. 6	etys .	22.00	g . n = q	
Drain-Source Breakdown Voltage			50, IRF152	V(BR)DSS	100	3463171	Vdc
$(V_{GS} = 0, I_{D} = 0.25 \text{ mA})$ IRF150, IRF IRF151			nt-Mody	60	el Epha	Channe	
Zero Gate Voltage Drain Current				IDSS	80	MII ets	mAdc
$(V_{DS} = Rated V_{DSS}, V_{GS} = 0)$ $(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0)$	0, TJ	= 125°C)		ed for high	are designa	0.2 Powel FETs	ese TMOS
Gate-Body Leakage Current, Forwa (VGSF = 20 Vdc, VDS = 0)	rd			IGSSF IGG	switc <u>hi</u> ng at s, converter	new100 Lee totalupay ge	nAdc
Gate-Body Leakage Current, Revers (VGSR = 20 Vdc, VDS = 0)	se			IGSSR	ching Spee	DO Fast Swift	nAdc
ON CHARACTERISTICS*	80	DIVIT		Specified at	On-Losses.	o vimunize	W [DS(on)
Gate Threshold Voltage (Vps = Vgs, Ip = 0.25 mA)		90		V _{GS(th)}	Dissipation	A Is Power	Vdc op
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 20 Adc)	F	IRF1 IRF1	50, IRF151 52	rDS(on)	_	0.055 0.080	Ohm
On-State Drain Current (V _{GS} = 10 (V _{DS} \ge 2.2 Vdc) (V _{DS} \ge 2.6 Vdc)	V)	IRF1 IRF1	50, IRF151 52	lD(on)	40 33	_	Adc
Forward Transconductance ($V_{DS} \ge 2.2 \text{ V, } I_D = 20 \text{ A}$) (RF150, IRF151 ($V_{DS} \ge 2.6 \text{ V, } I_D = 20 \text{ A}$) (RF152			9FS	9	= Enviro	mhos	
YNAMIC CHARACTERISTICS		301					
Input Capacitance	Ugit	581 182 081	Symbol	Ciss	_ gnits	3000	pF
Output Capacitance	-BN	$(V_{DS} = 25 \text{ V}, V_{C})$ f = 1 MHz		Coss	_	1500	brain-Source
Reverse Transfer Capacitance	ndstv	100 80 100	anal	C _{rss}	_	500	Yrain-Gate Vo
SWITCHING CHARACTERISTICS*			F11253				(Ags = 20
Turn-On Delay Time	all V			td(on)	_	35	801 ns -0168
Rise Time	Aide	$(V_{DD} \approx 24 \text{ V, I}_{D} =$		t _r	_	100	train Current
Turn-Off Delay Time		R _{gen} = 4.7 O	hms)	td(off)	_	125	Continuous
Fall Time		160 132		tf	_	100	Peak, To a
Total Gate Charge	enne VV	190	09	Q_g	60 (Typ)	120	TevnC late
Gate-Source Charge	WILC	$V_{DS} = 0.8 \text{ Rated}$ $V_{GS} = 10 \text{ Vdc, ID} = 0.8 \text{ Rated}$		Qgs	25 (Typ)	7,57 9	Derate abov
Gate-Drain Charge	100	03 031 01 96 10	gta T.T.	Qgd	35 (Typ)	ael agenete l	perating and
SOURCE DRAIN DIODE CHARACTER	ISTIC	S*			SOL	SIRS LOANA	HIJ JAMRE
Forward On-Voltage	W.O.	(Ic = Rated	Dung	V _{SD}	1.5 (Typ)	2.3(1)	Vdc
Forward Turn-On Time	100	$V_{GS} = \text{Rated ID},$ $V_{GS} = 0)$		ton	Limited by s	tray inductan	ce
Reverse Recovery Time				t _{rr}	450 (Typ)	se fo r 5 Sect	o mns %
NTERNAL PACKAGE INDUCTANCE	marks -	July stalls ma residence water	an annual for	h No con analysis	s sol mari en	O absorbant o	et e MTMISNO
Internal Drain Inductance (Measure closer to the source pin and the ce			on the header	to suit doint to	5 (Typ)	OFFISHING ST	t to anHus of t
Internal Source Inductance (Measu package to the source bond pad)	red fr	om the source pin, 0	.25" from the	L _S	12.5 (Typ)	i -	nH

*Pulse Test: Pulse Width \leqslant 300 $\mu \rm{s}$, Duty Cycle \leqslant 2%. (1) Add 0.2 V for IRF150 and IRF151.

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

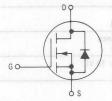
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IRF230

TMOS POWER FET 9 AMPERES rDS(on) = 0.4 OHM 200 VOLTS





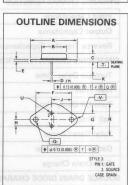
MAXIMUM RATINGS

	Rating		Symbol	Value	Unit	
Drain-Source Voltage	-	- v		200	Vdc	
Drain-Gate Voltage (R _{GS} = 20 kΩ)			V _{DGR} 200	VDGR 200	200	Vdc
Gate-Source Voltage		Indial	VGS	±20	Vdc	
Drain Current Continuous, T _C = 25°C T _C = 200		gt Obaind	ID = F Ack	9	Adc	
Peak, T _C = 25°C				36		
Total Power Dissipation Derate above 25°C	@ T _C = 25°C	20	PD letted Vosse	75 8.0 0.6	Watts W/°C	
Operating and Storage T	emperature Rar	ige	TJ, T _{stg}	-55 to 150	°C	

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes,	T ₁ 10 =	300	°C
1/8" from Case for 5 Seconds			

See the MTM8N20 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI-Y14.5M, 1982.

2. CONTROLLING DIMENSION: INCH.

3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO ZOAAA OUTLINE SHALL APPLY.

	MILLIN	METERS	INC	INCHES			
DIM	MIN	MAX	MIN	MAX			
A	11,630	39.37	185	1.550			
В	-	21.08	-	0.830			
C	6.35	8.25	0.250	0.325			
D	0.97	1.09	0.038	0.043			
E	1.40	1.77	0.055	0.070			
F	30.15	BSC	1.187 BSC				
G	10.92	BSC	0.430 BSC				
н	5.48	BSC	0.215 BSC				
J	16.89	16.89 BSC		BSC			
K	11.18	12.19	0.440	0.480			
Q	3.84	4.19	0.151	0.165			
R	-	26.67		1.050			
U	4.83	5.33	0.190	0.210			
٧	3.84	4.19	0.151	0.165			

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Min	Max	Unit
FF CHARACTERISTICS		NOT A COMM	31.51.795 A.	L. In	
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	TOTERN	V(BR)DSS	200	edeli I	Vdc
Zero Gate Voltage Drain Current (Vps = Rated Vpss, Vgs = 0) (Vps = 0.8 Rated Vpss, Vgs = 0,	T _J = 125°C)	IDSS	- 50	0.2	mAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		IGSSF	cesigned for	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	NEED TOWN	IGSSR		100	nAdc
N CHARACTERISTICS*		in halfinan/2	noming appear of On-Lossas	wiminiM o	Lantonia
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 0.25 mA)	+	VGS(th)	2 Dissipation	m se k iture A se Powe	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, I _D = 5 Adc)		rDS(on)	harac <u>ta</u> nzed	0.4	Ohm
On-State Drain Current ($V_{GS} = 10 \text{ V}$) ($V_{DS} \ge 3.6 \text{ Vdc}$)		I _{D(on)}	9	_	Adc
Forward Transconductance (V _{DS} ≥ 3.6 V, I _D = 5 A)	20	9FS	3	_	mhos
YNAMIC CHARACTERISTICS				TINGS	AR MUM
Input Capacitance	Symbol Value U	C _{iss}	Point	800	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss		450	n-Source
Reverse Transfer Capacitance	Vrpess 200 V	C _{rss}	-	150	n-Gata Vo
WITCHING CHARACTERISTICS*				(13)	GS = 20 I
Turn-On Delay Time	V65 ±20 . V	td(on)	_	30	ns
Rise Time	$(V_{DD} \approx 90 \text{ V}, I_D = 5 \text{ Apk},$	t _r	_	50	Indiana d
Turn-Off Delay Time	R _{gen} = 15 Ohms)	td(off)	_	50	edoundin
Fall Time	36	tf	_	40	aft. TC =
Total Gate Charge	PD 75 W	Q_g	15 (Typ)	30	nC
Gate-Source Charge	(V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 10 Vdc, I _D = Rated I _D)	Qgs	8 (Typ)	-	TOOL DIETO
Gate-Drain Charge	ds greats bottom	Q_{gd}	7 (Typ)	normalization A.	SAME SAME
OURCE DRAIN DIODE CHARACTERIST	TCS*			SANG FORCE	displanting
Forward On-Voltage	(Is = Rated Ip,	V _{SD}	1.7 (Typ)	2.0	Vdc
Forward Turn-On Time	$V_{GS} = 0$	ton	Limited by st	tray inductar	nce
Reverse Recovery Time		t _{rr}	325 (Typ)	or tout Sag	ns
NTERNAL PACKAGE INDUCTANCE (TO	-204) a side no pulbong e/tradi sevauo oplasi	b. hó tea steigre	ta Sheet for a co	Cusigner's Da	мтивизо
Internal Drain Inductance (Measured closer to the source pin and the center		Ld	5 (Typ)	_	nH
Internal Source Inductance (Measured package to the source bond pad)	from the source pin, 0.25" from the	L _S	12.5 (Typ)	_	nH

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

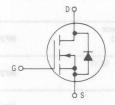
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- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



IRF240 IRF241 IRF243

TMOS POWER FETS 16 and 18 AMPERES rDS(on) = 0.18 OHM 150 and 200 VOLTS rDS(on) = 0.22 OHMS 150 VOLTS



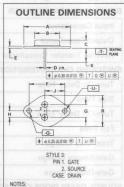


MAXIMUM RATINGS

Paties.		0	IRF			11-24
Rating		Symbol	240	241	243	Unit
Drain-Source Voltage	Coss	VDSS	200	150	150	Vdc
Drain-Gate Voltage $(R_{GS} = 20 \text{ k}\Omega)$	Cras	VDGR	200	150	150	Vdc
Gate-Source Voltage	(main)	VGS	±20		Vdc	
Drain Current Continuous, T _C = 25°C T _C = 200°C Peak, T _C = 25°C	nt (na)b [†]	1 _D	1	8 1 2	16 10 64	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	90	PD	betsil	125	2017)	Watts W/°C
Operating and Storage Temperature Ran	nge	TJ, Tstg	= 01	55 to 1	50	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	300	°C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

2. CONTROLLING DIMENSION: INCH.

- 0	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	38.36	39.37	1.510	1.550
В	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15	30.15 BSC		BSC
G	10.92	BSC	0.430	BSC
Н	5.48	BSC	0.215	BSC
J	16.89	BSC	0.665	BSC
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
FF CHARACTERISTICS	market a mark	The state of	3371	ala:O	20,476.0.26.00
Drain-Source Breakdown Voltage $(V_{GS} = 0, I_D = 0.25 \text{ mA})$	IRF240 IRF241, IRF243	V _{(BR)DSS}	200 150	al Enha	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0$) ($V_{DS} = 0.8\ Rated\ V_{DSS},\ V_{GS} = 0$)	, T _J = 125°C)	IDSS Wol not b	are designe	0.2 T = 1	mAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		IGSSF	s, converter	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)		IGSSR	ching Spea	100	nAdc
ON CHARACTERISTICS*	BOMT	19 paintade	, seeson Hio	enulination of	evated Fe
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 0.25 mA)	90	V _{GS(th)}	Dissignation bearesets	A Power in Usade Ch	Vdc
Static Drain-Source On-Resistance $(V_{GS} = 10 \text{ Vdc}, I_D = 10 \text{ Adc})$	IRF240, IRF241 IRF243	rDS(on)	_	0.18 0.22	Ohm
On-State Drain Current ($V_{GS} = 10 \text{ V}$ ($V_{DS} \ge 3.2 \text{ Vdc}$) ($V_{DS} \ge 3.5 \text{ Vdc}$)	(1) IRF240, IRF241 IRF243	I _{D(on)}	18 16	_	Adc
Forward Transconductance (V _{DS} \geqslant 3.2 V, I _D = 10 A) IRF240, IRF241 (V _{DS} \geqslant 3.5 V, I _D = 10 A) IRF243		9FS	6		mhos
YNAMIC CHARACTERISTICS	451				
Input Capacitance	Symuol 240 241 243	Ciss	Sem	1600	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	_	750	in-Source \
Reverse Transfer Capacitance	VBGR 200 150 150 Vd	C _{rss}	-	300	ioV etsD-ni
WITCHING CHARACTERISTICS*				10	GS = 20 k
Turn-On Delay Time	99V = 20 Vd	td(on)		30	ns
Rise Time	$(V_{DD} \approx 75 \text{ V, I}_{D} = 10 \text{ Apk,}$	t _r	_	60	n Current
Turn-Off Delay Time	R _{gen} = 4.7 Ohms)	td(off)	_	0 80	
Fall Time	72 84	tf	_	60	sak, To = .
Total Gate Charge	PD 125 Wal	Q_g	38 (Typ)	60	nC
Gate-Source Charge	(V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 10 Vdc, I _D = Rated I _D)	Qgs	16 (Typ)	min T. Avino (P	has halten
Gate-Drain Charge	- GS 481-01-05 - 1819-191	Qgd	22 (Typ)	EBROTESAG	A LES LABOR
OURCE DRAIN DIODE CHARACTERIS	TICS*				
Forward On-Voltage	(Is = Rated Ip,	V _{SD}	1.8 (Typ)	1.9(1)	Vdc
Forward Turn-On Time V _{GS} = 0) Reverse Recovery Time		ton	Limited by s	stray inductan	ce
		t _{rr}	450 (Typ)	sa for <u>5</u> Secol	ns
NTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured closer to the source pin and the cen	from the contact screw on the header ter of the die)	Ld	5 (Typ)	-	nH
Internal Source Inductance (Measure package to the source bond pad)	ed from the source pin, 0.25" from the	L _S	12.5 (Typ)		nH

^{*}Pulse Test: Pulse Width \leqslant 300 $\mu s,$ Duty Cycle \leqslant 2%. (1) Add 0.1 V for IRF240 and IRF241.

MOTOROLA ■ SEMICONDUCTOR **TECHNICAL DATA**

Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low rDS(on) to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETs 25 and 30 AMPERES rDS(on) = 0.085 OHM 150 and 200 VOLTS rDS(on) = 0.12 OHMS150 and 200 VOLTS

IRF250

IRF251 IRF252

IRF253





CASE 197A-02 TO-204AE

MAXIMUM RATINGS

00804		Symbol -	0 = 28V (IRF) = 20V)				11.4
Rating			250	251	252	253	Unit
Drain-Source Voltage		VDSS	200	150	200	150	Vdc
Drain-Gate Voltage (RGS = 20 kΩ)	(no)b [†]	VDGR	200	150	200	150	Vdc
Gate-Source Voltage		VGS	MgA 81 = 0±20 = 00V		Vdc		
Drain Current Continuous, T _C = 25°C T _C = 100°C Peak, T _C = 25°C	(110)b1	ID	30 25 19 16 120 100		6	Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	Ogd	P _D	betsR		50 V 01	= 89	Watts W/°C
Operating and Storage Temperature Range		TJ, Tstg	-55 to 150		°C		

THERMAL CHARACTERISTICS

Thermal Resista	ance — Junction to Case — Junction to Ambient	R _θ JC R _θ JA	0.83	°C/W
	Temp. for Soldering Purposes, e for 5 Seconds	TL	300	°C

See the MTM40N20 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

OU	TLINE DIMENSIONS
-	eanskasena rugalo
metine	Reventa Trant-8-
1	TITE STATE
LE	
	D 2 R
	# \$ 0.30 (0.012) ® T Q ® U
	[* 0 0.30 (0.012) ©] 1 Q @ 0
	-U-
1 /	0
H (-2+
1	+ •
1	
	-a-
	♦ φ 0.25 (0.010) ₩ T U ₩
	Gate-Drain Charge
	STYLE 3:
	PIN 1. GATE 2. SOURCE
	CASE. DRAIN
	CASE, UNAIN
NOTES:	
1 DIME	NSIONING AND TOLERANCING PER AM

NOT	ES:
1.	DIMENSIONING AND TOLERANCING PER ANS Y14.5M, 1982.
2.	CONTROLLING DIMENSION: INCH.

	MILLIN	METERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
A	38.36	39.37	1.510	1.550	
В	19.31	21.08	0.760	0.830	
C	6.35	8.25	0.250	0.325	
D	1.45	1.60	0.057	0.063	
E	1.53	1.77	0.060	0.070	
F	30.15	BSC			
G	10.92	2 BSC			
H	5.48	5.46 BSC		BSC	
J	16.89	16.89 BSC		BSC	
K	11.18	12.19	0.440	0.480	
Q	3.84	4.19	0.151	0.165	
R	25.15	26.67	0.990	1.050	
U	3.84	4.19	0.151	0.165	

ELECTRICAL CHARACTERISTICS (To = 25°C unless otherwise noted)

OMCHRI I	Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS			1991	5579 5	8	
Drain-Source Breakdown Volta (V _{GS} = 0, I _D = 0.25 mA)	ge	IRF250, IRF252 IRF251, IRF253	V(BR)DSS	200 150	ede <u>ra</u> le	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0, TJ = 125°C)			IDSS.	are tt sign!	0.2 TEN 15 WOO	mAdc
Gate-Body Leakage Current, Forward (V _{GSF} = 20 Vdc, V _{DS} = 0)			IGSSF	switc <u>h</u> ing ab s, conventen	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, Vps = 0)			IGSSR	ching Speed	100 Fast Swi	nAdc
ON CHARACTERISTICS*	PINCS		18 Dawnonke	On-Losses.	sauterenm	US(on)
Gate Threshold Voltage (VDS = VGS, ID = 0.25 mA)	90		VGS(th)	Dies 2 ation	nawo4 zi Al	DS Vdc
Static Drain-Source On-Resista (VGS = 10 Vdc, ID = 16 Add		IRF250, IRF251 IRF252, IRF253	rDS(on)	_	0.085 0.120	Ohm
On-State Drain Current (VGS = 10 V) (VDS \geq 2.5 Vdc) IRF250, IRF251 (VDS \geq 3.0 Vdc) IRF252, IRF253			I _{D(on)}	30 25	_	Adc
Forward Transconductance $(V_{DS} \ge 2.5 \text{ V}, I_D = 16 \text{ A})$ IRF250, IRF251 $(V_{DS} \ge 3.0 \text{ V}, I_D = 16 \text{ A})$ IRF252, IRF253			9FS	8 8	_	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance		200	Ciss		3000	pF
Output Capacitance	(VDS	$S = 25 \text{ V}, \text{ V}_{GS} = 0,$ f = 1 MHz	Coss	_	1200	
Reverse Transfer Capacitance	253	280 FBS 085	C _{rss}	_	500	
SWITCHING CHARACTERISTICS	987 GST	088 200 150 200	Y		арып	Source vo
Turn-On Delay Time	160 Vds		td(on)	_	35	ns
Rise Time	(V _{DD}	≈ 95 V, I _D = 16 Apk,	tr	_	100	aV ecruo
Turn-Off Delay Time	R	gen = 4.7 Ohms)	td(off)	_	125	Current
Fall Time	9	g 30 2	tf	_	2100 = 3	tinuous, 1
Total Gate Charge		1	Q_g	85 (Typ)	120	nC
Gate-Source Charge		= 0.8 Rated V _{DSS} , 10 Vdc, I _D = Rated I _D)	Qgs	45 (Typ)	Tim notheric	eid iewos
Gate-Drain Charge	O WY	1.2	Q _{gd}	44 (Typ)	- 5.83	evads en
SOURCE DRAIN DIODE CHARAC	TERISTICS*	Tatg -65 to 150	,LT	ersturs Range	orage Temp	ting and S
Forward On-Voltage		(I _S = Rated I _D ,	V _{SD}	1.2 (Typ)	1.8(1)	Vdc
Forward Turn-On Time			ton	Limited by s	tray inductar	nce less is
Reverse Recovery Time AUS		t _{rr}	200 (Typ)	gonul	ns	
NTERNAL PACKAGE INDUCTAN	CE	008 19	100	ildering Purpo	iemp. for St	turn Lead
Internal Drain Inductance (Mea closer to the source pin and th			L _d	5 (Typ)	daG a'nongieni	nH osumente
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)			L _S	12.5 (Typ)	_	nH

*Pulse Test: Pulse Width \leq 300 μs , Duty Cycle \leq 2%. (1) Add 0.2 V for IRF250 and IRF251.

MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

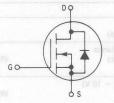
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low r_{DS(on)} to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



IRF330 IRF331 IRF333

TMOS POWER FETS 4.5 and 5.5 AMPERES rDS(on) = 1 OHM 350 and 400 VOLTS rDS(on) = 1.5 OHMS 350 VOLTS





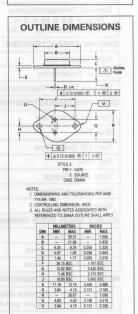
MAXIMUM RATINGS

D. et		0 1 1		IRF		Unit
Rating		Symbol	330	331	333	Unit
Drain-Source Voltage	Cost	VDSS	400	350	350	Vdc
Drain-Gate Voltage $(R_{GS} = 20 \text{ k}\Omega)$	Cres	VDGR	400	350	350	Vdc
Gate-Source Voltage	Table 1	VGS		± 20		Vdc
Drain Current Continuous, T _C = 25°C T _C = 100°C Peak, T _C = 25°C	rito (No)b [†]	ID	10.93	.5 .5	4.5 3 18	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	_B 0	PD	heboft	75 0.6	onW)	Watts W/°C
Operating and Storage Temperature Ran	ige	TJ, T _{stg}	= 01-	55 to 1	150 80	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	R _θ JC	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	300	°C

See the MTM5N35 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.



ELECTRICAL CHARACTERISTIC	(T _C = 25°C unless otherwise r	noted)
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	acteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	andalese.	T too	227 6	lain-	restare.
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)	IRF331, IRF333 IRF330	V(BR)DSS	350 400	el Enha	Vdc
Zero Gate Voltage Drain Current		IDSS	SOF	Al ens	mAdc
$(V_{DS} = Rated V_{DSS}, V_{GS} = 0)$ $(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0)$	0. Tı = 125°C)	ed for high	s are design	0.2	ese TMOS
Gate-Body Leakage Current, Forwa (VGSF = 20 Vdc, VDS = 0)		IGSSF	swit <u>ching</u> sers, converte	ewo100 eec Meluger pri	nAdc
Gate-Body Leakage Current, Reversion (VGSR = 20 Vdc, VDS = 0)	IGSSF	itching Spec	100 Fast Sw	nAdc	
Gate-Body Leakage Current, Revers (VGSR = 20 Vdc, VDS = 0)	se OM7	IGSSR	Nicological	100	nAdc
ON CHARACTERISTICS*	0.0	for Use With	haracterized	ain Diode C	1C-01-801U
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 0.25 mA)	FLA	V _{GS(th)}	2	42.050.	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 3 Adc)	IRF330, IRF331 IRF333	rDS(on)	_	1 1.5	Ohm
On-State Drain Current ($V_{GS} = 10$ ($V_{DS} \ge 5.5 \text{ Vdc}$) ($V_{DS} \ge 6.75 \text{ Vdc}$)	V) IRF330, IRF331 IRF333	ID(on)	5.5 4.5	=	Adc
Forward Transconductance (V _{DS} \geq 5.5 V, I _D = 3 A) (V _{DS} \geq 6.75 V, I _D = 3 A)	IRF330, IRF331 IRF333	9FS	3 3	_ 25WIT	mhos
DYNAMIC CHARACTERISTICS	RRI (1997)		polic	-0	
Input Capacitance	330 331 333	Ciss	- 0	900	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	_	300	in-Source
Reverse Transfer Capacitance	VDGR 400 350 380 Vec	C _{rss}	_	80	in-Gate Vo
SWITCHING CHARACTERISTICS*				112	rus = Sth
Turn-On Delay Time	20A 0Z = 55A	td(on)		30	ns
Rise Time	$(V_{DD} \approx 200 \text{ V}, I_D = 3 \text{ Apk},$	t _r	_	35	in Current antinuous
Turn-Off Delay Time	$R_{gen} = 15 \text{ Ohms}$	td(off)	_	0°00'55 0T	
Fall Time	22 18	tf	_	35	= Ol. XEE
Total Gate Charge	mew ev du	αg	18 (Typ)	30	nC
Gate-Source Charge	(V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 10 Vdc, I _D = Rated I _D)	Qgs	10 (Typ)	Sturena Tan	bas padsar
Gate-Drain Charge	- tgs to tao, ip tiated ip,	Q _{gd}	8 (Typ)	BUSSTOAN.	LEO LABOR
SOURCE DRAIN DIODE CHARACTER	STICS*		and other	december a source	Salamil Inventor
Forward On-Voltage	(I _S = Rated I _D	V _{SD}	1.2 (Typ)	1.5(1)	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited by s	tray inductar	ice
Reverse Recovery Time	J.	t _{rr}	420 (Typ)	se la -6 Seco	o-ns 8
NTERNAL PACKAGE INDUCTANCE (TO-204)	sub to the miniores	As not made as	Manuacia Pa	acviator
Internal Drain Inductance (Measure closer to the source pin and the ce	d from the contact screw on the heade nter of the die)	r L _d	5 (Typ)	_	nH
Internal Source Inductance (Measu package to the source bond pad)	red from the source pin, 0.25" from the	L _S	12.5 (Typ)	_	nH

*Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%. (1) Add 0.1 V for IRF330 and IRF331.

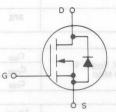
MOTOROLA SEMICONDUCTOR TECHNICAL DATA

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low rps(on) to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	VDSS	400	Vdc
Drain-Gate Voltage (RGS = 1.0 M Ω)	VDGR	400	Vdc
Gate-Source Voltage	VGS	± 20	Vdc
Drain Current Stabbil Varie vil Bellow Continuous Pulsed	I _D	10 40	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	125 00 1.0	Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stg}	-55 to 150	uid s,Cnos

THERMAL CHARACTERISTICS

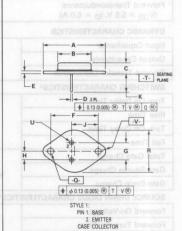
Thermal Resistance Junction to Case Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	300	°C

See the MTP8N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTP10N35 are applicable for this series of products.

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics - are given to facilitate "worst case" design.

Part Number	VDSS	rDS(on)	ID
IRF340	400 V	0.55 Ω	10 A





- DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
- ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

- 160	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
A	D900	39.37	00-en	1,550	
В	-	21.08	-	0.830	
C	6.35	8.25	0.250	0.325	
D	0.97	1.09	0.038	0.043	
E	1.40	1.77	0.055	0.070	
F	30.15 BSC		1.187 BSC		
G	10.92	BSC	0.430 BSC		
Н	5.46	BSC	0.215 BSC		
J	16.89	BSC	0.665	BSC	
K	11.18	12.19	0.440	0.480	
Q	3.84	4.19	0.151	0.165	
R	_	26.67	-	1.050	
U	4.83	5.33	0.190	0.210	
٧	3.84	4.19	0.151	0.165	

CASE 1-06 TO-204AA

MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise n	nerwise noted	unless	25°C	(Tc =	RISTICS	CHARACT	ELECTRICAL
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L	Characte	ristic	Symbol	Min	Max	Unit
	OFF CHARACTERISTICS					
-	Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)		V(BR)DSS	400		Vdc
	Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0, TJ	= 125°C)	IDSS	NHANCEN WER <u>T</u> HELL	0.25 1.00	mAdd
	Gate-Body Leakage Current, Forward $(V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0)$	gh voltage, high speed. ching regulators, con-	IGSSF	er FETis des optications	100	nAdc
	Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)		IGSSR	nd relay dris Fast Switchi	100 tola for	nAdc
	ON CHARACTERISTICS*	pecified at Elevated	-Losses. Sp	Minimiza On	6) (up)SQ)	WoJ 0
	Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 0.25 mA)	betim	V _{GS(th)}	2.0 Is Power D	4.0 AO2 be	Vdc
	Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 8.0 Adc)	r Use With Inductive	rDS(on)	Died <u>e</u> Charl	0.55	Ohm
	On-State Drain Current ($V_{GS} = 10 \text{ V}$) ($V_{DS} \ge 6.4 \text{ Vdc}$)		I _{D(on)}	10	_	Adc
	Forward Transconductance (V _{DS} ≥ 5.5 V, I _D = 5.0 A)		9FS	4.0	A ATTEN	mhos
	DYNAMIC CHARACTERISTICS					
	Input Capacitance		Ciss	- 0	1600	pF
	Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1.0 MHz)	Coss	-	450	
	Reverse Transfer Capacitance	1 = 1.0 (4)(12)	C _{rss}	_MY N	150	
	SWITCHING CHARACTERISTICS*			es c	SiAS L	
	Turn-On Delay Time		td(on)	_	35	ns
	Rise Time	$(V_{DD} = 25 \text{ V}, I_{D} = 5.0 \text{ Apk},$	t _r	_	15	
	Turn-Off Delay Time	$R_{gen} = 4.7 \text{ Ohms}$	td(off)	_	90	
	Fall Time		tf	_	35	SALE INVESTIGATION OF
	Total Gate Charge	A Jinka p. dvigV lod	Qg	40 (Typ)	60	nC
	Gate-Source Charge	(V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 10 Vdc, I _D = Rated I _D)	Qgs	20 (Typ)	ancun'	BOILEGE .
	Gate-Drain Charge	aby BOY of	Qgd	20 (Typ)	Lost	oV ets8.vo
	SOURCE DRAIN DIODE CHARACTERIST	CS*	ar Nag		HIM	0.1 = 85
	Forward On-Voltage	(IS = Rated ID,	V _{SD}	1.1 (Typ)	2.0	Vdc
	Forward Turn-On Time	$V_{GS} = 0$	ton	Limited by s	tray inductar	nce
	Reverse Recovery Time	10	3 t _{rr}	600 (Typ)	_	ns
	INTERNAL PACKAGE INDUCTANCE				malte	O nonacetti
	Internal Drain Inductance (Measured from closer to the source pin and the center of		Ld	5 (Typ)	C — e 25°C	THR= 25
	Internal Source Inductance (Measured fr package to the source bond pad)	om the source pin 0.25" from the	LS	12.5 (Typ)	Storage	as gnHs

*Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

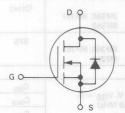
IRF350 IRF351 IRF352

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low rDS(on) to Minimize On-Losses. Specified at Elevated
 Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MAXIMUM RATINGS

oer oer			Def — Mole!				Roos
Rating			Symbol	350	351	352	Unit
Drain-Source Voltage	110 (Ty	105	VDSS	400	350	400	Vdc
(Roc = 10 MO)	60 (Typ	89	VDGR	400	350	400	Vdc
Gate-Source Voltage		VGS		± 20		Vdc	
Drain Current Continuous Pulsed		I _D		5 gl be	13 52	Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	1200 (17)	33	PD		150 1.2		Watts W/°C
Operating and Storage Temperature Range	district.		T _J , T _{stg}		55 to 1		°C

THERMAL CHARACTERISTICS

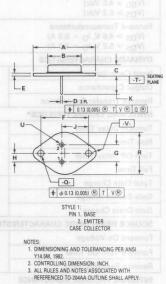
Thermal Resistance Junction to Case Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	300	°C

See the MTH15N35 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTH15N35 are applicable for this series of products.

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Part Number	VDSS	rDS(on)	ID
IRF350	400 V	0.3 Ω	15 A
IRF351	350 V	0.3 Ω	15 A
IRF352	400 V	0.4 Ω	13 A





	MILLIN	HETERS	INC	HES	
DIM	MIN MAX		MIN	MAX	
A	ni-ni	39.37	02-80	1.550	
В	-	21.08	-	0.830	
C	6.35	8.25	0.250	0.325	
D	0.97	1.09	0.038	0.043	
	1.40	1.77	0.055	0.070	
F	30.15	BSC	1.187	BSC	
G	10.92	BSC	0.430	BSC	
Н	5.48	BSC	0.215	BSC	
J	16.89	BSC	0.665	BSC	
K	11.18	12.19	0.440	0.480	
Q	Q 3.84	3.84 4.19	4.19	0.151	0.165
R	-	26.67	_	1.050	
U	4.83	5.33	0.190	0.210	
٧	3.84	4.19	0.151	0.165	

CASE 1-06 TO-204AA ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Charact	eristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)		IRF351 IRF350, IRF352	V _{(BR)DSS}	350 400		Vdc
Zoro Coto Voltago Drain Current	9		Inco			mAdc
Zero Gate Voltage Drain Current $(V_{DS} = Rated\ V_{DSS}, V_{GS} = 0)$ $(V_{DS} = 0.8\ Rated\ V_{DSS}, V_{GS} = 0, T$		DE SILICON GATI TRANSISTOR	IDSS		0.25 1.00	made
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		or high voltage, high switching regulators		wer FETs at sing applica	TV001 Po	nAdc peeds
Gate-Body Leakage Current, Reverse (V _{GSR} = 20 Vdc, V _{DS} = 0)			IGSSR	d and relay Fast Switch	ers, 00fend n Gate for	nAdc
ON CHARACTERISTICS*		cified at Elevated	-Losses, Spe	Minimize On	Lot moters	wal e
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = 0.25 \text{ mA})$		hatis	V _{GS(th)}	2.0	4.0 ste	obVemp
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 8.0 Adc)		IRF350, IRF351 IRF352	rDS(on)	Diode_Chara	0.3 0.4	Ohm
On-State Drain Current ($V_{GS} = 10 \text{ V}$) ($V_{DS} \ge 4.5 \text{ Vdc}$) ($V_{DS} \ge 5.2 \text{ Vdc}$)		IRF350, IRF351 IRF352	lD(on)	15 13	. <u>. 4</u> 111	Adc
Forward Transconductance ($V_{DS} \ge 4.5 \text{ V}$, $I_D = 8.0 \text{ A}$) ($V_{DS} \ge 5.2 \text{ V}$, $I_D = 8.0 \text{ A}$)		IRF350, IRF351 IRF352	9FS	8.0 8.0	=	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance				787 (3000	pF
Output Capacitance		= 25 V, V _{GS} = 0, = 1.0 MHz)	Coss	GS to	600	
Reverse Transfer Capacitance			C _{rss}	_	200	
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time			t _d (on)	_	35	ns
Rise Time	$(V_{DD} = 3)$	25 V, I _D = 8.0 Apk,	tr	_	65	NUMBER OF
Turn-Off Delay Time	Rger	1 = 4.7 Ohms)	td(off)	_	150	
Fall Time	Unit	ol 360 361 362	dray8 tf	_	75	
Total Gate Charge	Vde	400 350 400	Q_g	110 (Typ)	120	901 nC
Gate-Source Charge		0.8 Rated V _{DSS} , Vdc, I _D = Rated I _D)	Qgs	60 (Typ)	— egs	n-Gate Vol
Gate-Drain Charge	GO		Qgd	50 (Typ)	13.110	0.0 = 2.0
SOURCE DRAIN DIODE CHARACTERIS	TICS*	VAZ	89.A		059310	A Stunder
Forward On-Voltage	(Is	= Rated ID,	V _{SD}	_	1.5(1)	Vdc
Forward Turn-On Time		V _{GS} = 0)	t _{on}	Limited by s	stray inducta	nce beat
Reverse Recovery Time			19 t _{rr}	1200 (Typ)	mo ll agies	3 avns
INTERNAL PACKAGE INDUCTANCE	Watts				2020	Tc = 25°C
Internal Drain Inductance (Measured fr closer to the source pin and the center		screw on the header	e LT Ld	5 (Typ)	Storage	nH one gnue
Internal Source Inductance (Measured	from the source	e pin 0.25" from the	L _S	12.5 (Typ)	ARACTER	mperaturi

MOTOROLA SEMICONDUCTOR **TECHNICAL DATA**

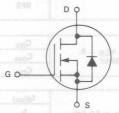
IRF440

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

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- Low rDS(on) to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive





MAXIMUM RATINGS

			× 8	O = IF	RF	8 = 18
Rati	ing (GVT) OS		Symbol	440	441	Unit
Drain-Source Voltage			VDSS	500	450	Vdc
Drain-Gate Voltage (RGS = 1.0 M Ω)			V _{DGR}	500	450	Vdc
Gate-Source Voltage		no.	VGS	±	20	Vdc
Drain Current Continuous Pulsed (qvT)		ρJ	I _D		.0	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	12:5 (Typ)	Łg	PD	1.	25 .0	Watts W/°C
Operating and Storage Temperature Range			T _J , T _{stg}	- 55	to 150	°C

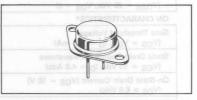
THERMAL CHARACTERISTICS

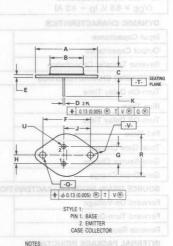
Thermal Resistance			°C/W
Junction to Case Junction to Ambient	$R_{\theta}JC$ $R_{\theta}JA$	1.0 30	
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	300	°C

See the MTP8N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics are given to facilitate "worst case" design.







- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.

3.	ALL RULES A	ND NOTES	ASSOCIA	TED WI	TH
	REFERENCED	TO-204AA	OUTLINE	SHALL	APPLY.

	MILLIN	METERS	INC	HES		
DIM	MIN	MAX	MIN	MAX		
A	635万00	39.37	HAT DE	1.550		
В	-	21.08	-	0.830		
C	6.35	8.25	0.250	0.325		
D	0.97	1.09	0.038	0.043		
E	1.40	1.77	0.055	0.070		
F	30.15	BSC	1.187	BSC		
G	10.92	10.92 BSC		BSC		
Н	5.48	BSC	0.215 BSC			
J	16.89	BSC	0.665	BSC		
K	11.18	12.19	0.440	0.480		
Q	3.84	4.19	0.151	0.165		
R	-	26.67	-	1.050		
U	4.83	5.33	0.190	0.210		
V	3.84	4.19	0.151	0.165		

CASE 1-06 TO-204AA

Charact	Symbol	Min	Max	Unit			
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)				V _{(BR)DSS}	450	-	Vdc
Zero Gate Voltage Drain Current $(V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0)$ $(V_{DS} = 0.8\ Rated\ V_{DSS},\ V_{GS} = 0.1)$	Г _Ј = 125°С)	N GATE	E SILICO	IDSS	HANCEM	0.25 1.0	mAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		rigin ,ageti	or high vo	IGSSF	ner FETs an	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)		,210/61/1901	Bumminas	IGSSR	d and relay	100	nAdc
ON CHARACTERISTICS*				speeds 5	HIDDIWG JEB-	101 9385	nuome w
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 mA)		betavel	is its being	VGS(th)	2.0	4.0	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, I _D = 4.0 Adc)		evitaubn	ited Use With fa	rDS(on)	s Pov <u>re</u> r Districted Gode Chara	0.85	Ohm
On-State Drain Current ($V_{GS} = 10 \text{ V}$) ($V_{DS} \ge 6.8 \text{ Vdc}$)				ID(on)	8.0	-	Adc
Forward Transconductance (V _{DS} ≥ 6.8 V, I _D = 4.0 A)			9.0	9FS	4.0	-	mhos
DYNAMIC CHARACTERISTICS			-			0.4399	
Input Capacitance		1	174	C _{iss}		1600	pF
Output Capacitance	(VDS =	= 25 V, VGS = 1.0 MHz)	= 0,	Coss	_	350	
Reverse Transfer Capacitance	1	= 1.0 IVIHZ)		C _{rss}		150	
SWITCHING CHARACTERISTICS*		/		100	MIT	AN 1107	
Turn-On Delay Time				td(on)	_ = ==	35	ns
Rise Time	(Vpp ≈ 2	(V _{DD} ≈ 200 V, I _D = 4.0 Apk,				15	
Turn-Off Delay Time		= 4.7 Ohm		t _r	_	90	
Fall Time				tf		30	1
Total Gate Charge				Qa	40 (Typ)	60	nC
Gate-Source Charge	(VGS =	10 V, V _{DS} =	0.8 ×	Qgs	20 (Typ)	_	1
Gate-Drain Charge	nated vD	SS, ID = Rat	red ID)	Q _{qd}	20 (Typ)	BaS_	
SOURCE DRAIN DIODE CHARACTERIS	TICS*	600 460	Voss			epsil	т-Source Vo
Forward On-Voltage	(le	= Rated ID,	REGV	V _{SD}		2.0	Vdc
Forward Turn-On Time		$V_{GS} = 0$		ton	Limited by s	tray induct	ance
Reverse Recovery Time			Ves	t _{rr}	600 (Typ)	9589	ns
INTERNAL PACKAGE INDUCTANCE	Ade .	0.0					Inempor
Internal Drain Inductance (Measured fr closer to the source pin and the center		screw on th	e header	L _d	5 (Typ)	-	nH
Internal Source Inductance (Measured source bond pad)	from the source	e pin 0.25" fr	om the	L _S	12.5 (Typ)	2585	To Hagese
ulse Test: Pulse Width \leq 300 μ s, Duty Cycle	≤ 2.0%.	- 65 to 150	gleT (T				ating and S

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

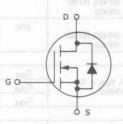
IRF450 IRF451 IRF452

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

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MAXIMUM RATINGS

		(flotb)		IRF		nagh
Rating		Symbol	450	451	452	Unit
Drain-Source Voltage	(gyT) 011	VDSS	500	450	500	Vdc
Drain-Gate Voltage (R _{GS} = 1.0 MΩ)	50 (Typ) 50 (Typ)	VDGR	500	450	500	Vdc
Gate-Source Voltage		VGS		±20		Vdc
Drain Current Continuous Pulsed	Limited by st	I _D	35	3	12 48	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	(qv1) 9081	PD	ushnar	150 1.2	S 10000000	Watts W/°C
Operating and Storage Temperature Range	12.5 (Typ)	T _J , T _{stg}		55 to 1		°C

THERMAL CHARACTERISTICS

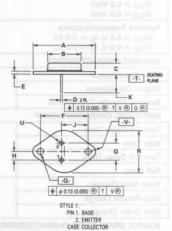
Thermal Resistance Junction to Case Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	300	°C

See the MTH13N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristss — are given to facilitate "worst case" design.

Part Number	VDSS	rDS(on)	ID
IRF450	500 V	0.4 Ω	13 A
IRF451	450 V	0.4 Ω	13 A
IRF452	500 V	0.5 Ω	12 A





NOTES:

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI

244 EM 1992

Y14.5M, 1982.

2. CONTROLLING DIMENSION: INCH.

3. ALL RULES AND NOTES ASSOCIATED WITH
REFERENCED TO-204AA OUTLINE SHALL APPLY.

	MILLIM	ETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
A	-	39.37	-	1.550	
В	10110	21.08	0.17709	0.830	
C	6.35	8.25	0.250	0.325	
D	0.97	1.09	0.038	0.043	
E	1.40	1.77	0.055	0.070	
F	30.15	BSC	1.187 BSC		
G	10.92	BSC	0.430 BSC		
Н	5.46	BSC	0.215 BSC		
J	16.89	BSC	0.665	BSC	
K	11.18	12.19	0.440	0.480	
Q	3.84	4.19	0.151	0.165	
R	-	26.67	-	1.050	
U	4.83	5.33	0.190	0.210	
٧	3.84	4.19	0.151	0.165	

CASE 1-06 TO-204AA

Characteristic			Symbol	Min	Max	Unit	
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)		IRF451	V _{(BR)DSS}	450	_	Vdc	
		IRF450, IRF452		500			
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0, TJ =			IDSS	HANGEM ER RELD	0.25 1.00	mAdc	
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	411	or high voltage, hig	IGSSF	wer FETs an	100	nAdc	
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)		switching regulators	IGSSR	and relay	100	nAdc	
ON CHARACTERISTICS*			speads bu	ast Switchill	101 9782 1	iogilic =	
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 0.25 mA)		cified at Elevated	V _{GS(th)}	2.0	4.0	Vdc	
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 7.0 Adc)		IRF450, IRF451	rDS(on)	s Power Dis Diode-Chara	0.4	Ohm	
On-State Drain Current (V _{GS} = 10 V) (V _{DS} ≥ 5.2 Vdc) (V _{DS} ≥ 6.0 Vdc)		IRF450, IRF451 IRF452	I _{D(on)}	13 12		Adc	
Forward Transconductance $(V_{DS} \ge 5.2 \text{ V, I}_D = 7.0 \text{ A})$ $(V_{DS} \ge 6.0 \text{ V, I}_D = 7.0 \text{ A})$		IRF450, IRF451 IRF452	9FS	6.0 6.0	nd#	mhos	
DYNAMIC CHARACTERISTICS							
Input Capacitance	(4)		Ciss	- 1	3000	pF	
Output Capacitance		25 V, V _{GS} = 0, 1.0 MHz)	Coss	- 307	600		
Reverse Transfer Capacitance			C _{rss}	-8	200		
SWITCHING CHARACTERISTICS*		2.0		Torontemones	MARKET AND		
Turn-On Delay Time			td(on)		35	ns	
Rise Time	(V _{DD} ≈ 20	$0 \text{ V, I}_{D} = 7.0 \text{ Apk,}$	t _r	_	50	я момих	
Turn-Off Delay Time	Rgen	= 4.7 Ohms)	td(off)	-	150		
Fall Time	Unit	d 450 451 452	tf	_	70		
Total Gate Charge	Vde V	800 480 800	Qg	110 (Typ)	120	nC	
Gate-Source Charge) V, V _{DS} = 0.8 × S, I _D = Rated I _D)	Qgs	50 (Typ)	908	n-Gate Volt	
Gate-Drain Charge	50	0, 0	Qgd	60 (Typ)	(O)	10.1 - 20	
SOURCE DRAIN DIODE CHARACTERISTICS	Vdc *	±20	SpA		Itage	Source Vo	
Forward On-Voltage	(Is	= Rated ID,	V _{SD}	_	1.3(1)	Vdc	
Forward Turn-On Time	V	GS = 0)	ton	Limited by s	tray inducta	nce	
Reverse Recovery Time			t _{rr}	1200 (Typ)	noiteals	ns	
INTERNAL PACKAGE INDUCTANCE	Watts	150					
Internal Drain Inductance (Measured from t closer to the source pin and the center of t		screw on the header	Ld	5 (Typ)	25°C_ Storage	nH	
Internal Source Inductance (Measured from package to the source bond pad)	the source	pin 0.25" from the	L _S	12.5 (Typ)	Rang <u>a.</u> ARACT ER B	nH	
ulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2. Add 0.1 V for IRF450 and IRF451.	0%. WO	68.0	Rusc			rmal Resista	
AAMS-OT							

MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

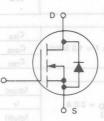
IRF510 IRF511 IRF512 IRF513

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

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- · Silicon Gate for Fast Switching Speeds
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- Source-to-Drain Diode Characterized for Use With Inductive Loads





MAXIMUM RATINGS

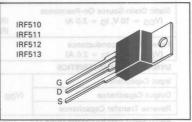
		IF	RF		
Symbol	510	511	512	513	Unit
VDSS	100	60	100	60	Vdc
V _{DGR}	100	60	100	60	Vdc
VGS		±	20		Vdc
ID	4.0	4.0	3.5	3.5	Adc
ID	2.5	2.5	2.0	2.0	Adc
IDM	16	16	14	14	Adc
PD	2		THE STATE OF THE S		Watts W/°C
T _J ,T _{stg}	JOIT 1	- 55	to 150		°C
	VDSS VDGR VGS ID ID PD	VDSS 100 VDGR 100 VGS 1D 4.0 ID 2.5 IDM 16 PD	Symbol 510 511 VDSS 100 60 VDGR 100 60 VGS ± 10 4.0 ID 4.0 4.0 16 16 IDM 16 16 16 2 PD 2 0 0 0 0	V _{DSS} 100 60 100 V _{DGR} 100 60 100 V _{GS} ±20 I _D 4.0 4.0 3.5 I _D 2.5 2.5 2.0 I _{DM} 16 16 14 P _D 20 0.16	Symbol 510 511 512 513 VDSS 100 60 100 60 VDGR 100 60 100 60 VGS ±20 10 3.5 3.5 ID 2.5 2.5 2.0 2.0 IDM 16 16 14 14 PD 20 0.16 0.16

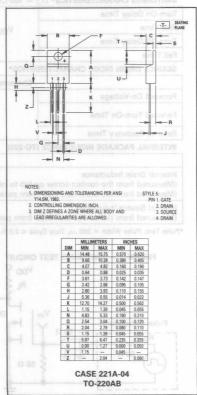
THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	R _O JC R _O JA	6.4 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	PO TL	tuo V 300 ug	°C

See the MTP6N10 Designer's Data Sheet for a complete set of design curves for this product.

Part Number	VDS	rDS(on)	ID
IRF510	100 V	0.6 Ω	4.0 A
IRF511	60 V	0.6 Ω	4.0 A
IRF512	100 V	0.8 Ω	3.5 A
IRF513	60 V	0.8 Ω	3.5 A





Char	racteristic	Symb	ol Min	Тур	Max	Unit
FF CHARACTERISTICS				ATA	U JAC	AMH
rain-Source Breakdown Voltage (VGS = 0, I _D = 250 μA)	IRF510,512 IRF511,513	V _{(BR)D}	SS 100 60	_	=	Vdc
ero Gate Voltage Drain Current (VGS = 0 V, VDS = Rated VDSS)		IDSS			0.25	mAdc
$(V_{GS} = 0 \text{ V}, V_{DS} = 0.8 \text{ Rated } V_{DS})$				_	1.0	
	Part 8	IGSS	F -	_	100	nAdc
everse Gate-Body Leakage Current (VGS = -20 V, VDS = 0)	RAI STAD V	IGSS	RASIMATOM	AHITS .	-100	nAdc
N CHARACTERISTICS*	701	BEAU COST AND RESIDEN	W. 1-5 ST-	130005	1000	I STATE OF
ate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μA)		VGS(t	h) 2.0	ritching	4.0	Vdc
n-State Drain Current	100000000	ID(or		total and	Hote D. no	Adc
$(V_{DS} = 25 \text{ V}, V_{GS} = 10 \text{ V})$	IRF510,511 IRF512,513	hetini Loo	4.0 3.5	19 10	10	buff e
tatic Drain-Source On-Resistance		bal daw eat rDS(o		in Diode	oC-ot-apt	Ohms
$(V_{GS} = 10 \text{ V}, I_D = 2.0 \text{ A})$	IRF510,511 IRF512,513	0.03(0	_		0.6	sod .
	: श्वामा : स्वामा	9FS	1.0	-	-	mhos
YNAMIC CHARACTERISTICS		9 4				
put Capacitance		Ciss	- 1	2	150	pF
utput Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0, f)$	OS = 25 V, V _{GS} = 0, f = 1.0 MHz) C _{OSS} —		-	100	
everse Transfer Capacitance		C _{rss}		_	25	
WITCHING CHARACTERISTICS* (T	J = 100°C)	・「「」」	00	100		
urn-On Delay Time		td(or	n) —	MY NEW	20	ns
ise Time	V _{DD} ≈ 0.5 V _{DSS} , I _D	= 2.0 A t _r	-	6277	25	1
urn-Off Delay Time	$Z_0 = 50 \Omega$	t _d (of	f) —	_	25	
all Time		tf		_	20	
OURCE DRAIN DIODE CHARACTE	RISTICS*					
	Characteristic		Sy	mbol	Тур	Unit
orward On-Voltage			V	SD	2.0	Vdc
orward Turn-On Time	(I _S = Rated I		ya t	t _{on}		by stray
leverse Recovery Time	00 00 Vdc	088 1001 880	V			ns
NTERNAL PACKAGE INDUCTANCE	(TO-220)	11 08 001 986	IV.		spark	Gate Ve
W lea-		Symb	ol Min	Тур	Max	Unit
nternal Drain Inductance Measured from the contact screw of Measured from the drain lead 0.25°			292	3.5	erii Leist	nH Laugun
nternal Source Inductance Measured from the source lead 0.2	a 16 Adc 1 sun	L _s	-	7.5	Pumed	Curient
llse Test: Pulse Width ≤ 300 μs, Duty C	ycle ≤ 2.0 %. RESISTIVE SV	VITCHING	_ SWITCHING		ORMS	ricesori ste above ste above
	RL Vout	td(on) + ton	tr	^t d(off) →	toff =	LAMAL nel Res
V _i Pulse Generator	DUT	A.8 8.58	90%		90%	of moitor
Pulse Generator $z = 50 \Omega$		Inverted			di Tempi	-
50 Ω	Supplement of the	of revisio ripusto lo re/s	talinmos a tot to	90% -	ampland o	

MOTOROLA ■ SEMICONDUCTOR **TECHNICAL DATA**

Power Field Effect Transistor

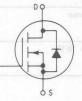
N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low r_{DS(on)} to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads







CARRIE CON GO

IRF520

TMOS POWER FETS 7 and 8 AMPERES rDS(on) = 0.3 OHM 60 and 100 VOLTS rDS(on) = 0.4 OHMS 60 and 100 VOLTS



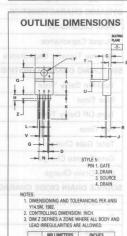
MAXIMUM RATINGS

00 Pasta	Rating		Symbol		IRF			
Kating			Symbol	520	521	522	523	Unit
Drain-Source Voltage		(instant)	VDSS	100	60	100	60	Vdc
Drain-Gate Voltage (RGS = 20 kΩ)		1)	VDGR	100	60	100	60	Vdc
Gate-Source Voltage		(Holb)	VGS	10000	±	20		Vdc
Drain Current Continuous, $T_C = 25^{\circ}C$ $T_C = 100^{\circ}C$ Peak, $T_C = 25^{\circ}C$	73 (Typ)	60 100	I _D	Vpss	8 5 12	75	7	Adc
Total Power Dissipation @ T Derate above 25°C	C = 25°C	ppp	PD			32		Watts W/°C
Operating and Storage Temp	perature Range	OSV	TJ, Tstg	-60	- 55	to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	R _θ JC	3.12	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	300	°C

See the MTP10N10E Designer's Data Sheet for a complete set of design curves for the product on this data sheet.



	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
A	14.48	15.75	0.570	0.620	
В	9.66	10.28	0.380	0.405	
C	4.07	4.82	0.160	0.190	
D	0.64	0.88	0.025	0.035	
F	3.61	3.73	0.142	0.147	
G	2.42	2.66	0.095	0.105	
Н	2.80	3.93	0.110	0.155	
J	0.36	0.55	0.014	0.022	
K	12.70	14.27	0.500	0.562	
L	1.15	1.39	0.045	0.058	
N	4.83	5.33	0.190	0.210	
Q	2.54	3.04	0.100	0.120	
R	2.04	2.79	0.080	0.110	
S	1.15	1.39	0.045	0.055	
T	5.97	6.47	0.235	0.255	
U	0.00	1.27	0.000	0.050	
٧	1.15	_	0.045	_	
Z	-	2.04	-	0.080	

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

002201	Characte	ristic		Symbol	Min	Max	Unit
FF CHARACTERISTICS							
Drain-Source Breakdown Vo (VGS = 0, ID = 0.25 mA)	V _(BR) DSS	60 100	Heid Name	Vdc			
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0, TJ = 125°C)					_80	0.2	mAdc
Gate-Body Leakage Current, (VGSF = 20 Vdc, VDS =				IGSSF	are <u>designa</u> switching ap	100	nAdc
Gate-Body Leakage Current, (VGSR = 20 Vdc, VDS =				IGSSR	-	100	nAdc
ON CHARACTERISTICS*	367	10000		Scentiled at	On-Losses	or rest swi	Lesso noun
Gate Threshold Voltage (VDS = VGS, ID = 0.25 m	nA)	COLON I		V _{GS(th)}	2 Dissipation	mpe k iture AA is Power	Vdc
Static Drain-Source On-Resi (VGS = 10 Vdc, ID = 4 A		IRF520, IRI IRF522, IRI		rDS(on)	varacterized —	0.3 0.60 0.4	Ohm Tue
On-State Drain Current (VGS (VDS ≥ 2.4 Vdc) (VDS ≥ 2.8 Vdc)	s = 10 V)	IRF520, IRI IRF522, IRI		I _{D(on)}	8 7	=	Adc
Forward Transconductance $(V_{DS} \ge 2.4 \text{ V, } I_D = 4 \text{ A}) \\ (V_{DS} \ge 2.8 \text{ V, } I_D = 4 \text{ A}) \\ \text{IRF520, IRF521} \\ \text{IRF522, IRF523}$				9FS	1.5 1.5	=	mhos
YNAMIC CHARACTERISTICS							
Input Capacitance				Ciss	_	600	pF
Output Capacitance		$(V_{DS} = 25 \text{ V}, V_{GS} = 0)$ f = 1 MHz),	Coss	_	400	AR MUMIX
Reverse Transfer Capacitano	e ga	481 141127	Jodanyi	C _{rss}	-	100	
WITCHING CHARACTERISTIC	S*	820 521 522 523					
Turn-On Delay Time	Vide	69 001 09 001	ssov	td(on)	_	40	ns
Rise Time	384	$(V_{DD} \approx 0.5 V_{DSS}, I_{D} = 4)$	Apk,	t _r	_	70	ain-Gme Vo
Turn-Off Delay Time	rstadi	R _{gen} = 50 Ohms)	20V	td(off)	_	100	(808 = 508)
Fall Time	ana		60.	tf		70	A STATE OF THE STATE OF T
Total Gate Charge		Y 8	Q)	Qg	13 (Typ)	0 a 15 o T	nC nC
Gate-Source Charge		(VDS = 0.8 Rated VDS: VGS = 10 Vdc, ID = Rate		Qgs	7 (Typ)	1C = 100°C	Peak, Tc =
Gate-Drain Charge	offic U	- GS - TO TGG, TD = Hate	0/	Q _{gd}	6 (Typ)	(ii) and	O volument land
OURCE DRAIN DIODE CHAR	ACTERISTIC	CS* 96.0	- Cr		9	125°C	Derate show
Forward On-Voltage	0	(IS = Rated ID,	ntaT (L)	V _{SD}	1.4 (Typ)	2.3(1)	Vdc
Forward Turn-On Time		$V_{GS} = 0$		ton	Limited by s	tray inductan	ice o James
Reverse Recovery Time	With		Raic	t _{rr}	280 (Typ)	mut — sons	ns
NTERNAL PACKAGE INDUCT	ANCE	62.5	ALBA	700	tion to Ambie	mut —	
Internal Drain Inductance (Measured from the conta (Measured from the drain			e)	Ld	3.5 (Typ) 4.5 (Typ)	d Temp. for I se for <u>5</u> Seco	sxim Hn² Lea 1/81 from Ca
(Measured from the drain lead 0.25" from package to center of die) Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)				L _S	7.5 (Typ)		77 MIN TO 1 THE SEC

*Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%. (1) Add 0.1 V for IRF520 and IRF521.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

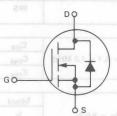
IRF530 IRF531 IRF532 IRF533

N-CHANNEL	ENHANCE	MENT-MOI	DE SILICON	GATE
TMOS P	OWER FIEL	D EFFECT	TRANSISTO	R

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MAXIMUM RATINGS

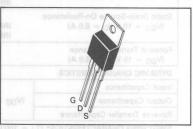
			IF	RF		
Rating no	Symbol	530	531	532	533	Unit
Drain-Source Voltage	VDSS	100	60	100	60	Vdc
Drain-Gate Voltage $(R_{GS} = 1.0 \text{ M}\Omega)$	VDGR	100	60	100	60	Vdc
Gate-Source Voltage	VGS		±	20		Vdc
Continuous Drain Current T _C = 25°C	1 _D	14	14	12	12	Adc
Continuous Drain Current T _C = 100°C	ID	9.0	9.0	8.0	8.0	Adc
Drain Current — Pulsed	IDM	56	56	48	48	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75 0.6			90100	Watts W/°C
Operating and Storage Temperature Range	T _J ,T _{stg}	P4	- 55 t	to 150		°C

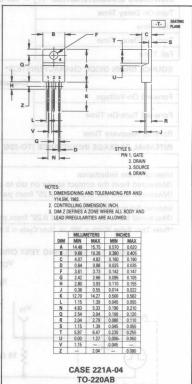
THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	R _O JC R _O JA	1.67 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T _L ³⁰	300	°C

See the MTM12N10 Designer's Data Sheet for a complete set of design curves for this product.

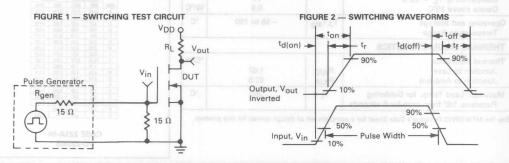
Part Number	VDS	rDS(on)	ID
IRF530	100 V	0.18 Ω	14 A
IRF531	60 V	0.18 Ω	14 A
IRF532	100 V	0.25 Ω	12 A
IRF533	60 V	0.25 Ω	12 A





วิลิกรีวินิrce breakdown voltage (VGS = 0, ID = 250 μA)	IRF530,532 IRF531,533	V(BR)DSS	100 60	Ξ	=	Vdc
Zero Gate Voltage Drain Current		IDSS				mAdc
(VGS = 0 V, VDS = Rated VDSS)				0.25 1.0		
(V _{GS} = 0 V, V _{DS} = 0.8 Rated V _D Forward Gate-Body Leakage Curren	loose			100	nAdc	
(VGS = 20 V, VDS = 0)	IGSSF			100	HAUC	
Reverse Gate-Body Leakage Current (VGS = -20 V, VDS = 0)	E SILICON GATE IRE	IGSSR	NIGEN NELLE	L ENION	-100	nAdc
ON CHARACTERISTICS*	and another and a	al manusiants	ove of 2	D	DOMET A	i ry
Gate Threshold Voltage (Vps = Vgs, Ip = 250 μA)	witching regulators, IRF	VGS(th)	2.0	stei m ig a	4.0	Vdc
On-State Drain Current (V _{DS} = 25 V, V _{GS} = 10 V)	IRF530,531	I _{D(on)}	14 12	or Fast S	on Gate	Adc
Santia Dania Sauran On Basistera	IRF532,533	The State of the S	Charac	ibniC nie	10-ol-ad	-
Static Drain-Source On-Resistance (VGS = 10 V, ID = 8.0 A)	IRF530,531	rDS(on)	_	_	0.18	Ohm
1,03	IRF532,533			_	0.25	
Forward Transconductance (V _{DS} = 15 V, I _D = 8.0 A)	Q.C	9FS	4.0	_	<u>-</u>	mhos
DYNAMIC CHARACTERISTICS			1.00			1
Input Capacitance		Ciss	-	-	800	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz})$	Coss	-		500	
Reverse Transfer Capacitance	\ 4 [7]	C _{rss}	+		150	
SWITCHING CHARACTERISTICS* (T	J = 100°C)			WTY E	B7	
Turn-On Delay Time		td(on)	+ 1		30	ns
Rise Time	$V_{DD} \simeq 36 \text{ V, I}_{D} = 8.0 \text{ A}$	tr	_	_	75	
Turn-Off Delay Time	$Z_{O} = 15 \Omega$	td(off)	_		40	
Fall Time		tf	_	_	45	
SOURCE DRAIN DIODE CHARACTE	RISTICS*					
4.00	Characteristic		Syr	nbol	Тур	Unit
Forward On-Voltage			V	SD	2.3	Vdc
Forward Turn-On Time	$(I_S = Rated I_D, V_{GS} = 0)$	Symbol 53	t	on		by stra
Reverse Recovery Time	e e0 100 60 Vdc	Vpss 10	t	rr	360	ns
INTERNAL PACKAGE INDUCTANCE	(TO-220)	OF ROOV			tage	Gate Vo
ALSO :		Symbol	Min	Тур	Max	Unit
Internal Drain Inductance (Measured from the contact screw of		Ld	28 <u>11</u>	3.5	omego sin_Cutre	nH
(Measured from the drain lead 0.25	from package to center of die)	R. - al -	3 70 01	4.5	mu Din ig	D sugur
Internal Source Inductance	5" from package to source bond pad.)	Ls	_	7.5	best on —	Current

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0 %.



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

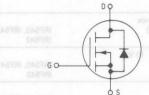
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

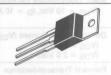
- · Silicon Gate for Fast Switching Speeds
- Low rps(on) to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



IRF540 IRF541 IRF542

TMOS POWER FETS 24 and 27 AMPERES FDS(on) = 0.085 OHM 60 and 100 VOLTS FDS(on) = 0.11 OHMS 100 VOLTS





CASE 221A-04 (TO-220AB)

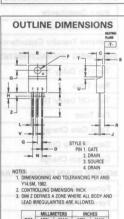
MAXIMUM RATINGS

008	ating		Combal		Unit		
oos Hat	ing		Symbol	540 541 54		542	Unit
Drain-Source Voltage			V _{DSS}	100	60	100	Vdc
Drain-Gate Voltage (RGS = 20 kΩ)		(ne)b ²	VDGR	100	60	100	Vdc
Gate-Source Voltage		Model	VGS	#0 T = ±20		Vdc	
Drain Current Continuous, $T_C = 25^{\circ}C$ $T_C = 100^{\circ}C$ Peak, $T_C = 25^{\circ}C$	40 (Typ)	yi gO	ID Voss	1	7 7 08	24 15 96	Adc
Total Power Dissipation @ T Derate above 25°C	C = 25°C	bgO	PD	= Qi	125 1	20	Watts W/°C
Operating and Storage Temp	perature Rang	je	T _J , T _{sta}		55 to 1	50	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	R _θ JC R _θ JA	1 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes,	TL	300	°C
1/8" from Case for 5 Seconds			

See the MTP25N10 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.



	MILLIN	METERS	INC	HES
MIC	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
В	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
Н	2.80	3,93	0.110	0.155
3	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
٧	1.15	-	0.045	-
Z	-	2.04	-	0.080

MOTOROLA SEMICONDUCTOR B TECHNICAL DATA

FI FCTRICAL	CHARACTERISTICS	(TC =	25°C unless	otherwise	noted)

Char	acteris	tic				Symbol	Min	Max	Unit
FF CHARACTERISTICS						-	0.5.75 6	6 0799	
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA) IRF540, IRF542 IRF541							100 60	rien d Enha	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0, TJ = 125°C)						IDSS	IOS_ are d esigne	0.2 1	mAdc
Gate-Body Leakage Current, Forwa (VGSF = 20 Vdc, VDS = 0)							switching ac s, converter	new 100 bee of substances	
Gate-Body Leakage Current, Rever (VGSR = 20 Vdc, VDS = 0)	se					IGSSR	ching Speed	001 or Fast Swi	nAdc
N CHARACTERISTICS*	20 C31	NA TE				Specified at	On-Losses.	o Minimize	(no)801
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 0.25 mA)		0				V _{GS(th)}	Dissipation	16 Wo 4 ai Ai	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 15 Adc)	F	7		IRF54	0, IRF541 2	rDS(on)	_	0.085 0.11	Ohm
On-State Drain Current (VGS = 10 (VDS \geq 2.3 Vdc) (VDS \geq 2.6 Vdc)	V)		-	IRF54	0, IRF541 2	ID(on)	27 24	_	Adc
Forward Transconductance ($V_{DS} \ge 2.3 \text{ V, } I_D = 15 \text{ A}$) ($V_{DS} \ge 2.6 \text{ V, } I_D = 15 \text{ A}$)	3.5			IRF54	0, IRF541 2	9FS	6.0 6.0	=	mhos
YNAMIC CHARACTERISTICS									
Input Capacitance			Ciss	_	1600	AR APEN			
Output Capacitance	nu	(VD	f = 25	v, v _{GS}	lodenes	Coss	_	800	
Reverse Transfer Capacitance	2 1052	542	198	840	topinge	C _{rss}	-	300	
WITCHING CHARACTERISTICS*	Valg	1.00	0.0	001	Pagy			oltage	V aprop2-r
Turn-On Delay Time	aby:					td(on)	_	30 898	loV ns
Rise Time		(V _{DD}	≈ 30 V	, I _D =	15 Apk,	tr		60	3S = 20 M
Turn-Off Delay Time	dbV	R	gen =	4.7 Ohr	ms)	td(off)	_	80	Source V
Fall Time	dbiA.	238		e	ol l	tf	_	30	Current manuales
Total Gate Charge		15	7			Q_g	40 (Typ)	0.60 = 01	nC
Gate-Source Charge			= 0.8 10 Vdc		VDSS, Rated ID)	Qgs	17 (Typ)	_ 5-6	i = oT pla
Gate-Drain Charge	Wates	00	125		d _d	Qgd	23 (Typ)	Selbation (fil.)	Power Di
OURCE DRAIN DIODE CHARACTER	ISTICS		11 69 21		T 14	-	nacil ourseses	moT non-well	has noise
Forward On-Voltage		4	(IS = F	Rated I),	V _{SD}	1.5 (Typ)	2.3(1)	Vdc
Forward Turn-On Time	44630		VGS	= 0)		ton	Limited by s	tray inductar	nce
Reverse Recovery Time	1		62.6		RAJE	t _{rr}	450 (Typ)	anut —	ns
ITERNAL PACKAGE INDUCTANCE	30		300		JT.	,8590	loidering Purp	Temp. for S	beed mum
Internal Drain Inductance (Measured from the contact scre (Measured from the drain lead 0					of die)	L _d	3.5 (Typ) 4.5 (Typ)	e for 5 Seco Designar's Da	Hn Cas MTP25N10
Internal Source Inductance (Measured from the source lead	0.25" f	rom pa	ckage t	o sourc	ce bond pad)	L _S	7.5 (Typ)	_	

*Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%. (1) Add 0.1 V for IRF540 and IRF541.

MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

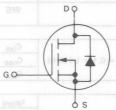
IRF610 IRF612

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive
 Loads





MAXIMUM RATINGS

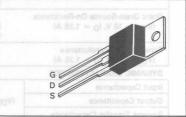
			IF		
	Rating	Symbol	610	612	Unit
Drain-Source Voltag	e	VDSS	200	200	Vdc
Drain-Gate Voltage (RGS = 1.0 M Ω)	out sins textino	VDGR	200	200	Vdc
Gate-Source Voltage		VGS	±	20	Vdc
Continuous Drain Cu	urrent T _C = 25°C	ID	2.5	2.0	Adc
Continuous Drain Cu	urrent T _C = 100°C	ID	1.5	1.25	Adc
Drain Current — Pul	sed	IDM	10	8.0	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C		PD	-	20 16	Watts W/°C
Operating and Stora	ge Temperature Range	TJ, T _{stq}	- 55	to 150	°C

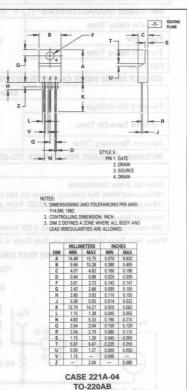
THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	R_{θ} JC R_{θ} JA	6.4 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	tuo VL Jugit	300	°C

See the MTP2N20 Designer's Data Sheet for a complete set of design curves for this product.

Part Number	VDS	rDS(on)	ID
IRF610 (0 =	200 V	1.5 Ω	2.5 A
IRF612	200 V	2.4 Ω	2.0 A





Characteristic		Symbol	Min	Тур	Max	Unit
FF CHARACTERISTICS						
rain-Source Breakdown Voltage (VGS = 0, ID = 250 μ A)		V(BR)DSS	200	_	_	Vdc
ero Gate Voltage Drain Current (V _G S = 0 V, V _D S = Rated V _{DSS}) (V _G S = 0 V, V _D S = 0.8 Rated V _{DSS} , T _C = 125°C)		IDSS	_	=	0.25	mAdc
orward Gate-Body Leakage Current (VGS = 20 V, VDS = 0)		IGSSF	_	_	100	nAdc
everse Gate-Body Leakage Current (VGS = -20 V, VDS = 0)	E SILICON CATE RANSISTOR	IGSSR	HER A	NWO9,8	- 100	nAdc
	for low voltage, high	bannisab er	ETS at	S Power	OMT se	Tine
	switching regulators		2.0	witching lenoid a	4.0	Vdc
Vn-State Drain Current (Vps = 25 V, Vgs = 10 V) IRF610 IRF612	bolir	ID(on)	2.5	for Fasi SOA⊟s P	con Gati Jgs d —	Adc
tatic Drain-Source On-Resistance (VGS = 10 V, I _D = 1.25 A) IRF610 IRF612	- eviloubal strivi esta	rDS(on)	_	_	1.5 2.4	Ohms
orward Transconductance (V _{DS} = 15 V, I _D = 1.25 A)	90	9FS	0.8		ecesses 1	mhos
YNAMIC CHARACTERISTICS	1-0		1 10	350	10007	
nput Capacitance	/1 HA	Ciss			150	pF
	$(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz})$		_		80	
everse Transfer Capacitance	(VDS = 23 V, VGS = 0, 1 = 1.0 WHZ)				25	
WITCHING CHARACTERISTICS* (T.J = 100°C)		C _{rss}	1 5	100		
urn-On Delay Time	2.4	td(on)			15	ns
	/DSS, ID = 1.25 A	t _r	_	_	25	
• 00 0.0 •	$= 50 \Omega$	td(off)	_	_	15	-
all Time		t _f	_	_	15	
SOURCE DRAIN DIODE CHARACTERISTICS*						
Characteristic			Svr	nbol	Тур	Unit
orward On-Voltage				SD	1.8	Vdc
	= Rated I _D , V _{GS} = 0)			on	Limited	by stray
Reverse Recovery Time			t	rr	290	ns
NTERNAL PACKAGE INDUCTANCE (TO-220)	VDG8 200 200				Vultage	erað-ni
DM08.1		Symbol	Min	Тур	Max	Unit
nternal Drain Inductance Measured from the contact screw on tab to center of Measured from the drain lead 0.25" from package to c		Ld	2445	3.5	Dr ein Cu	nH
nternal Source Inductance	0.8 01 sand	L _S	2/00/2	7.5	alu9 — In	rtinuous la Curra
Measured from the source lead 0.25" from package to ulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %.	81.0	FIGURE 2 — S	- t _r	3T @ 110	toff -	de blens spriden Mars

MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

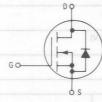
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low r_{DS(on)} to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FETS 4 and 5 AMPERES rDS(on) = 0.8 OHM 150 and 200 VOLTS

IRF620 IRF621



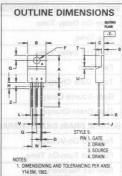


MAXIMUM RATINGS

40 ns				Combal		IRF	
	Rating			Symbol	620	621	Unit
Drain-Source Voltage				VDSS	200	150	Vdc
Drain-Gate Voltage (RGS = 20 kΩ)		110/0.		VDGR	200	150	Vdc
Gate-Source Voltage	11 (Typ)	Og .		VGS	±	20	Vdc
Drain Current Continuous, T _C = 25°C T _C = 100°C	6 (Typ)	Ogd	(g) b	I _D	o Vdc	5	Adc
Peak, T _C = 25°C						10	*aom
Total Power Dissipation @ 7 Derate above 25°C	$T_C = 25^{\circ}C$	uo _j		PD	1 3	0 32	Watts W/°C
Operating and Storage Tem	perature Rang	e		TJ, Tstg	-55	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	(sib lo Tame)	300	°C



2. CONTROLLING DIMENSION: INCH.

3. DIM 2 DEFINES A ZONE WHERE ALL BODY AND LEAD INDECTION AND THE ALL BODY AND LEAD INDECTION AND THE ALL BODY AND THE ALL BOD

	MILLIN	ETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
В	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
٧	1.15	-	0.045	_
Z	-	2.04	-	0.080

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) Characteristic Symbol Min Max Unit **OFF CHARACTERISTICS** Drain-Source Breakdown Voltage V(BR)DSS Vdc IRF620 200 $(V_{GS} = 0, I_D = 0.25 \text{ mA})$ IRF621 150 Zero Gate Voltage Drain Current mAdc IDSS 0.2 (VDS = Rated VDSS, VGS = 0) $(V_{DS} = 0.8 \text{ Rated } V_{DSS}, V_{GS} = 0, T_{J} = 125^{\circ}C)$ Gate-Body Leakage Current, Forward 100 IGSSF (VGSF = 20 Vdc, VDS = 0) Gate-Body Leakage Current, Reverse IGSSR 100 nAdc $(V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0)$ **ON CHARACTERISTICS*** Gate Threshold Voltage 2 4 Vdc VGS(th) $(V_{DS} = V_{GS}, I_{D} = 0.25 \text{ mA})$ Static Drain-Source On-Resistance rDS(on) 08 Ohm $(V_{GS} = 10 \text{ Vdc}, I_D = 2.5 \text{ Adc})$ On-State Drain Current (VGS = 10 V) 5 Adc ID(on) (VDS ≥ 4 Vdc) Forward Transconductance **gFS** 1.3 mhos $(V_{DS} \ge 4 \text{ V, I}_{D} = 2.5 \text{ A})$ DYNAMIC CHARACTERISTICS Ciss Input Capacitance 600 pF $(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ **Output Capacitance** 300 Coss f = 1 MHzReverse Transfer Capacitance Crss 80 SWITCHING CHARACTERISTICS* Turn-On Delay Time 40 td(on) ns (VDD ≈ 0.5 Rated VDSS, Rise Time tr $I_D = 2.5 \text{ Apk},$ Turn-Off Delay Time 100 td(off) $R_{gen} = 50 \text{ Ohms}$ Fall Time 60 tf **Total Gate Charge** Q_g 11 (Typ) 15 nC (VDS = 0.8 Rated VDSS, Qgs Gate-Source Charge 5 (Typ) VGS = 10 Vdc, ID = Rated ID) Gate-Drain Charge 6 (Typ) 123 \mathbf{Q}_{gd} SOURCE DRAIN DIODE CHARACTERISTICS* Forward On-Voltage 1.7 (Typ) Vdc VSD 1.8 $(I_S = Rated I_D V_{GS} = 0)$ Forward Turn-On Time Limited by stray inductance ton Reverse Recovery Time trr 300 (Typ) INTERNAL PACKAGE INDUCTANCE Internal Drain Inductance Ld nH (Measured from the contact screw on tab to center of die) 3.5 (Typ) (Measured from the drain lead 0.25" from package to center of die) 4.5 (Typ) Internal Source Inductance 7.5 (Typ) Ls (Measured from the source lead 0.25" from package to source bond pad)

^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

MOTOROLA ■ SEMICONDUCTOR **TECHNICAL DATA**

Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate TMOS

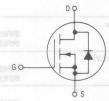
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low rDS(on) to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



IRF630 IRF631 IRF632

TMOS POWER FETS 8 and 9 AMPERES rDS(on) = 0.4 OHM 150 and 200 VOLTS rDS(on) = 0.6 OHMS 200 VOLTS





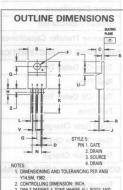
MAXIMUM RATINGS

450			0 -		IRF	SGA	11-14
Rating			Symbol	630	631	632	Unit
Drain-Source Voltage			V _{DSS}	200	150	200	Vdc
Drain-Gate Voltage (RGS = 20 kΩ)	_	(no)h ¹	V _{DGR}	200	150	200	Vdc
Gate-Source Voltage		77	VGS	e = gr	±20	- GGV	Vdc
Drain Current Continuous, $T_C = 25^{\circ}C$ $T_C = 100^{\circ}C$ Peak, $T_C = 25^{\circ}C$	(Typ)	11010- 11 00	ID		9 6 86	8 5 32	Adc
Total Power Dissipation @ T _C : Derate above 25°C	144150	pg0	PD	A = G	75 0.6	01 = 8	Watts W/°C
Operating and Storage Temper	ature Range	9	TJ, Tstg	-	55 to 1	50	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	R _θ JC R _θ JA	1.67 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	300	°C

See the MTM8N20 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTM8N20 are applicable for this series of product.



11. DIMENSIONING AND TOLERANGING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	MILLIN	TELENS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
В	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
Н	2.80	3.93	0.110	0.155
Jo	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1,39	0.045	0.055
N	4.83	5.33	0.190	0.210
0	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
٧	1.15	-	0.045	-
Z	-	2.04	-	0.080

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) Characteristic Symbol Min Max Unit OFF CHARACTERISTICS Vdc Drain-Source Breakdown Voltage V(BR)DSS 200 IRF630, IRF632 $(V_{GS} = 0, I_{D} = 0.25 \text{ mA})$ 150 IRF631 mAdc Zero Gate Voltage Drain Current IDSS $\begin{array}{lll} (V_{DS} = \mbox{Rated V}_{DSS}, \mbox{V}_{GS} = 0) \\ (V_{DS} = 0.8 \mbox{ Rated V}_{DSS}, \mbox{V}_{GS} = 0, \mbox{T}_{J} = 125 \mbox{°C}) \end{array}$ 0.2 1 Gate-Body Leakage Current, Forward 100 IGSSF nAdc (VGSF = 20 Vdc, VDS = 0) Gate-Body Leakage Current, Reverse 100 nAdc **IGSSR** (VGSR = 20 Vdc, VDS = 0) **ON CHARACTERISTICS*** Gate Threshold Voltage VGS(th) 2 4 Vdc $(V_{DS} = V_{GS}, I_{D} = 0.25 \text{ mA})$ Static Drain-Source On-Resistance Ohm rDS(on) $(V_{GS} = 10 \text{ Vdc}, I_D = 5 \text{ Adc})$ IRF630, IRF631 0.4 IRF632 0.6 On-State Drain Current (VGS = 10 V) Adc D(on) (V_{DS} ≥ 3.6 Vdc) IRF630, IRF631 9 (V_{DS} ≥ 4.8 Vdc) IRF632 8 Forward Transconductance mhos 9FS $(V_{DS} \ge 3.6 \text{ V}, I_{D} = 5 \text{ A})$ IRF630, IRF631 3 $(V_{DS} \ge 4.8 \text{ V}, I_{D} = 5 \text{ A})$ IRF632 3 **DYNAMIC CHARACTERISTICS** Input Capacitance Ciss 800 pF $(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ Output Capacitance 450 Coss f = 1 MHzReverse Transfer Capacitance Crss 150 SWITCHING CHARACTERISTICS* Turn-On Delay Time 30 td(on) Rise Time 50 tr $(V_{DD} \approx 90 \text{ V}, I_D = 5 \text{ Apk},$ $R_{gen} = 15 \text{ Ohms}$ Turn-Off Delay Time 50 td(off) Fall Time 40 tf Total Gate Charge Q_q 15 (Typ) 30 nC $(V_{DS} = 0.8 \text{ Rated } V_{DSS},$ $V_{GS} = 10 \text{ Vdc}, I_D = \text{Rated } I_D)$ Qgs Gate-Source Charge 8 (Typ) Q_{gd} Gate-Drain Charge 7 (Typ) **SOURCE DRAIN DIODE CHARACTERISTICS*** Forward On-Voltage 1.8(1) VSD 1.7 (Typ) Vdc (IS = Rated ID, Forward Turn-On Time $V_{GS} = 0$ Limited by stray inductance ton Reverse Recovery Time 325 (Typ) ns INTERNAL PACKAGE INDUCTANCE Internal Drain Inductance nH Ld (Measured from the contact screw on tab to center of die) 3.5 (Typ) (Measured from the drain lead 0.25" from package to center of die) 4.5 (Typ) Internal Source Inductance Ls (Measured from the source lead 0.25" from package to source bond pad) 7.5 (Typ)

*Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%. (1) Add 0.1 V for IRF630.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Power Field Effect Transistor N-Channel Enhancement-Mode **Silicon Gate TMOS**

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low rDS(on) to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

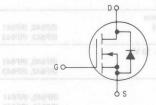


TMOS POWER FETS 16 and 18 AMPERES rDS(on) = 0.18 OHM 150 and 200 VOLTS rDS(on) = 0.22 OHMS 150 and 200 VOLTS

IRF640 IRF641

IRF642

IRF643



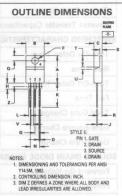


MAXIMUM RATINGS

750			0 1		IF	RF		Unit
Rating			Symbol	640	641	642	643	Unit
Drain-Source Voltage			VDSS	200	150	200	150	Vdc
Drain-Gate Voltage (R _{GS} = 20 kΩ)		(no)b ^j	V _{DGR}	200	150	200	150	Vdc
Gate-Source Voltage		INC. VE.	VGS	(acr	1/10 T±	20	18	Vdc
Drain Current Continuous, $T_C = 25^{\circ}C$ $T_C = 100^{\circ}C$ Peak, $T_C = 25^{\circ}C$	(gyT) 85	tf QQ	ID	1	8 1 2	1	6 0 64	Adc
Total Power Dissipation @ T Derate above 25°C	C = 25°C	Ogd	PD	Delsa	1:	25 1	= 89	Watts W/°C
Operating and Storage Temp	erature Range	е	TJ, Tstg		- 55	to 150		°C

THERMAL CHARACTERISTICS

TIERIVIAL CHARACTERISTICS			
Thermal Resistance — Junction to Case — Junction to Ambient	R _θ JC R _θ JA	1 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	300	°C



am	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
В	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
н	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
0	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
٧	1.15	-	0.045	-
Z	-	2.04	-	0.080

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characte	eristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS					
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	IRF640, IRF642 IRF641, IRF643	V(BR)DSS	200 150	Fjeld Enha	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0$) ($V_{DS} = 0.8\ Rated\ V_{DSS},\ V_{GS} = 0$,	T _J = 125°C)	IDSS	so	0.2	mAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		IGSSF	switching an	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)		IGSSR	_	100_	nAdc
ON CHARACTERISTICS*	ARMA I	Specified at	On-Losses.	o Minimize	i inelarii V
Gate Threshold Voltage (VDS = VGS, ID = 0.25 mA)	00	V _{GS(th)}	2 Dissipation	mpe p lure	Vdc
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 10 Adc)	IRF640, IRF641 IRF642, IRF643	rDS(on)	iaracterized _	0.18 0.22	Ohm
On-State Drain Current (VGS = 10 V) (VDS \geqslant 3.2 Vdc) (VDS \geqslant 3.5 Vdc)	IRF640, IRF641 IRF642, IRF643	lD(on)	18 16	_	Adc
Forward Transconductance ($V_{DS} \ge 3.2 \text{ V, } I_D = 10 \text{ A}$) ($V_{DS} \ge 3.5 \text{ V, } I_D = 10 \text{ A}$)	IRF640, IRF641 IRF642, IRF643	9FS	6	=	mhos
YNAMIC CHARACTERISTICS					
Input Capacitance		Ciss		1600	TAR pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	_	750	
Reverse Transfer Capacitance	640 641 642 843	C _{rss}	_	300	
WITCHING CHARACTERISTICS*	ISS 200 150 200 150 V	gV V		agari	-Source Vo
Turn-On Delay Time	GR 200 150 200 150 V	t _{d(on)}	_	30	aloV ns 2
Rise Time	$(V_{DD} \approx 75 \text{ V}, I_D = 10 \text{ Apk},$	t _r		60	3S = 50 kg
Turn-Off Delay Time	R _{gen} = 4.7 Ohms)	td(off)		80	Source Vol
Fall Time		tf		60	Current
Total Gate Charge	11 10	Q_g	38 (Typ)	60	nC
Gate-Source Charge	$(V_{DS} = 0.8 \text{ Rated } V_{DSS},$ $V_{GS} = 10 \text{ Vdc}, I_{D} = \text{Rated } I_{D})$	Qgs	16 (Typ)		is = pT at
Gate-Drain Charge	VGS = 10 Vdc, 1D = Hated 1D,	Q _{gd}	22 (Typ)	T (a) General	Power Dis
OURCE DRAIN DIODE CHARACTERIST	ICS*		anne Sanne	moT anone	2 has nales
Forward On-Voltage	(I _S = Rated I _D ,	V _{SD}	1.8 (Typ)	1.9(1)	Vdc
Forward Turn-On Time	$V_{GS} = 0$	ton	Limited by s	tray inductar	ice
Reverse Recovery Time	UC	t _{rr}	450 (Typ)	tonul—	ns
NTERNAL PACKAGE INDUCTANCE	300 °	,008	aldering Purpor	Temp, for Sc	baaJ mum
Internal Drain Inductance (Measured from the contact screw of (Measured from the drain lead 0.25)		Ld	3.5 (Typ) 4.5 (Typ)	NG588 d 101	nH
Internal Source Inductance (Measured from the source lead 0.2	5" from package to source bond pad	L _S	7.5 (Typ)	_	

*Pulse Test: Pulse Width \leq 300 μs , Duty Cycle \leq 2.0%. (1) Add 0.1 V for IRF640 and IRF641.

ID

1.5 A

rDS(on)

3.6 Ω

MOTOROLA ■ SEMICONDUCTOR TECHNICAL DATA

VDSS

400 V

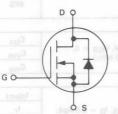
IRF710

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low rDS(on) to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





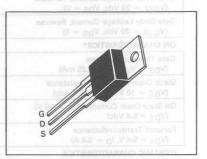
MAXIMUM RATINGS

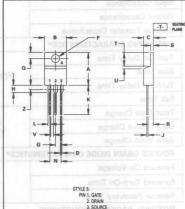
Rating	3.0 (Typ)	Symbol	Value	Unit
Drain-Source Voltage	3.0 (Typ)	V _{DSS}	400	Vdc
Drain-Gate Voltage (R _{GS} = 1.0 MΩ)		VDGR	400	Vdc
Gate-Source Voltage	(d)	VGS	± 20	Vdc
Drain Current Continuous Pulsed	(qyT) 008	IDM	1.5 6.0	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C		PD PD	20 0.16	Watts W/°C
Operating and Storage Temperature Range	7.5 (Typ)	T _J , T _{stg}	-55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	$R_{ heta JC}$ $R_{ heta JA}$	6.4 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	300	°C

Design curves of the MTP2N35 are applicable for this series of products. The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves - representing boundaries on device characteristics - are given to facilitate "worst case" design.





OTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. DIM Z DESIRES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
A	14.48	15.75	0.570	0.620	
В	9.66	10.28	0.380	0.405	
C	4.07	4.82	0.160	0.190	
D	0.64	0.88	0.025	0.035	
F	3.61	3.73	0.142	0.147	
G	2.42	2.66	0.095	0.105	
Н	2.80	3.93	0.110	0.155	
J	0.36	0.55	0.014	0.022	
K	12.70	14.27	0.500	0.562	
L	1.15	1.39	0.045	0.055	
N	4.83	5.33	0.190	0.210	
0	2.54	3.04	0.100	0.120	
R	2.04	2.79	0.080	0.110	
S	1.15	1.39	0.045	0.055	
T	5.97	6.47	0.235	0.255	
U	0.00	1.27	0.000	0.050	
٧	1.15	-	0.045	-	
Z	-	2.04	-	0.080	

CASE 221A-04 TO-220AB

OFF CHARACTERISTICS Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	Characteristic			Max	Unit
(103 0) 0120 11111		V _{(BR)DSS}	400	_	Vdc
Zero Gate Voltage Drain Current		IDSS			mAdc
$(V_{DS} = Rated V_{DSS}, V_{GS} = 0)$ $(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, 1)$	J = 125°C)	NT-MODE SIL	HAN <u>IC</u> ENIE	0.25 1.00	N-CHA
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	Sie i UM	IGSSF	EM MELLO S FET is design	500	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	egulators, con-	1 _{GSSR}	licet ia ns suc Lelay drive	500	nAdc
ON CHARACTERISTICS*		a Speeds	set Switching	Gate for Fr	• Silleon
Gate Threshold Voltage (Vps = Vgs, lp = 0.25 mA)	at Elaveted	VGS(th)	2.0	4.0	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 0.8 Adc)		rDS(on)	Power Disti	3.6	Ohm
On-State Drain Current (V _{GS} = 10 V) (V _{DS} ≥ 5.4 Vdc)	5V3GD8/R 42	I _D (on)	1.5	_	Adc
Forward Transconductance (V _{DS} ≥ 5.4 V, I _D = 0.8 A)		9FS	0.5	_	mhos
DYNAMIC CHARACTERISTICS			10000	A 400 T	N.
Input Capacitance		Ciss	1_0000	150	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Coss		50	
Reverse Transfer Capacitance	f = 1.0 MHz)	C _{rss}		15	
SWITCHING CHARACTERISTICS*		-135	1 107	B Riv	
Turn-On Delay Time		td(on)	T 1_ (2)	10	ns
Rise Time	(V _{DD} = 0.5 V _{DSS} , I _D = 0.8 A		land or	20	
Turn-Off Delay Time	$R_{\text{gen}} = 50 \text{ Ohms}$	td(off)	_	10	-
Fall Time		tf		15	
Total Gate Charge		Qq	6.0 (Typ)	7.5	nC
Gate-Source Charge	(VDS = 0.8 Rated VDSS,	0	3.0 (Typ)	Rating	
Gate-Drain Charge	$V_{GS} = 10 \text{ Vdc}, I_{D} = 2.0 \text{ A}$	Q _{ad}	3.0 (Typ)	_spat	Source Vo
SOURCE DRAIN DIODE CHARACTERIS	TICS* OBV 000	aaoV	1	99	-Gate Volta
Forward On-Voltage		V _{SD}	1.1 (Typ)	1.6	Vdc
Forward Turn-On Time	$(I_S = 2.0 \text{ A}, V_{GS} = 0)$	ton		stray inducta	NOT THE THEOD
Reverse Recovery Time	900	trr	600 (Typ)	_	ns
INTERNAL PACKAGE INDUCTANCE	0.8	wal	000 (1.)		bes
Internal Drain Inductance (Measured from the contact screw or		d ^q L _d	3.5 (Typ) 4.5 (Typ)	ipation Brc	PoHer Dis TC = 25°C ate above
(Measured from the drain lead 0.25"	0° 081 or 8	pad)	7.5 (Typ)	<u>6</u> ((810)	sting and S

MOTOROLA SEMICONDUCTOR **TECHNICAL DATA**

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

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- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS 2.5 and 3 AMPERES rDS(on) = 1.8 OHM 400 VOLTS rDS(on) = 2.5 OHM 400 VOLTS

IRF720 IRF722



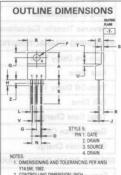
MAXIMUM RATINGS

				Vos = 0,	Symbol		Unit
		Rating		Symbo	720	722	Unit
Drain-Source Volt	age			V _{DSS}	400	400	Vdc
Drain-Gate Voltag (RGS = 1 M Ω)	е ()6		(no)b [‡]	V _{DGR}	400	400	Vdc
Drain Current Continuous Pulsed	100		(Holb)	IDW	3 12	2.5 10	Adc
Total Power Dissip	pation @ T 5°C	C = 25°C	80	PD		10 .32	Watts W/°C
Operating and Sto	rage Temp	perature Range	180	TJ, Tstg	-55	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes,	TE	300	°C
1/8" from Case for 5 Seconds			

See the MTP3N40 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.



- 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND

	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
A	14.48	15.75	0.570	0.620	
В	9.66	10,28	0.380	0.405	
C	4.07	4.82	0.160	0.190	
D	0.64	0.88	0.025	0.035	
F	3.61	3.73	0.142	0.147	
G	2.42	2.66	0.095	0.105	
Н	2.80	3.93	0.110	0.155	
J	0.36	0.55	0.014	0.022	
K	12.70	14.27	0.500	0.562	
L	1.15	1.39	0.045	0.055	
N	4.83	5.33	0.190	0.210	
Q	2.54	3.04	0.100	0.120	
R	2.04	2.79	0.080	0.110	
S	1.15	1.39	0.045	0.055	
T	5.97	6.47	0.235	0.255	
U	0.00	1.27	0.000	0.050	
٧	1.15	-	0.045	-	
Z	-	2.04	_	0.080	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

	Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Vol (VGS = 0, ID = 0.25 mA)	tage	V(BR)DSS	400	bieri	Vdc
Zero Gate Voltage Drain Cur (VDS = Rated VDSS, VGS (VDS = 0.8 Rated VDSS, V	= 0)	IDSS	_ 5(0.25	mAdc
Gate-Body Leakage Current, (VGSF = 20 Vdc, VDS = 0	and the second decision of the second	IGSSF	re de <u>sig</u> ned vitching appl	8 500 8 19W00 bs	nAdc
Gate-Body Leakage Current, (VGSR = 20 Vdc, VDS = 0)	Reverse	IGSSR	conv <u>e</u> rters,	500	nAdc
N CHARACTERISTICS*					
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 0.25 m	A)	V _{GS(th)}	2	oper Aure	Vdc
Static Drain-Source On-Resis (VGS = 10 Vdc, I _D = 1.5 A		rDS(on)	racterized for	1.8 abs	Ohm is
On-State Drain Current (VGS (VDS \geq 5.4 Vdc) (VDS \geq 6.25 Vdc)	= 10 V) IRF720 IRF722	I _{D(on)}	3 2.5	_	Adc
Forward Transconductance (VDS \geq 5.4 V, ID = 1.5 A) (VDS \geq 6.25 V, ID = 1.5 A	IRF720 IRF722	9FS	1 1	=	mhos
YNAMIC CHARACTERISTICS					
Input Capacitance		Ciss		600	pF
Output Capacitance	$(V_{DS} = 25 \text{ V, } V_{GS} = 0,$ f = 1 MHz)	Coss	- pritts	200	
Reverse Transfer Capacitano		C _{rss}	_	40	
WITCHING CHARACTERISTIC	8* 30A 00F 00F 850A			egai	n-Source Vol
Turn-On Delay Time	VOGR 400 400 VOC	td(on)		40	ns
Rise Time	$(V_{DD} \approx 200 \text{ V}, I_{D} = 1.5 \text{ Apk},$	tr	-	50	in Current
Turn-Off Delay Time	R _{gen} = 50 Ohms)	td(off)	-	100	Snormano
Fall Time	DM 12 10	tf	_	50	bealt
Total Gate Charge	SURVY OF 04	Og	12 (Typ)	15	nC
Gate-Source Charge	(V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 10 Vdc, I _D = Rated I _D)	Ogs	6 (Typ)	menaT approx	bna gnita
Gate-Drain Charge	- G3	Ogd	6 (Typ)	arroscorro.	CAMP EASE
OURCE-DRAIN DIODE CHARA	CTERISTICS*				10.00 10.00 10.00
Forward On-Voltage	(I _S = Rated I _D ,	V _{SD}	1.1 (Typ)	1.6	Vdc
Forward Turn-On Time	VGS = 0)	ton	Limite	d by stray ind	uctance
Reverse Recovery Time		t _{rr}	500 (Typ)	for <u>5. Second</u>	ns
NTERNAL PACKAGE INDUCTA	NCE feeds stab sidt no louborg ent not zernyo o	plack to me stal	ihent for a comp	esignar's Data	na MTPSNAD D
	screw on tab to center of die) ad 0.25" from package to center of die)	L _d	3.5 (Typ) 4.5 (Typ)	=	nH
Internal Source Inductance (Measured from the source le	L _S	7.5 (Typ)	_		

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

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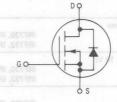


IRF733
TMOS POWER FETS
4.5 and 5.5 AMPERES

rDS(on) = 1 OHM 350 and 400 VOLTS

rDS(on) = 1.5 OHM 350 and 400 VOLTS

IRF730 IRF731





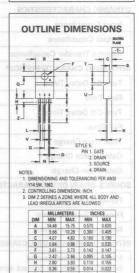
MAXIMUM RATINGS

	H191		Combal	IRF				Linia
	Rating		Symbol	730	731	732	733	Unit
Drain-Source Vo	tage		VDSS	400	350	400	350	Vdc
Drain-Gate Volta (R _{GS} = 20 kΩ			V _{DGR}	400	350	400	350	Vdc
Gate-Source Volt	age	(110	VGS		±	20		Vdc
Drain Current Continuous, To To Peak, TC = 25	c = 100°C	(tho	ID ID		.5 .5 .5	;	.5 3 8	Adc
Total Power Diss Derate above 2		30 B	PD	PSS In		5.6	SQ(V)	Watts W/°C
Operating and St	torage Temperature Range	bg	T _J , T _{stg}		- 55 1	to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance, — Junction to Case — Junction to Ambient	R _θ JC R _θ JA	1.67 62.5 = gh	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	(0 300 DV	°C

See the MTM5N35 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.



MOTOROL	A TMOS	POWER	MOSFET	DATA
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Characteristic			Min	Max	Unit
OFF CHARACTERISTICS		10044	5.5 00	11.11.11	4
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	IRF731, IRF733 IRF730, IRF732	V _(BR) DSS	350 400	-1010 En <u>h</u> and	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0, TJ = 125°C)			e des ig ned fo	0.2 0.2 Description	mAdc
Gate-Body Leakage Current, Forw (VGSF = 20 Vdc, VDS = 0)	ard	IGSSF	sectim <u>a</u> applib converters, so	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)			ing Speeds	100	nAdc
ON CHARACTERISTICS*	SOMT	30 DOI 110	data reasson in	enuberacur	w (no)sur
Gate Threshold Voltage (VDS = VGS, ID = 0.25 mA)	00	VGS(th)	ssipa 2 nulling acterized for	A is Power D	OZ Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, I _D = 3 Adc)	IRF730, IRF731 IRF732, IRF733	rDS(on)	=	1 1.5	Ohm
On-State Drain Current (V _{GS} = 10 (V _{DS} \geq 5.5 Vdc) (V _{DS} \geq 6.75 Vdc)	(PV) IRF730, IRF731 IRF732, IRF733	I _{D(on)}	5.5 4.5	Ξ	Adc
Forward Transconductance (VDS \geq 5.5 V, ID = 3 A) (VDS \geq 6.75 V, ID = 3 A)	IRF730, IRF731 IRF732, IRF733	gFS	3 3	Ξ	mhos
DYNAMIC CHARACTERISTICS				800	HAN MUI
Input Capacitance	IN U NAME OF THE PARTY OF	C _{iss}	_	800	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss		300	20
Reverse Transfer Capacitance	1 400 380 400 380 VIC	C _{rss}	_	80	DV 8910DG-
SWITCHING CHARACTERISTICS*	90 908 909 988 909 8	adv		ag	Cate Votta
Turn-On Delay Time	± 20 V/a	td(on)		30	ns
Rise Time	(V _{DD} ≈ 200 V, I _D = 3 Apk,	t _r		35	Current
Turn-Off Delay Time	R _{gen} = 15 Ohms)	td(off)	_	55	Tieseousis, T
Fall Time	8.5 8.5	tf	_	35	is a set of
Total Gate Charge		Q_g	18 (Typ)	30	nC
Gate-Source Charge	(V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 10 Vdc, I _D = Rated I _D)	Qgs	10 (Typ)	— oras	evode em
Gate-Drain Charge	1° 081 to 88 - 01	Ω_{gd}	8 (Typ)	egme T egete	B bas gait
SOURCE-DRAIN DIODE CHARACTER	IISTICS*			ACTERISTICS	AL CHAR
Forward On-Voltage	Wor tell	V _{SD}	1.2 (Typ)	1.5(1)	Vdc
Forward Turn-On Time	(I _S = Rated I _D ,	ton	Limited by st	ray inductance	
Reverse Recovery Time	V _{GS} = 0)	t _{rr}	4:20 (Typ)	remp, for Soli	ns
NTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screv (Measured from the drain lead 0.2		L _d	3.5 (Typ) 4.5 (Typ)	E state thought	nH
Internal Source Inductance (Measured from the source lead 0.	25" from package to source bond pad)	L _S	7.5 (Typ)	_	

*Pulse Test: Pulse Width \leq 300 $\mu s,$ Duty Cycle \leq 2%. (1)Add 0.1 V for IRF730 and IRF731.

ID

10 A

10 A

3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

IRF740 IRF741

VDSS

400 V

350 V

rDS(on)

0.55 Ω

0.55 Ω

Part Number

IRF740

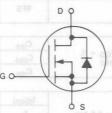
IRF741

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

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MAXIMUM RATINGS

				0	1F	RF	
	Rating	(gyT) 0S	Occur	Symbol	740	741	Unit
Drain-Source Volta	age	20 (Yep)	baO	VDSS	400	350	Vdc
Drain-Gate Voltage (RGS = 1.0 M Ω				V _{DGR}	400	350	Vdc
Gate-Source Volta		Section L	U6"	VGS	+	20	Vdc
Drain Current Continuous Pulsed		600 (Typ)	110	I _D		0	Adc
Total Power Dissip @ T _C = 25°C Derate above 25		3.5 (Typ) 4.5 (Typ)	PI	PD	1	25	Watts W/°C
Operating and Sto Temperature Ra		7.5 (Typ)	g-l	TJ, T _{stg}	- 55 t	to 150	°C

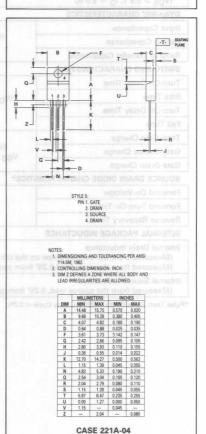
THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	R _θ JC R _θ JA	1.0 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	275	°C

See the MTP8N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTP10N35 are applicable for this series of products.

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

108*	REPRETERIES	лако ио
egs	1	Gana Th
2.25 p	C	adv)
11		Static Dri (VGS =
	5.5 Vdc)	



TO-220AB

Vos	Charac	teristic			Symbol	Min	Max	Unit
RF741 RF740 RF74	OFF CHARACTERISTICS				200			
VDS = 0.8 Rated VDSS, VGS = 0, TJ = 125°C)					V(BR)DSS		_	Vdc
Comparison Com	(VDS = Rated VDSS, VGS = 0)					IANCEMEI R FIELD 6		mAdc
VGSR = 20 Vdc, VDS = 0		TREY	oltaga, high	t high vi	IGSSF	r FETS pro	500	nAdc
Static Drain-Source On-Resistance					IGSSR	nd re la y driv	500	nAdc
Vos	ON CHARACTERISTICS*				anosto	gomeson.		2 1100 HO
VGS = 10 Vdc, ID = 5.0 Adc			0.904	M3 10 DOI	VGS(th)	2.0	4.0	Vdc
Vos 5.5 vdc Section Sectio	Static Drain-Source On-Resistance			diiW e	rDS(on)	ower Dissip ide Charach	0.55	Ohm
(V _{DS} ≥ 5.5 V, I _D = 5.0 A) DYNAMIC CHARACTERISTICS Input Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz) Coss					I _{D(on)}	10	spec" avi	Adc
Coss -				00	9FS	4.0	_	mhos
Output Capacitance	DYNAMIC CHARACTERISTICS					1000	KEL AND	
Reverse Transfer Capacitance f = 1.0 MHz) Coss Crss Tun-On Delay Time Rise Time Rise Time Furn-Off Delay Time Rigen = 4.7 Ohms) Coss Tun-Off Delay Time Rigen = 4.7 Ohms) Rigen = 4.7 Ohms Rigen = 4.	nput Capacitance		/ 1	1-1	Ciss	-	1600	pF
Crss — 150	Output Capacitance	$(V_{DS} = 2)$	$5 \text{ V, V}_{GS} = 0$),	Coss	1	450	
Turn-On Delay Time Turn-Off Delay Time Tur	Reverse Transfer Capacitance		1.0 (VIF12)			-	150	
Rise Time (VDD = 25 V, ID = 5.0 Apk, Rgen = 4.7 Ohms) (VDD = 25 V, ID = 5.0 Apk, Rgen = 4.7 Ohms) (VDD = 25 V, ID = 5.0 Apk, Rgen = 4.7 Ohms) (VDD = 25 V, ID = 5.0 Apk, Rgen = 4.7 Ohms) (VDS = 0.8 Rated VDSS, VGS = 10 Vdc, ID = Rated ID) (VDS = 0.8 Rated VDSS, VGS = 10 Vdc, ID = Rated ID) (VDS = 0.8 Rated VDSS, VGS = 10 Vdc, ID = Rated ID) (VDS = 0.8 Rated VDSS, VGS = 10 Vdc, ID = Rated ID) (VDS = 0.8 Rated VDSS, VGS = 20 (Typ) (VDS = 0.8 Rated VDSS, VGS = 20 (Typ) (VDS = 0.8 Rated ID) (VD	SWITCHING CHARACTERISTICS*		1	47		187	700 007	
Rise Time (VDD = 25 V, ID = 5.0 Apk, Rgen = 4.7 Ohms) (VDD = 25 V, ID = 5.0 Apk, Rgen = 4.7 Ohms) (VDD = 25 V, ID = 5.0 Apk, Rgen = 4.7 Ohms) (VDD = 25 V, ID = 5.0 Apk, Rgen = 4.7 Ohms) (VDS = 0.8 Rated VDSS, VGS = 10 Vdc, ID = Rated ID) (VDS = 0.8 Rated VDSS, VGS = 10 Vdc, ID = Rated ID) (VDS = 0.8 Rated VDSS, VGS = 10 Vdc, ID = Rated ID) (VDS = 0.8 Rated VDSS, VGS = 10 Vdc, ID = Rated ID) (VDS = 0.8 Rated VDSS, VGS = 20 (Typ) (VDS = 0.8 Rated VDSS, VGS = 20 (Typ) (VDS = 0.8 Rated ID) (VD	Turn-On Delay Time	L _D			td(on)	1 6	35	ns
Turn-Off Delay Time $R_{gen} = 4.7 \text{ Ohms} $ $t_{d(off)} - 90$ $t_{f} - 35$ $Total Gate Charge Gate-Source Charge Gate-Drain Charge Gate-Drain Charge R_{gen} = 4.7 \text{ Ohms} R_{gen} = 4.7 \text{ Ohms} R_{gen} = 4.7 \text{ Ohms} t_{f} - 35 Q_{g} = 40 \text{ (Typ)} = 60 Q_{gs} = 20 \text{ (Typ)} - Q_{gd} = 20 \text{ (Typ)} $	Rise Time	(Vpp = 25)	nk		_	15		
Fall Time Total Gate Charge Gate-Source Charge Gate-Drain Charge Gate-Drain Charge Gound Convert Charge (Is = Rated Ip, Vgs = 0) Vgs = 0) Vgs = 0 Vsc (Is = Rated Ip, Vgs = 0) Vgs = 0) Vgs = 0 Vsc (Is = Rated Ip, Vgs = 0) Vgs = 0) Vgs = 0 Vsc (Is = Rated Ip, Vgs = 0) Vgs = 0 Vsc (Is			pk,					
Total Gate Charge Gate-Source Charge Gate-Drain Charge Gate-Drain Charge Gate-Drain Charge Gounce Charge Gate-Drain Charge Gounce Charace (Is = Rated ID, VsD		La John Committee			_	35	AR MUMB	
Gate-Source Charge Gate-Drain Charge Gate-Drain Charge Gate-Drain Charge Gounce Drain Charge SOURCE DRAIN DIODE CHARACTERISTICS* Forward On-Voltage Forward Turn-On Time Reverse Recovery Time NTERNAL PACKAGE INDUCTANCE Internal Drain Inductance (Measured from the contact screw on the tab to center of die) (VDS = 0.8 Rated VDSS, VGS = 10 Vdc, ID = Rated ID) Qgs	Total Gate Charge		781			40 (Typ)	60	nC
Gate-Drain Charge SOURCE DRAIN DIODE CHARACTERISTICS* Forward On-Voltage Forward Turn-On Time Reverse Recovery Time NTERNAL PACKAGE INDUCTANCE Internal Drain Inductance (Measured from the contact screw on the tab to center of die) Qgd 20 (Typ) — VSD 1.1 (Typ) 2.0 Vdc ton Limited by stray inductance trr 600 (Typ) — ns Add 1.1 (Typ) 2.0 Vdc ton Limited by stray inductance trr 600 (Typ) — ns NTERNAL PACKAGE INDUCTANCE 1.2 1.3 1.4 1.5 1.7 1.7 1.7 1.7 1.7 1.7 1.7 1.7 1.7 1.7							gnlts.R	
SOURCE DRAIN DIODE CHARACTERISTICS* Forward On-Voltage Forward Turn-On Time Reverse Recovery Time NTERNAL PACKAGE INDUCTANCE Internal Drain Inductance (Measured from the contact screw on the tab to center of die) SOURCE DRAIN DIODE CHARACTERISTICS* (IS = Rated ID, VSD 1.1 (Typ) 2.0 Vdc ton Limited by stray inductance trr 600 (Typ) — ns Add Ld Add 3.5 (Typ) —		$V_{GS} = 10 \text{ Vol}$	c, ID = Rate	d ID)			_ 928	n-Source Vol
Forward On-Voltage Forward Turn-On Time Reverse Recovery Time NTERNAL PACKAGE INDUCTANCE Internal Drain Inductance (Measured from the contact screw on the tab to center of die) (Is = Rated ID, VSD		STICS*	400 350	Noov V	-gu	20 (19)	9	r-Gate Voltag
Forward Turn-On Time		7 1 1 2 2 2			Ven	1.1 (Tvn)	2.0	Vdc
Reverse Recovery Time	100 7.99			SaA			7131	DOMESTICAL
NTERNAL PACKAGE INDUCTANCE Internal Drain Inductance (Measured from the contact screw on the tab to center of die) 3.5 (Typ) 3.5 (Typ)	THUS	obA.	3 %				_	109511011
Internal Drain Inductance (Measured from the contact screw on the tab to center of die) Ld 3.5 (Typ) — Orac Orac Orac Orac Orac Orac Orac Orac Orac Orac Orac Orac Orac Orac Orac Orac Orac Orac Orac Orac			98	xeal	411	000 (1.75)		boot hour
(Measured from the drain lead 0.25" from package to center of die) 4.5 (Typ) —	(Measured from the contact screw of			69	Ld		_	PovHn Diss To = 25°C rate above 2
Internal Course Industrance		25" from package t	o source bon	d pad)	L _S	7.5 (Typ)	apero	S bas gaits
Internal Source Inductance	Reverse Recovery Time NTERNAL PACKAGE INDUCTANCE Internal Drain Inductance (Measured from the contact screw of the Measured from the drain lead 0.25" Internal Source Inductance	on the tab to cente	r of die)	G ^q	t _{rr}	3.5 (Typ) 4.5 (Typ)	pation	Dissi 25°C 30ve 2

3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

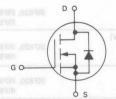
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low r_{DS(on)} to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



IRF820 IRF821 IRF823

TMOS POWER FETS 2 and 2.5 AMPERES FDS(on) = 3 OHM 450 and 500 VOLTS FDS(on) = 4 OHM 450 VOLTS





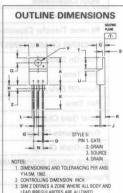
MAXIMUM RATINGS

	Rating			Symbol		SSV N IRF SQV)		
				Symbol	820 821		823	Unit
Drain-Source Volt	age	L		VDSS	500	450	450	Vdc
Drain-Gate Voltage $(R_{GS} = 1 M\Omega)$	je ₀₈	- 1	(neib [†]	V _{DGR}	500	450	450	Vdc
Gate-Source Volta	age		7	VGS	= gl	± 20	= OGV	Vdc
Drain Current Continuous Pulsed	30	12 (Tvo)	M. P.	I _D		.5	2 8	Adc
Total Power Dissi Derate above 2		c = 25°C	Oge	PD	* SaV	40 0.32	VGS =	Add
Operating and St	orage Temp	erature Range	pgD	T _J , T _{stg}		55 to 1	50	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	R _θ JC R _θ JA	3.12 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	300	°C

See the MTP3N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.



- 1	EAD IR			HERE ALL	
1	omi	MILLIN	ETERS	INC	HES
	DIM	MIN	MAX	MIN	MAX
- 1	A	14.48	15.75	0.570	0.620
4	В	9.66	10.28	0.380	0.405
1	C	4.07	4.82	0.160	0.190
1	D	0.64	0.88	0.025	0.035
1	F	3.61	3.73	0.142	0.147
1	G	2.42	2.66	0.095	0.105
1	H	2.80	3.93	0.110	0.155
1	J	0.36	0.55	0.014	0.022

K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	not V	0.045	1-11
Z	-	2.04	-	0.080

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

	Characteristic		Symbol	Min	Max	Unit
FF CHARACTERISTICS			- The A.	-325	La Land String	-
Drain-Source Breakdown (VGS = 0, ID = 0.25 m.		IRF821, IRF82 IRF820	*(DN)D33	450 500	ied <u>n</u> a l	Vdc
Zero Gate Voltage Drain C (VDS = Rated VDSS, V (VDS = 0.8 Rated VDSS	GS = 0)	°C)	IDSS dold not	es de ri gned	0.25	mAdc
Gate-Body Leakage Curre (VGSF = 20 Vdc, VDS			IGSSF	witchi <u>ng</u> app , cenverters,	500	nAdc
Gate-Body Leakage Curre (VGSR = 20 Vdc, VDS			IGSSR	hing Speeds	500	nAdc
N CHARACTERISTICS*	801	MIT	78 DSITION	de reassorium	PSUMMING O	DS(dn)
Gate Threshold Voltage (VDS = VGS, ID = 0.25	i mA)		V _G S(th)	Jissip 2 (on Li racterized for	A is Privar I	Vdc
Static Drain-Source On-Re (VGS = 10 Vdc, ID = 1		IRF820, IRF82 IRF82		_	3 4	Ohm
On-State Drain Current (V $(V_{DS} \ge 7.5 \text{ Vdc})$ $(V_{DS} \ge 8 \text{ Vdc})$	GS = 10 V)	IRF820, IRF82		2.5 2	_	Adc
Forward Transconductand (VDS \geq 7.5 V, ID = 1 A (VDS \geq 8 V, ID = 1 A)		IRF820, IRF82 IRF82		1 1	=	mhos
YNAMIC CHARACTERISTIC	S					
Input Capacitance	106				400	pF
Output Capacitance	(VDS	$f = 25 \text{ V}, \text{ V}_{GS} = 0,$ f = 1 MHz	Coss	- 0	150	
Reverse Transfer Capacita		820 821	C _{rss}		40	
WITCHING CHARACTERIST	rics*	089 500 450	V .		abeli	ov samos
Turn-On Delay Time	28V 968		^t d(on)	-	60	ns
Rise Time		\approx 200 V, I _D = 1 Apk,	t _r	_	50	Source Vo
Turn-Off Delay Time	R	gen = 50 Ohms)	[†] d(off)	-	60	Inemo3
Fall Time	2	lp 2.5	tf	-	30	attounite
Total Gate Charge	()/22	- 10 V V 0 8 w	Qg	12 (Typ)	15	nC
Gate-Source Charge		= 10 V, V_{DS} = 0.8 x V_{DSS} , I_{D} = Rated I_{D}		6 (Typ)	D1.00 upusdie	Power Dis
Gate-Drain Charge		Shelish T	Qgd	6 (Typ)	and Table	Link Hills
OURCE-DRAIN DIODE CHA	RACTERISTICS*	1 1914	0.1	- 0	Sirastato A	salin iak
orward On-Voltage	CT ST		V _{SD}		1.5(1)	Vdc
orward Turn-On Time		(I _S = Rated I _D , V _{GS} = 0)		Limited by st	ray inductance	o ot neithr
everse Recovery Time		00E 1T	t _{rr}	500 (Typ)	Termo Tor So	ns
ITERNAL PACKAGE INDU	CTANCE			8	tor S Second	from Cast
Internal Drain Inductance (Measured from the conta (Measured from the drain			nuo igiesb L _d ius eis	3.5 (Typ) 4.5 (Typ)	ssigner's Déta 5	e awan Hu
Internal Source Inductance (Measured from the source		ge to source bond pad	L _S	7.5 (Typ)	-	

^{*}Pulse Test: Pulse Width \leq 300 $\mu s,$ Duty Cycle \leq 2%. (1) Add 0.1 V for IRF820 and IRF821.

Power Field Effect Transistor

N-Channel Enhancement Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low rDS(on) to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



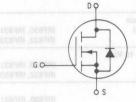


TMOS POWER FETs 4 and 4.5 AMPERES rDS(on) = 1.5 OHMS 450 and 500 VOLTS rDS(on) = 2 OHMS 450 and 500 VOLTS

IRF830 IRF831

IRF832

IRF833





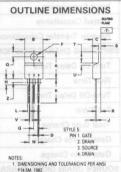
MAXIMUM RATINGS

	Ratino	-		Cumbal	IRF				Unit
	200	3		Symbol	830	831	832	833	Unit
Drain-Source Voltag	je		Cres	VDSS	500	450	500	450	Vdc
Drain-Gate Voltage (RGS = 20 kΩ)	nir .		C-161	V _{DGR}	500	450	500	450	Vdc
Gate-Source Voltag	е		100000	VGS	± 20		Vdc		
Drain Current Continuous, TC =	25°C 100°C		(86)87		4	.5	2	4	Adc
Peak, T _C = 25°C				ID	1	8	1	6	
Total Power Dissipa Derate above 25°0		$T_C = 25^{\circ}C$	180	PD			.6		Watts W/°C
Operating and Store	age Tem	perature Ran	ige land	TJ, Tstg		- 55 1	to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	R ₀ JC	1.67	°C/W
— Junction to Ambient	R _H JA	62.5	
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	300	°C

See the MTM4N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTP4N45 are applicable for this series of product.



	OLLING D	IMENSION A ZONE W		BODY A	ND
LEAD IF		RITIES ARI			,
91	MILLIA	METERS	INC	HES	1
DHM	MIN	MAX	MIN	MAX	1

	MILLIN	HETERS	INC	INCHES			
MIC	MIN	MAX	MIN	MAX			
A	14.48	15.75	0.570	0.620			
8	9.66	10.28	0.380	0.405			
C	4.07	4.82	0.160	0.190			
D	0.64	0.88	0.025	0.035			
F	3.61	3.73	0.142	0 147			
G	2.42	2.66	0.096	0.105			
Н	2.80	3.93	0.110	0.155			
J	0.36	0.55	0.014	0 022			
K	12.70	14.27	0.500	0.562			
L	1.15	1.39	0.045	0.055			
N	4.83	5.33	0.190	0.210			
0	2 54	3.04	0.100	0 120			
R	2.04	2.79	0.080	0.110			
5	1.15	1.39	0.045	0.055			
T	5.97	6.47	0.235	0.255			
U	0.00	1.27	0.000	0.050			
٧	1.15	-	0.045	1-			
Z	-	2.04	-	0.080			



Characterist	tic	Symb	ool	Min	Max	Unit
FF CHARACTERISTICS					4 4 40	
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	IRF831, IRF833 IRF830, IRF832	V(BR)D	oss	450 500	Held Enba	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS} , V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS} , V_{GS} = 0, T _J	= 125°C)	IDSS	S pid not be	OS an decim	0.2	mAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		IGSS			and p.001r a	
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)		IGSS	STATE OF THE PERSON NAMED IN COLUMN NAMED IN C	ching Spae		nAdc
N CHARACTERISTICS*	DWT	78 (Specified	On-Losses.	eximinity o	(no)eq
Gate Threshold Voltage (VDS = VGS, ID = 0.25 mA)	00	V _{GS(1}	th) of nid	2 Jacque IO	A is Potent	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, I _D = 2.5 Adc) IRF830, IRF831 IRF832, IRF833		rDS(o	on)	=	1.5 2	Ohmub
On-State Drain Current ($V_{GS} = 10 \text{ V}$) ($V_{DS} \ge 6.75 \text{ Vdc}$) ($V_{DS} \ge 8 \text{ Vdc}$) IRF830, IRF831 ($V_{DS} \ge 8 \text{ Vdc}$) IRF832, IRF833		ID(or	n)	4.5	=	Adc #
Forward Transconductance $(V_{DS} \ge 6.75 \text{ V, } I_D = 2.5 \text{ A})$ $(V_{DS} \ge 8 \text{ V, } I_D = 2.5 \text{ A})$	IRF830, IRF831 IRF832, IRF833	9FS	5	2.5 2.5	=	mhos
YNAMIC CHARACTERISTICS					Nes	WUW BAT
Input Capacitance	981	and source	Ciss	_	800	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0)$ f = 1 MHz)	Ostory Co.	Coss	_	200	
Reverse Transfer Capacitance	500 450 500 450	Vpss	C _{rss}	_	60	Source Vi
WITCHING CHARACTERISTICS*	500 450 500 450	POGV			651	-Gate Volta
Turn-On Delay Time			td(on)	_	30	ns
Rise Time (V _{DD} ≈ 200 V, I _D = 2.5 Ap			tr	_	30	Source Vd
Turn-Off Delay Time	R _{gen} = 15 Ohms)		td(off)	_	55	Cument ntinuous.
Fall Time	8 2.5		tf	_	30	
Total Gate Charge	0 10	G:	Q_g	22 (Typ)	30	nC
TAXABLE IN THE PROPERTY OF THE	(Vnc = 0.8 Rated Vncc	200		100	WHEN THE PROPERTY OF	TITLE YEAR ONLY

SOURCE	DRAIN	DIODE	CHARACTERISTICS*

Gate-Source Charge

Gate-Drain Charge

Forward On-Voltage	(IS = Rated ID,	Place	V _{SD}	1.1 (Typ)	1.5(1)	Vdc
Forward Turn-On Time V _{GS} = 0)		ALBR	ton	Limited by stray inductance		
Reverse Recovery Time	nne AUN		t _{rr}	450 (Typ)	Termo Torr	ns
TERNAL PACKAGE INDUCTANCE				abn	for 5 Seco	from Case
Internal Drain Inductance (Measured from the contact screw of (Measured from the drain lead 0.25°		al design product	to autos of	3.5 (Typ) 4.5 (Typ)	nsigner's Par MTP4MS an	O daynHTM erb to seven
Internal Source Inductance			Lo	7.5 (Tvp)	_	

 $(V_{DS} = 0.8 \text{ Rated } V_{DSS}, V_{GS} = 10 \text{ Vdc}, I_D = \text{Rated } I_D)$

 Q_{gs}

 Q_{gd}

12 (Typ)

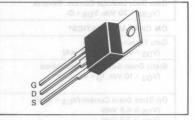
10 (Typ)

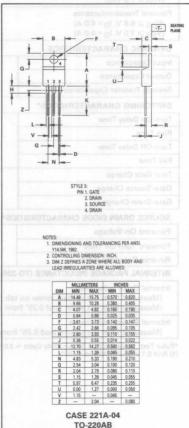
(Measured from the source lead 0.25" from package to source bond pad)

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%. (1) Add 0.1 V for IRF830 and IRF831.

IRF840 IRF841 IRF842 IRF843

Part Number	VDSS	rDS(on)	ID
IRF840	500 V	0.85 Ω	8.0 A
IRF841	450 V	0.85 Ω	8.0 A
IRF842	500 V	1.10 Ω	7.0 A
IRF843	450 V	1.10 Ω	7.0 A



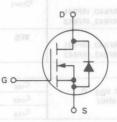


N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low r_{DS(on)} to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MAYIMLIM BATINGS

MAXIMUM RATINGS	-	[730]	bī l					
B. C. Bi	0	IRF Sha O A = ol A				Unit		
Rating	Symbol	840	841	842	843	Unit		
Drain-Source Voltage	V _{DSS}	500	450	500	450	Vdc		
Drain-Gate Voltage $(R_{GS} = 1.0 \text{ m}\Omega)$	V _{DGR}	500	450	500	450	Vdc Vdc		
Gate-Source Voltage	VGS	±20		11	Vdc			
Drain Current Continuous Pulsed	I _D	8.0 32					Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	(qyT) 608	334		125			(0 = 2	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 150		10	°C			

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	R _θ JC R _θ JA	1.0 aq brood o	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	TL	275	°C

See the MTP8N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Characteris	tic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage		V(BR)DSS			Vdc
(V _{GS} = 0, I _D = 0.25 mA)	IRF841, IRF843 IRF840, IRF842		450 500	_	
48 0 000 0 000 0 000 0 000 0 0 0 0 0 0 0	INF040, INF042	BOOM TY	300	WHELEN	mAdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0)		DSS	ER FIELD I	1600 350 150 150 1600 350 150 150 150 150	mAdc
(V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 0, T _J = 125	°C)	of benoised for	ers attal are	1.00	Thesa
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	witching regulators.	I GSSF	ig ap pl icatio ind relay dr		nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	Sectional 2 to hei	IGSSR	it Switching	500	nAdc
ON CHARACTERISTICS*	302030 14 00	A CONTRACTOR		ereture	
Gate Threshold Voltage		VGS(th)	2.0	4.0	Vdc
$(V_{DS} = V_{GS}, I_D = 0.25 \text{ mA})$	driff/ s	at I set begge	ode Charaet	d electron	Source
Static Drain-Source On-Resistance		rDS(on)		tive Loads	Ohm
(V _{GS} = 10 Vdc, I _D = 4.0 Adc)	IRF840, IRF841 IRF842, IRF843				
On-State Drain Current (VGS = 10 V)	111 0-2, 111 0-3	In		1.0	Adc
$(V_{DS} \ge 6.8 \text{ Vdc})$	IRF840, IRF841	ID(on)	8.0		Auc
(V _{DS} ≥ 7.0 Vdc)	IRF842, IRF843		7.0	is. 7,782	local I
Forward Transconductance		9FS	76.71		mhos
$(V_{DS} \ge 6.8 \text{ V}, I_D = 4.0 \text{ A})$ $(V_{DS} \ge 7.0 \text{ V}, I_D = 4.0 \text{ A})$	IRF840, IRF841 IRF842, IRF843	1	4.0		
DYNAMIC CHARACTERISTICS					
Input Capacitance	1 1	C. 90	- 107	1600	pF
	(V _{DS} = 25 V, V _{GS} = 0,	Ciss	- E	11100 5 Tet	pr
Output Capacitance	f = 1.0 MHz)	Coss	65		
Reverse Transfer Capacitance	9.9	C _{rss}		150	
SWITCHING CHARACTERISTICS*		T		9-1	Lakers
Turn-On Delay Time		td(on)			ns
Rise Time	$(V_{DD} \approx 200 \text{ V}, I_D = 4.0 \text{ Apk},$	t _r	lo-dray2	10	Ratter
Turn-Off Delay Time	R _{gen} = 4.7 Ohms)	td(off)	-		
Fall Time	. 500 450 Vae .	16 tf 008	seav		Source Ve
Total Gate Charge	(V _{GS} = 10 V, V _{DS} = 0.8 ×	Q_g	40 (Typ)	60	ofoV nC
Gate-Source Charge	Rated V _{DSS} , I _D = Rated I _D)	Qgs	20 (Typ)	- 11	m 0.1 = 8
Gate-Drain Charge	±20 Vdc	Qgd	20 (Typ)	_ a5e	Source Vol
SOURCE DRAIN DIODE CHARACTERISTIC	S*	0.0			Current
Forward On-Voltage	(I _S = Rated I _D ,	V _{SD}	Mol	1.9 (1)	Vdc
Forward Turn-On Time	VGS = 0)	ton	Limited by	stray inducta	ance
Reverse Recovery Time	125 Watts	trr	600 (Typ)	-	ns
INTERNAL PACKAGE INDUCTANCE (TO-2	20)				A SAOCTO BIL
Internal Drain Inductance (Measured from the contact screw on ta		L _d	3.5 (Typ)	_	Hn H
(Measured from the drain lead 0.25" fro	in package to center of die)		4.5 (Typ)	ours - JAN	
Internal Source Inductance (Measured from the source lead 0.25" fr	om package to source bond pad)	L _S	7.5 (Typ)	- 601 56	al Resista ation to Ca
Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤			ALGR	troidi	nA or noise
1) Add 0.1 V for IRF840 and IRF841.					

Advance Information

Small-Signal TMOS Field Effect Transistor N-Channel Enhancement-Mode

N-Channel Enhancement-Mode Silicon Gate TMOS 4-Pin DIP

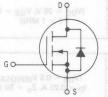
These TMOS FETs are designed for low voltage, high speed switching applications which require very low on-state resistance, high transconductance, and high device ruggedness.

- · Silicon Gate for Fast Switching Speeds
- Low Drive Current
- Package Designed for Auto Insertation
- Ease of Paralleling
- No Second Breakdown
- Stable Over Wide Temperature Range
- Rugged SOA is Power Dissipation Limited

IRFD1Z0 IRFD1Z3









CASE 370-01

MAXIMUM RATINGS

Rating			Symbol	IRFD1Z0	IRFD1Z3	Unit
Drain-Source Voltage	8	8310	V _{DSS}	100	60	Vdc
Drain-Gate Voltage (R _{GS} = 20 kΩ)	Mál	0210	VDGR	100	60	Vdc
Gate-Source Voltage		0123	VGS	± 20		Vdc
Drain Current Continuous T _C = 25°C Pulsed		(6) -	I _D	0.5	0.4 3.2	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	ls e	MOTEVIENE	PD	KS = SISYS VIDE	1	Watts mW/°C
Operating and Storage Temperature Ran	ge		T _J , T _{stg}	- 55 1	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance	R _θ JA	120	°C/W
Junction to Ambient (Free Air Operation)	IOARIU2 II		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	A 4 460 L (2042)	Symbol	Min	Тур	Max	Unit
FF CHARACTERISTICS	TERISTICS De Breakdown Voltage IRFD1Z0 V(BR)DSS 100 — — D, ID = 250 μA) IRFD1Z3 60 — — Voltage Drain Current (VDSS = Rated VDSS, VGS = 0 V) IDSS — 250 Leakage Current, Foward (VGSF = 20 V) IGSSF — 500		-0-1			
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 250 μA)	THE RESIDENCE OF THE PARTY OF T	V _{(BR)DSS}		_	1=1	Vdc
Zero Gate Voltage Drain Current (V _{DSS} = Rated	V _{DSS} , V _{GS} = 0 V)	IDSS	- 1	130	250	μAdc
Gate-Body Leakage Current, Foward ($V_{GSF} = 20$	V)012 3280	IGSSF	-	_	500	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20$) V)	IGSSR	10		500	nAdc

(continued)

ELECTRICA	L CHARACTERISTICS	- Continued (Tc =	25°C unless	otherwise noted)
------------------	-------------------	-------------------	-------------	------------------

Characteristic		Symbol	Min	Тур	Max	Unit
ON CHARACTERISTICS						
Gate Threshold Voltage (ID = 250 μ A, VDS = VGS)		V _{GS(th)}	notie	m <u>l</u> o,	nl ⁴ 93	Vdc
Static Drain-Source On-Resistance ⁽¹⁾ (V _{GS} = 10 Vdc, I _D = 0.25 A)	IRFD1Z0 IRFD1Z3	rDS(on)	DINT	len	2.4 3.2	Ohms
On-State Drain Current ⁽¹⁾ (V _{GS} = 10 V, V _{DS} = 5 V)	IRFD1Z0 IRFD1Z3	ID(on)	0.5 0.4	ot 1 hand	Effe naHen	Adc
Forward Transconductance ⁽¹⁾ (I _D = 0.25 A, V _{DS} = 5 V)		9fs.	0.25	BONN	on:D	mhos
APACITANCE A SECOND SEC		andtho w	of tel ker	onionis ov	e eTGG G	OMET ON

Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0$ f = 1 MHz)	Ciss	s w <u>hi</u> lch re	ppli <u>cation</u>	70	pF
Output Capacitance		Coss	- DUNIOUS	dir rigini i	30	r soive
Reverse Transfer Capacitance		C _{rss}	Speds	Swittenine	10	test nor

SWITCHING CHARACTERISTICS

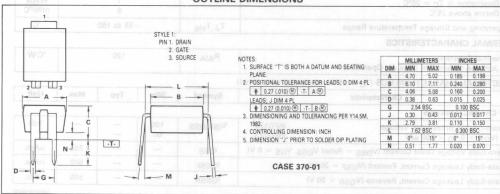
Turn-On Delay Time	1	td(on)	nou <u>a</u> stass	II OZUA N	20	ns
Rise Time	$(V_{DS} \approx 0.5 \text{ V(BR)DSS}$ $I_{D} = 0.25 \text{ A, } Z_{O} = 50 \Omega)$	t _r	_	- 038	25	Second
Turn-Off Delay Time		td(off)	te Range	uls <u>a</u> qm	25	svO std
Fall Time	The second of th	tf	na nousque	sin iawo	20	- pegg

SOURCE-DRAIN DIODE CHARACTERISTICS

Diode Forward Voltage (V _{GS} =)	0)(1)	I _S = 0.5 A, IRFD1Z0 I _S = 0.4 A, IRFD1Z3	VF		_	1.3	Vdc
Continuous Source Current, Bod	y Diode	IRFD1Z0 IRFD1Z3	IS			0.5 0.4	Adc
Pulsed Source Current, Body Diode		IRFD1Z0	ISM	_	18:14 (R _G = 20 kg) 4:sil	208) 42810	V areA-nie
±20 Vdc		IRFD1Z3		_	_	3.2	te-Snurce
Forward Turn-On Time	//-	(I _S = Rated I _S , V _{GS} = 0)			negligible	е	ns
Reverse Recovery Time	II IIS			_	100	To_ 25°C	Continuou

(1)Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

OUTLINE DIMENSIONS



Advance Information

Small-Signal TMOS Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate TMOS 4-Pin DIP

These TMOS FETs are designed for low voltage, high speed power switching applications which require very low on-state resistance, high transconductance, and high device ruggedness.

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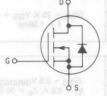
IRFD110 IRFD113



1 WATT
TMOS FETs

rDS(on) = 0.8 OHM
60 VOLTS

rDS(on) = 0.6 OHM
100 VOLTS





CASE 370-01

MAXIMUM RATINGS

S Ratin	ig —		Forns	Symbol	IRFD110	IRFD113	Unit
Drain-Source Voltage		el	FD110	V _{DSS}	eb100 yoo8	Source00 arrent	Vdc
Drain-Gate Voltage (RGS = 20 k Ω)			-D113	VDGR	100	60	Vdc
Gate-Source Voltage	_	MSI	50110F	VGS	epoi0_	20	Vdc
Drain Current Continuous T _C = 25°C		noi	(0 =	Deten	al) 1	0.8	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C		SNO	DIMENSI	PD BMLTUO	s, Duty Cycle < 25		Watts mW/°C
Operating and Storage Temperature	Range			T _J , T _{stq}	- 55	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance	(3570.)	WILLIMETERS MICHES	$R_{\theta JA}$	120	°C/W
Junction to Ambient			30000 5		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS	S10.6 BAO 00.0 L					A
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 250 μA)	IRFD110 IRFD113	V(BR)DSS	100 60	=	5=1	Vdc
Zero Gate Voltage Drain Current (VDSS = Rated	V_{DSS} , $V_{GS} = 0 V$)	IDSS	- 1	THE	250	μAdc
Gate-Body Leakage Current, Foward ($V_{GSF} = 20$) V)	IGSSF	- 1	-	500	nAdc
Gate-Body Leakage Current, Reverse (VGSR = -	- 20 V)	IGSSR		_	- 500	nAdc

(continued)



ELECTRICAL CHARACTERISTICS — Continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Тур	Max	Unit			
ON CHARACTERISTICS									
Gate Threshold Voltage (I _D = 250 μA, V _{DS} = V _{GS})		VGS(th)	2	ITTIO	4 3	Vdc			
Static Drain-Source On-Resistance ⁽¹⁾ (VGS = 10 Vdc, I _D = 0.8 A)	IRFD110 IRFD113	rDS(on)	PEND B	redit	0.6	Ohms			
On-State Drain Current ⁽¹⁾ (V _{GS} = 10 V, V _{DS} = 5 V)	IRFD110 IRFD113	I _{D(on)}	1 0.8	oneri Deneri	nB-los	Adc			
Forward Transconductance ⁽¹⁾ (I _D = 0.8 A, V _{DS} = 5 V)		9fs	0.8	ningh on	THE SE	mhos			
APACITANCE		on doiding	conitrollar	tchion at	has your	n beens			

Input Capacitance	0.0	Ciss	nce_high	te resiste	200	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0)$ f = 1 MHz)	Coss	aeemb	aggut agn	100	Mance, and
Reverse Transfer Capacitance		C _{rss}	erpado (HIIIIIIVY	25	Part Drive

SWITCHING CHARACTERISTICS

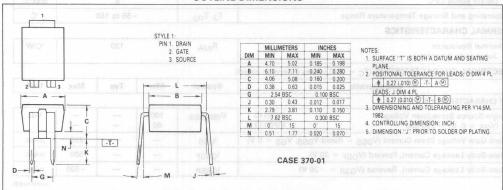
Turn-On Delay Time	1	td(on)	_	_	20	ns
Rise Time	(V _{DS} ≈ 0.5 V _{(BR)DSS}	t _r	e Range	utsiagma	25	evO eldeti
Turn-Off Delay Time	$I_D = 0.8 \text{ A}, Z_O = 50 \Omega$	td(off)	J n ait aqi	owe r Dist	9 8 2508	baggul
Fall Time 10.05E 38A0		tf	_	_	20	

SOURCE-DRAIN DIODE CHARACTERISTICS

Diode Forward Voltage (VGS = 0	orrotte	I _S = 1 A, IRFD110 I _S = 0.8 A, IRFD113	VF	— pniz	B B	2.5	Vdc
Continuous Source Current, Bod	y Diode	IRFD110 IRFD113	IS	=	- 20 loc	0.8	Adc
Pulsed Source Current, Body Dio	de	IRFD110 IRFD113	ISM		=	8 6.4	Α
Forward Turn-On Time	/le	(I - D-t1 V 0)			negligible	as = -Ta	ns
Reverse Recovery Time	(IS = Rated IS, VGS = 0)		t _{rr}		100		Pulsed

(1)Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

OUTLINE DIMENSIONS



Advance Information

Small-Signal TMOS Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate TMOS 4-Pin DIP

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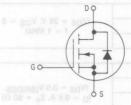
IRFD120 IRFD121 IRFD122 IRFD123



1 WATT
TMOS FETs

rDS(on) = 0.3 OHM
100 VOLTS

rDS(on) = 0.4 OHM
60 VOLTS





CASE 370-01

MAXIMUM RATINGS

Ratio	ng			Symbol	IRFD120	IRFD121	IRFD122	IRFD123	Unit
Drain-Source Voltage		430	FD123	VDSS	A 100	60	100	60	Vdc
Drain-Gate Voltage (RGS = 20 k Ω)	_	el el	15103	VDGR	100	60	100	60	Vdc
Gate-Source Voltage	-		FD123	VGS	± 20			Vdc	
Drain Current Continuous T _C = 25°C	-	MSI	FD121 FD128	ID		sbolG y	urrent, Bod 1	Source C.	Adc
Pulsed sidipilpan		nol		IDM	5	.2	amii 4	4)-muT by	Former.
Total Power Dissipation (a T _C = 25°C				PD	Nu = Sn		1		Watts
Derate above 25°C					18 A 29h	is, Duty Oye	8		mW/°C
Operating and Storage Temperature Range				TJ, Tstg		- 55 to	0 + 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance	$R_{\theta JA}$	120	°C/W
Junction to Ambient	SEPTEMBER 1		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Тур	Max	Unit
FF CHARACTERISTICS	329 00 0 309 823	0			T Tan	1
Drain-Source Breakdown Voltage (VGS = 0, ID = 250 μ A)	IRFD120, IRFD122 IRFD121, IRFD123	V(BR)DSS	100 60	<u></u>		Vdc
Zero Gate Voltage Drain Current (VDSS = Ra	ated V _{DSS} , V _{GS} = 0 V)	IDSS	_	0 -	250	μAdo
Gate-Body Leakage Current, Foward (VGSF = 20 V)		IGSSF	_	_	500	nAdc
Gate-Body Leakage Current, Reverse (VGSR	= -20 V)	IGSSR	_	_	- 500	nAdc

(continued)

ELECTRICAL CHARACTERISTICS — Continued (T_C = 25°C unless otherwise noted)

Characterist	tic	Symbol	Min	Тур	Max	Unit
IN CHARACTERISTICS					-1	
Gate Threshold Voltage (ID = 250 μ A, VDS = VGS)		V _{GS(th)}	2	No est	4	Vdc
Static Drain-Source On-Resistance ⁽¹⁾ $(V_{GS} = 10 \text{ Vdc}, I_D = 0.6 \text{ A})$	IRFD120, IRFD121 IRFD122, IRFD123	rDS(on)	n <u>5</u> 1	[Eac	0.3 0.4	Ohms
On-State Drain Current(1) (V _{GS} = 10 V, V _{DS} = 5 V)	IRFD120, IRFD121 IRFD122, IRFD123	ID(on)	1.3	onadi O <u>w</u> IT	nel Er G <u>e</u> te	Adc
Forward Transconductance ⁽¹⁾ (I _D = 0.6 A, V _{DS} = 5 V)	2007	9fs 9fs	0.9	e designe	IS FETs an	mhos
APACITANCE		anductance	gh transco	stance, hi	state resi	no wel
Innut Considerate	0.0	C.		dnage	600	Joh dei

600	eb pFid t
400	Silicon Ga
100	low urive lackage D
	estates at onitetian

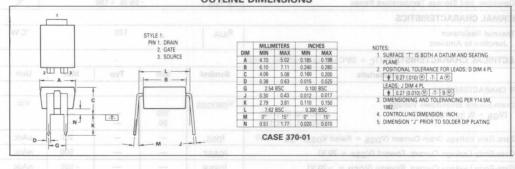
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	L	td(on)	news C. a.	IWI	40	ns
Rise Time	(V _{DS} ≈ 0.5 V _{(BR)DSS} ,	trhatim	il nottegi	aid Towo!	70	- begged
Turn-Off Delay Time	$I_D = 0.6 \text{ A, } Z_O = 50 \Omega$	td(off)	_	_	100	
Fall Time		tf	_	_	70	

SOURCE-DRAIN DIODE CHARACTERISTICS

Reverse Recovery Time	is - nated is, vgs = 0)	t _{rr}	_	280	_	newo? Is
Forward Turn-On Time	(Is = Rated Is, VGS = 0)	ton		negligible		ns
Pulsed Source Current, Body Diode IRFD120, IRFD121 IRFD122, IRFD123		ISM	=	= 5	5.2 4.4	Aurent onlinuo
obV OS #	IRFD122, IRFD123	IS		-	1.1	ponuo2-e
Cantinuous Source Current Rody	ntinuous Source Current, Body Diode IRFD120, IRFD121			c = 20 kg	1.3	Adc
Diode Forward Voltage (VGS = 0	iode Forward Voltage ($V_{GS}=0$) $I_{S}=1.3$ A, IRFD120, IRFD121 $I_{S}=1.1$ A, IRFD122, IRFD123				2.5 2.3	Vdc

(1)Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

OUTLINE DIMENSIONS



Advance Information

Small-Signal TMOS Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate TMOS 4-Pin DIP

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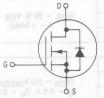
IRFD210 IRFD211 IRFD212 IRFD213



1 WATT
TMOS FETs

rDS(on) = 1.5 OHM
200 VOLTS

rDS(on) = 2.4 OHM
150 VOLTS





CASE 370

MAXIMUM RATINGS

Sov Rating		Symbol	IRFD210	IRFD211	IRFD212	IRFD213	Unit
Drain-Source Voltage		VDSS	200	150	200	150	Vdc
Drain-Gate Voltage (R _{GS} = 20 kΩ)	el le	VDGR	200	150	200	150	Vdc
Gate-Source Voltage		VGS	± 20			and accused	Vdc
Drain Current Continuous T _C = 25°C Pulsed	(mg)	I _D	0	.6 0.45 .5 1.8		45 .8 10-muT	Adc
Total Power Dissipation (a T _C = 25°C Derate above 25°C	m ^j	PD	Pacovery Time 1 and 1 an		Watts mW/°C		
Operating and Storage Temperature Range	enoiei	T _J , T _{sta}	345	- 55 t	-55 to +150		°C

THERMAL CHARACTERISTICS

Thermal Resistance	R_{θ} JA	120	°C/W
Junction to Ambient	20 20 20 20 20 20 20 20 20 20 20 20 20 2		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	2000 - 2000 This 1	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS	198 (PRO 20 1	20 1	M. T	R	1 100		
Drain-Source Breakdown Voltage	200,000	V(BR)DSS			1774	Vdc	
$(V_{GS} = 0, I_D = 250 \mu A)$	IRFD120, IRFD122 IRFD121, IRFD123	20 8	200 150	_	1 1		
Zero Gate Voltage Drain Current ($V_{DSS} = R$	ated V _{DSS} , V _{GS} = 0 V)	IDSS	u u		250	μAdo	
Gate-Body Leakage Current, Foward (VGSF	= 20 V)	IGSSF	_		500	nAdc	
Gate-Body Leakage Current, Reverse (VGSR	= -20 V)	IGSSR	_	_	-500	nAdc	

(continued)

ELECTRICAL CHARACTERISTICS — **Continued** (T_C = 25°C unless otherwise noted)

Characte	eristic	Symbol	Min	Тур	Max	Unit
ON CHARACTERISTICS						
Gate Threshold Voltage (ID = 250 μ A, VDS = VGS)		V _{GS(th)}	2	STATIO	1114 9	Vdc
$ \begin{array}{ll} \text{Static Drain-Source On-Resistance} \text{(1)} \\ \text{(VGS} = 10 \text{ Vdc, I}_{D} = 0.3 \text{ A)} & \text{IRFD210, IRFD211} \\ & \text{IRFD212, IRFD213} \end{array} $		rDS(on)	21 <u>1</u> 81	Tak	1.5 2.4	Ohms
On-State Drain Current ⁽¹⁾ (VGS = 10 V, VDS = 5 V) IRFD210, IRFD211 IRFD212, IRFD213		ID(on)	1.5 2.4	MOS.	in∃ is Tetsi	Adc
Forward Transconductance ⁽¹⁾ $(I_D = 0.3 \text{ A, } V_{DS} = 5 \text{ V})$		9fs dpid.egs	0.5 lov wol to	bengisel	FETS are s	mhos
CAPACITANCE	BUNT	amper r	ans which	applican	ewitching	s tawou
Input Capacitance	90	C _{iss}		380	150	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0)$ f = 1 MHz)	Coss	aboag2	witching		on Gate
Reverse Transfer Capacitance		C _{rss}				Drive Cu
SWITCHING CHARACTERISTICS	1		HOM	pani oron		ege uest
Turn-On Delay Time	00	td(on)	_		wo 15	hns
Rise Time	$(V_{DS} \approx 0.5 V_{(BR)DSS})$	t _r	Range	per <u>ap</u> ure	25	te Over 1
Turn-Off Delay Time	$I_D = 0.3 \text{ A}, Z_O = 50 \Omega)$	^t d(off)	-	digero en	15	Dog Dog
Fall Time		tf	_	_	15	
SOURCE-DRAIN DIODE CHARACTER	STICS					
Diode Forward Voltage (VGS = 0)	I _S = 0.6 A, IRFD210, IRFD211 S = 0.45 A, IRFD212, IRFD213	V _{SD}	_	mite <u>ll</u>	2 1.8	Vdc
Continuous Source Current, Body Diode IRFD210, IRFD211 IRFD212, IRFD213		IS	=	207001	0.6 0.45	Adc
Pulsed Source Current, Body Diode	IRFD210, IRFD211 IRFD212, IRFD213	ISM	=	=	2.5 1.8	A

(1)Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

Forward Turn-On Time

Reverse Recovery Time

OUTLINE DIMENSIONS

(IS = Rated IS, VGS = 0)

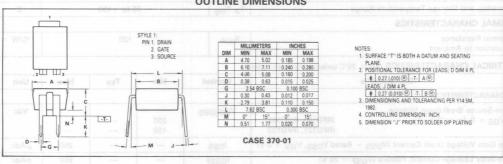
ton

trr

negligible

290

ns



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Advance Information

Small-Signal TMOS Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate TMOS 4-Pin DIP

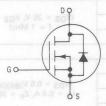
These TMOS FETs are designed for low voltage, high speed power switching applications which require very low on-state resistance, high transconductance, and high device ruggedness.

- Silicon Gate for Fast Switching Speeds
- Low Drive Current
- Package Designed for Auto Insertion
- Ease of Paralleling
- No Second Breakdown
- Stable Over Wide Temperature Range
- Rugged SOA is Power Dissipation Limited

IRFD220 IRFD221 IRFD222 IRFD223



1 WATT TMOS FETS "DS(on) = 0.8 OHM 200 VOLTS "DS(on) = 1.2 OHM 150 VOLTS





MAXIMUM RATINGS

Rating _		Symbol	IRFD220	IRFD221	IRFD222	IRFD223	Unit
Drain-Source Voltage		VDSS	200	150	200	150	Vdc
Drain-Gate Voltage (R _{GS} = 20 kΩ)	8	VDGR	200	150	200	150	Vdc
Gate-Source Voltage		VGS	1201	aboli i	20	wet westung	Vdc
Drain Current Continuous T _C = 25°C Pulsed	no ¹	ID IDM	0	.8	0	.7 .6 O-muT t	Adc
Total Power	. 33	PD			Time	VievoceR	1504051
Dissipation (α T _C = 25°C Derate above 25°C		CHARLE CHARLE	.850		1 008		Watts mW/°C
Operating and Storage Temperature Range	9	T _J , T _{stg}		- 55 to	+ 150		°C

THERMAL CHARACTERISTICS

		C1 61612	
Thermal Resistance	R _θ JA	120	°C/W
Junction to Ambient	289 899 - 800		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	2001 2000 000 1 800	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS	1/20 5/05 \$47 00.0		4	H	1 100	7)
Drain-Source Breakdown Voltage (VGS = 0, ID = 250 μ A)	IRFD220, IRFD222 IRFD221, IRFD223	V(BR)DSS	200 150	-00		Vdc
Zero Gate Voltage Drain Current (VDSS =	Rated V _{DSS} , V _{GS} = 0 V)	IDSS	-1- N-		250	μAdc
Gate-Body Leakage Current, Foward (V_{GS}	F = 20 V)	IGSSF	-		500	nAdc
Gate-Body Leakage Current, Reverse (VGS	R = -20 V	IGSSR	_	_	-500	nAdc

(continued)

ELECTRICAL CHARACTERISTICS — Continued (T_C = 25°C unless otherwise noted)

Charac	Symbol	Min	Тур	Max	Unit	
ON CHARACTERISTICS						
Gate Threshold Voltage (I _D = 250 μA, V _{DS} = V _{GS})	VGS(th)	2	BWHO.	490	Vdc	
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 0.4 A)	(1) IRFD220, IRFD221 IRFD222, IRFD223	rDS(on)	JEVE E BOHST	nai cf Ti	0.8 1.2	Ohms
On-State Drain Current ⁽¹⁾ $(V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V})$ $IRFD220, IRFD221$ $IRFD222, IRFD223$		ID(on)	0.8 0.7	hance NAOS	nB_En Sa t e	Adc
Forward Transconductance ⁽¹⁾ (I _D = 0.4 A, V _{DS} = 5 V)	9fs dgid spst	0.5	designed	ma eT33 are	mhos	
APACITANCE (no) 201	EDMT	эпирэт п	ons which	application	awitching	15vvoq
Input Capacitance	0.0	Ciss	HOUSTIGHT)	ness.	600	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0)$ f = 1 MHz)	Coss	Speeds	Svei re ning	300	con Gate
Reverse Transfer Capacitance		C _{rss}	_		80	1
WITCHING CHARACTERISTICS	+		nous	Baul Ours		Rage Dec
Turn-On Delay Time	1 00	td(on)	_	— n	vob 40 18	onons 8
Rise Time	$(V_{DS} \approx 0.5 V_{(BR)DSS})$	tr	Range	nul <u>er</u> equ	60	avO sld
Turn-Off Delay Time	$_{\rm e}I_{\rm D}=0.4~{\rm A},~{\rm Z}_{\rm O}=50~{\rm \Omega})$	td(off)	tita notre	diseid isw	100	ged
Fall Time		tf	_	_	60	
OURCE-DRAIN DIODE CHARACTE	RISTICS					
Diode Forward Voltage (V _{GS} = 0	V _{SD}	- = -	Parting—	1.8	Vdc	
Continuous Source Current, Body Diode IRFD220, IRFD221 IRFD222, IRFD223		Is	=	$=2\overline{0}(\Omega)$	0.8 0.7	Adc
Pulsed Source Current, Body Diode IRFD220, IRFD221 IRFD222, IRFD223		ISM	=	=	6.4 5.6	A
Forward Turn-On Time	(la - Reted la Vala 0)	ton		negligible	Jer - 31	ns
Reverse Recovery Time	(I _S = Rated I _S , V _{GS} = 0)	ter	_	150	_	

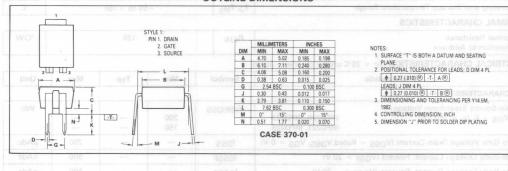
(1)Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

Reverse Recovery Time

OUTLINE DIMENSIONS

trr

150



Advance Information

Small-Signal Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

... designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid, relay drivers, inverters, choppers, audio amplifiers, and high energy pulse circuits.

- Silicon Gate for Fast Switching Speeds
- Low Drive Current Required
- Easy Paralleling
- No Second Breakdown
- Excellent Temperature Stability

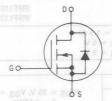


N-CHANNEL
TMOS POWER FETS

rDS(on) = 0.6 OHM
100 VOLTS

rDS(on) = 0.8 OHM
60 VOLTS

3





MAXIMUM RATINGS

		Rating		ed Voss.	Symbol	IRFF110	IRFF113	Unit
Drain-Source Volta	age		The control	,A	VDSS	100	60	Vdc
Drain-Gate Voltage	e (RGS = 1 m	ηΩ)	12	1911111	VDGR	100	60	Vdc
Gate-Source Volta	ige				VGS	#ACTERISTIC	20 3000 144	Vdc
Drain Current Continuous	2.5	_	gsV		or rangi _D	3.5	anettoV-r	Adc
Pulsed					IDM	14	12	
Total Power Dissip Derate above 25		= 25°C	no!	(na)GF	PD all		5 12 miT ylevos	Watts W/°C
Operating and Sto	orage Tempera	ature Range			TJ, T _{stq}	- 55	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JA}$	8.33 175	°C/W
Maximum Lead Temperature 1.6 mm from Case for 10 s	TL	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS	4 N				
Drain-Source Breakdown Voltage $(V_{GS}=0, I_{D}=250 \ \mu A)$	IRFF110 IRFF113	V _{(BR)DSS}	100 60		Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0)		IDSS	-	250	μAdc

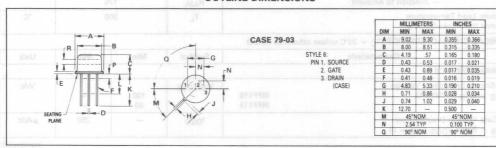
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ELECTRICAL CHARACTERISTICS — continued (Tc = 25°C unless otherwise noted)

Charact	eristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS			noited	e Inform	SOLEY
Gate-Body Leakage Current, Forward (VGS = 20 Vdc, VDS = 0)		IGSSF	-	100	μAdc
Gate-Body Leakage Current, Reversion (VGS = -20 Vdc, VDS = 0)	IGSSR	enā11	-100	nAdc	
N CHARACTERISTICS*		a bankil	Sections	second at 1 d	and the state of
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μA)		VGS(th)	2	OM 4 oss	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 1.5 Adc)	IRFF110 IRFF113	rDS(on)	igh <u>sp</u> eed pa regu <u>la</u> tors, c		Ohm
On-State Drain Current (VGS = 10 Vdc, V _{DS} = 5 V)	IRFF110 IRFF113	ID(on)	3.5 aba 3	pulse circuits. or Fast-Switchi	Anergr on Gate i
Forward Transconductance (I _D = 1.5 A) IRFF110, IRFF111		9fs	1	ren negunes lig reakdown	mhos
YNAMIC CHARACTERISTICS	T & 1/2-00		40	SOUTH STUTE CHECK	near siles
Input Capacitance		C _{iss}	_	200	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	_	100	
Reverse Transfer Capacitance		C _{rss}	-	25	
WITCHING CHARACTERISTICS*					
Turn-On Delay Time		td(on)		20	ns
Rise Time	$(V_{DD} \simeq 0.5 \text{ Rated V}_{DSS},$ $I_{D} = 1.5 \text{ A},$	t _r	0.000.000	25	
Turn-Off Delay Time	$R_{gen} = 50 \text{ ohms}$	td(off)	_	25	
Fall Time 09 00 RDGV		tf	- 1	20	
OURCE DRAIN DIODE CHARACTER	ISTICS*			1991	ource vo
Forward On-Voltage IRFF110		V _{SD}	_	2.5	Vdc
Forward Turn-On Time	IRFF113	V _{SD}	-	2	Vdc
Reverse Recovery Time	$(I_S = Rated I_{D(on)})$ $V_{GS} = 0)$	ton	-D'85	Negligible	ns
neverse necovery rime	VGS - 0)	t _{rr}	_	200 (Typ)	ns

^{*}Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Advance Information

Small-Signal Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

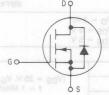
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- Excellent Temperature Stability

IRFF120 IRFF123



N-CHANNEL TMOS POWER FETS rDS(on) = 0.3 OHM 100 VOLTS rDS(on) = 0.4 OHM 60 VOLTS





MAXIMUM RATINGS

	Rating		A S.	Symbol	IRFF120	IRFF123	Unit
Drain-Source Voltage		(ita)b)	(amrlo 08	VDSS	100	60	Vdc
Drain-Gate Voltage (RGS = 1 mΩ)		42		V _{DGR}	100	60 adora MAS	Vdc
Gate-Source Voltage		VSD	120	VGS	±	20 08/0//0	Vdc
Drain Current	_	QSY	123	REAL			Adc
Continuous Pulsed			(no)(d) ba	IDM	6 24	5 20	Forward
Total Power Dissipation @ To Derate above 25°C	; = 25°C	101		PD		20 Y 18 Y 1	Watts W/°C
Operating and Storage Tempe	erature Range			T _J , T _{stg}	-55	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	6.25 175	°C/W
Maximum Lead Temperature 1.6 mm from Case for 10 s	TL	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

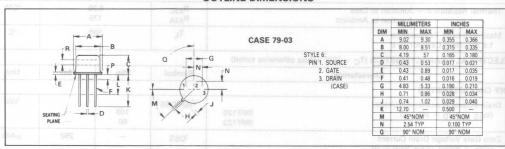
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS		18 19 1	1120	111/3/	
Drain-Source Breakdown Voltage (VGS = 0, ID = 250 μ A)	IRFF120 IRFF123	V(BR)DSS	100	- SALP	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0)		IDSS	-	250	μAdc

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Charac	teristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS			* *		
Gate-Body Leakage Current, Forw (VGS = 20 Vdc, VDS = 0)	ard	IGSSF	INZUO . B	100	nAdc
Gate-Body Leakage Current, Reve (VGS = 20 Vdc, VDS = 0)	rse	IGSSR	_ AE	-100	nAdc
N CHARACTERISTICS*		3 60 25 69 8 69 1	自由中国 图 图	PAPER I BUS	DOT B SUPE
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = 250 \mu A)$	200	VGS(th)	2	SPITA TO	Vdc
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 3 Adc)	IDEE120	rDS(on)	, high speed	0.3 0.4	Ohm bengisel
On-State Drain Current (VGS = 10 V, VDS = 5 V)	IRFF120 IRFF123	ID(on)		rivers, inverte	
Forward Transconductance (I _D = IRFF120, IRFF121 V _{DS} = IRFF122, IRFF123 V _{DS} =	= 5 V	9fs	1.5 bs		sodmos (
YNAMIC CHARACTERISTICS	4 []		yfilide	imperature Sta	Tinelles
Input Capacitance		C _{iss}	_	600	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	_	400	
Reverse Transfer Capacitance		C _{rss}	_	100	
WITCHING CHARACTERISTICS*					
Turn-On Delay Time		td(on)	_	40	ns
Rise Time (STAR)	$(V_{DD} \simeq 0.5 \text{ Rated } V_{DSS},$ $I_{D} = 3 \text{ A},$	t _r	politeit	70	
	R _{gen} = 50 ohms)	td(off)	-	100	
Turn-Off Delay Time				70	
Fall Time	HangV	tf		151,72110	
Fall Time 08 007	ваеУ	t _f .		(00	Ros - 1 r
Fall Time 08 007	ваеУ	v _{SD}		2.50010	
Fall Time OURCE DRAIN DIODE CHARACTE Forward On-Voltage	RISTICS*		-		Vdc
Fall Time OURCE DRAIN DIODE CHARACTE	RISTICS*	V _{SD}		2.5 garlo	Vdc Vdc ns

OUTLINE DIMENSIONS



Advance Information

Small-Signal Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

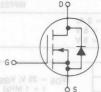
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- Silicon Gate for Fast Switching Speeds
- Low Drive Current Required
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- No Second Breakdown
- Excellent Temperature Stability

IRFF220 IRFF223



N-CHANNEL
TMOS POWER FETS
rDS(on) = 0.8 OHM
200 VOLTS
rDS(on) = 1.2 OHMS
150 VOLTS





MAXIMUM RATINGS

	- 00	Rating	7/	A (SK)(JSS)	Symbol	IRFF220	IRFF223	Unit
Drain-Source Vo	oltage		(fip)b ¹	(amilo (VDSS	200	150	Vdc
Drain-Gate Volt (RGS = 1 ms			47		VDGR	200	150 HO 30010 MIAI	Vdc
Gate-Source Vo	Itage	-	gay	0	VGS	±	20 aganloV-no	Vdc
Drain Current	1.8		ggV	133	IRFF2			Adc
Continuous Pulsed				(no)(I)	IDM	3.5 14	3 12	Forward
Total Power Dissipation @ T _C = 25°C Derate above 25°C			PD		20 .16	Watts W/°C		
Operating and	Operating and Storage Temperature Range				T _J , T _{stg}	-55	to 150	°C

THERMAL CHARACTERISTICS

TETWAL GRAND TENOTION			
Thermal Resistance — Junction to Case — Junction to Ambient	R _θ JC R _θ JA	6.25 175	°C/W
Maximum Lead Temperature 1.6 mm from Case for 10 s	TL	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

erous area characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (SEAS)	4	THAT	11.	97	
Drain-Source Breakdown Voltage (VGS = 0, I_D = 250 μ A)	IRFF220 IRFF223	V(BR)DSS	200 150	17-8-1-10 - DADER	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0)		IDSS	_	250	μAdc

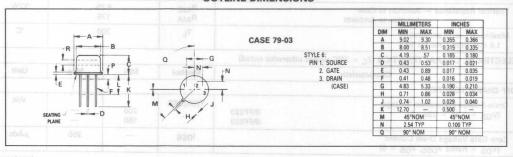
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ELECTRICAL CHARACTERISTICS — continued (TC = 25°C unless otherwise noted)

Charac	teristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS			4.		
Gate-Body Leakage Current, Forw (VGS = 20 Vdc, VDS = 0)	ard	IGSSF	попец	100	nAdc
Gate-Body Leakage Current, Reve (VGS = -20 Vdc, VDS = 0)	rse	IGSSR		- 100	nAdc
N CHARACTERISTICS*		E COM CONTRA	FE STOP IS IN	40011	a sort
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μA)	270,000	VGS(th)	2	4 1	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, I _D = 2 Adc) IRFF220 IRFF223		rDS(on)	tigh apead	0.8 1.2	Ohm
On-State Drain Current (VGS = 10 Vdc, V _{DS} = 5 Vdc)	ID(on)	3.5		Asy dr	
Forward Transconductance (I _D = IRFF220, IRFF221 V _{DS} = IRFF222, IRFF223 V _{DS} =	= 5 V	9fs	1.5	or rast switch trent Required ing	mhos
YNAMIC CHARACTERISTICS	4 17 1/		viili	det2 andered	aT inst
Input Capacitance	AD TO	C _{iss}		600	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	_	300	
Reverse Transfer Capacitance	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	C _{rss}	_	80	
WITCHING CHARACTERISTICS*					
Turn-On Delay Time		[†] d(on)	_	40	ns
Rise Time	(V _{DD} ≈ 0.5 Rated V _{(BR)DSS} , I _D = 2 A	t _r	no.ling	60	
Turn-Off Delay Time	R _{gen} = 50 ohms)	^t d(off)	_	100	
Fall Time 681 605	enaV	tf	_	60	Late Man
OURCE DRAIN DIODE CHARACTE	RISTICS*			(1)	Im t = a
Forward On-Voltage	IRFF220	V _{SD}		2 aparts	Vdc
SBA A	IRFF223	V _{SD}	-	1.8	Vdc
Forward Turn-On Time	(IS = Rated ID(on)	ton	_	Negligible	ns
Reverse Recovery Time	$V_{GS} = 0$	t _{rr}		350 (Typ)	ns

^{*}Pulse Test Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

OUTLINE DIMENSIONS



Power Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate TMOS

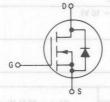
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds

- Low rDS(on) to Minimize On-Losses
 Rugged SOA is Power Dissipation Limited
 Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FETs 14 and 15 AMPERES rDS(on) = 0.1 OHM 50 VOLTS rDS(on) = 0.12 OHM





MAXIMUM RATINGS

			0	-	Device		
Rating		Symbol	IRFZ20 IRFZ22		Unit		
Drain-Source Voltage	(((0)))		V _{DSS}		50	Vdc	
Drain-Gate Voltage (RGS = 1 M Ω)	200,000,00	e spic	VDGR	S G G A J	50	Vdc	
Gate-Source Voltage	(HO)E		VGS		±20	Vdc	
Drain Current — Continuous @ T _C = 25°C — Continuous @ T _C = 100°C	90		I _D	15 10	14 9 egrent	Adc	
— Pulsed @ T _C = 25°C □	200	Lei batel	IDM	60	56, 1000	Sate Source	
Total Power Dissipation @ T _C = 25°C Derate above 25°C			PD	*SOITSIBT	40 0.32	Watts W/°C	
Operating and Storage Temperature Range	rioV	T	TJ, T _{stg}		-65 to 150	°C	

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	R _θ JC	3.12 emil y	°C/W
— Junction to Ambient Maximum Lead Temperature for Soldering Purposes,	R _Ø JA	62.5	°C
1/8" from Case for 5 Seconds			

See the MTP15N05E Designer's Data Sheet for a complete set of design curves for the IRFZ20. See the MTP12N05E Designer's Data Sheet for a complete set



Ch	naracteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS		- 000	50.00.000	at at the same	
Drain-Source Breakdown Voltag	ge (V _{GS} = 0, I _D = 0.25 mA)	V(BR)DSS	50	01917	Vdc
Zero Gate Voltage Drain Currer (VDS = Rated VDSS, VGS = (VDS = 0.8 Rated VDSS, VGS	0)	IDSS	nemean	0.2 1	mAdc
Gate-Body Leakage Current, Fo	rward (VGSF = 20 Vdc, VDS = 0)	IGSSF	_	100	nAdc
Gate-Body Leakage Current, Re	verse (VGSR = 20 Vdc, VDS = 0)	IGSSR	are designed	100	nAdc
ON CHARACTERISTICS*		drivers.	valer bas bid	arters, solen	tors, conv
Gate Threshold Voltage (VDS =	VGS, ID = 0.25 mA)	V _{GS(th)}	ebsed2 pnid	or Fast Switte	Vdc
Static Drain-Source On-Resistar (VGS = 10 Vdc, ID = 9 Adc)	nce IRFZ20 IRFZ22	rDS(on))n-Losses Vissip⇔ion L	0.1 0.12	Ohm
On-State Drain Current (V _{GS} = $(V_{DS} \ge 1.5 \text{ Vdc})$ (V _{DS} $\ge 1.7 \text{ Vdc})$	10 V) IRFZ20 IRFZ22	I _D (on)	15 14	in Diode Chi bads	Adc
Forward Transconductance (VDS \geq 1.5 V, ID = 9 A) (VDS \geq 1.7 V, ID = 9 A)	IRFZ20 IRFZ22	9FS	5 5	=	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	8.6	Ciss	-	850	pF
Output Capacitance	$(V_{DS} = 25 \text{ V, V}_{GS} = 0,$ f = 1 MHz)	Coss	_	350	TAR NUR
Reverse Transfer Capacitance		C _{rss}	-	100	area arrows
SWITCHING CHARACTERISTICS*	Symbol		Rating		
Turn-On Delay Time		td(on)		30	ns
Rise Time	$(V_{DD} \approx 25 \text{ V}, I_D = 9 \text{ Apk},$	t _r	- (0)	90	IV somes-
Turn-Off Delay Time	R _{gen} = 50 Ohms)	td(off)	34.00	40	Hov sist-
Fall Time	S9A	tf		30	OV sounds
Total Gate Charge	01	Qg	12 (Typ)	17	nC
Gate-Source Charge	(V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 10 Vdc, I _D = Rated I _D)	Qgs	9 (Typ)	Pulse d (a Tg	
Gate-Drain Charge	a ^q	Q_{gd}	3 (Typ)	gT ® m ailegle	Power Dis
SOURCE-DRAIN DIODE CHARACT	TERISTICS*				
Forward On-Voltage	(I _S = Rated I _D ,	V _{SD}	0.8 (Typ)	1.1(1)	Vdc
Forward Turn-On Time	$V_{GS} = 0$	ton	Limite	d by stray indu	uctance
Reverse Recovery Time	Staff	t _{rr}	100 (Typ)	ncelunctio	ns
*Pulse Test: Pulse Width ≤ 300 μs, Do 1) Add 0.15 V for IRFZ20.	uty Cycle ≤ 2%.	urposes,	r so Ambient or Soldering Pr	temperature fi	beed mum

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14 SM. 1982.

2. CONTROLLING DIMENSION: INCH.

3. DIM 2 DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

Power Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate TMOS

IRFZ32

IRFZ30

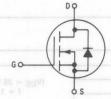
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds

- Low rDS(on) to Minimize On-Losses
 Rugged SOA is Power Dissipation Limited
 Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FETS 25 and 30 AMPERES rDS(on) = 0.05 OHM 50 VOLTS rDS(on) = 0.07 OHM





MAXIMUM RATINGS

	25	ina (no)bi		C	Device pmit ya		Unit
	Rating Symb	Symbol	IRFZ30	IRFZ32	emiT sall		
Drain-Source	Voltage	(Ito)b ²	O Ohmst	VDSS		ay Timo 05	Vdc
Drain-Gate Vo	Itage (RGS = 1 M Ω)	¥2		VDGR		50	Vdc
Gate-Source V	oltage (gyT) 8	20 21		VGS	±20 agrad3		Vdc
Drain Current — Continuous @ T _C = 25°C — Continuous @ T _C = 100°C — Pulsed @ T _C = 25°C		IDM	30 19 80	25 16 60	mia IQ emi		
Total Power D Derate abov	ve 25°C T _C = 25		ni beti	PD		75 0.6 spallov-	Watts W/°C
Operating and	Storage Temperatur	e Range	(0 =	TJ, T _{stg}	-65	to 150	O. C.

THERMAL CHARACTERISTICS OF THE STATE OF THE

Thermal Resistance — Junction to Case — Junction to Ambient	R _θ JC	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	JT CASE 221	300	°C

See the MTP30N05E Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

Characterist	ic		Symbol		Min	Max	Unit
FF CHARACTERISTICS							
Drain-Source Breakdown Voltage (VGS =	0, ID = 0.25 mA)		V(BR)DS	3	50		Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0, TJ = 125°C)			IDSS	islai	d En	0.2	mAdc
Gate-Body Leakage Current, Forward (VG		s = 0)	IGSSF	1 0 0 0 00	- 9/15/	100	nAdc
Gate-Body Leakage Current, Reverse (VG			IGSSR	_	_	100	nAdc
ON CHARACTERISTICS*	A DO	,eps	May wol 1	of bang	Ts are desi	Power FE	e TMOS
Gate Threshold Voltage (VDS = VGS, ID	= 0.25 mA)	gain	V _{GS(th)}	ons suo	2	4	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 16 Adc)		IRFZ30 IRFZ32	rDS(on)		victhing Sp	0.05 0.07	Ohm
On-State Drain Current (V _{GS} = 10 V) (V _{DS} \geq 1.5 Vdc) (V _{DS} \geq 1.75 Vdc)	G	IRFZ30 IRFZ32	ID(on)	imul no U for U	30 25	DA is Power ein Diage	Adc
Forward Transconductance $(V_{DS} \ge 1.5 \text{ V, } I_{D} = 16 \text{ A})$ $(V_{DS} \ge 1.75 \text{ V, } I_{D} = 16 \text{ A})$	IRFZ30 IRFZ32		9FS		9	=	mhos
DYNAMIC CHARACTERISTICS	11/						
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0 f = 1 MHz)			Ciss	_	1600	pF
Output Capacitance				Coss		800	
Reverse Transfer Capacitance			C _{rss}	_	200		
SWITCHING CHARACTERISTICS*						SDM	TAR WUI
Turn-On Delay Time				td(on)	noiseR	25	ns
Rise Time SSSAM DESPRIN	(V _{DD} ≈ 25 V	, ID = 16 Ap	k,	tr	_	35	
Turn-Off Delay Time	Rgen =	50 Ohms)		d(off)	_	45	Source
Fall Time 08	Apev			tf	(OM I	35	NoV esso-
Total Gate Charge	(Vpc = 0.8	Rated Voca		Ωg	26 (Typ)	30	nC
Gate-Source Charge	VGS = 10 Vdc	Rated V _{DSS} c, I _D = Rated	ID)	Qgs	14 (Typ)	- Co st inue	Current
Gate-Drain Charge	had			Q_{gd}	12 (Typ)	6) basius -	
SOURCE-DRAIN DIODE CHARACTERISTICS	- 09				792 = oT	aniterio	Power Dis
Forward On-Voltage	(I _S = I	Rated ID,		V _{SD}	1.2 (Typ)	1.5(1)	Vdc
Forward Turn-On Time	VGS	$V_{GS} = 0$		ton		by stray in	
Reverse Recovery Time Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤	2%.			t _{rr}	150 (Typ)	RACTERIAL Inca — Jun	ns in ns
1) Add 0.1 V for IRFZ30.	EATING CAS	E 221A-04 D-220AB)	STYLE 5: PIN 1. GATE 2. DRAIN	ing Purp ing omplet	DIM MIN A 14.48 B 9.66 C 4.07	MAX MIN MU 15.75 0.570 0.6 10.28 0.380 0.4 4.82 0.160 0.1	AX 120 100 100 11M
	V14 58	NSIONING AND TOLERANCING IL 1982: BOULING DIMENSION: INCH. DEFINES A ZONE WHERE ALL			F 3.61 G 2.42 H 2.80 J 0.36 K 12.70 L 1.15 N 4.83 Q 2.54	0.88 0.025 0.0 3.73 0.142 0.1 2.66 0.095 0.1 3.93 0.110 0.1 4.27 0.500 0.5 1.39 0.045 0.0 5.33 0.190 0.2 3.04 0.100 0.1 2.79 0.060 0.1 3.90 0.045 0.0 6.47 0.235 0.2 1.27 0.000 0.0 1.29 0.000 0.0 1.21 0.000 0.0 1.22 0.000 0.0 1.23 0.000 0.0 1.24 0.000 0.0 1.25 0.000 0.0 1.27 0.000 0.0 1.28 0.000 0.0 1.28 0.000 0.0 1.29 0.000 0.0	05 55 22 62 65 55 10 10

Power Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

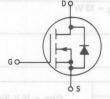
- Silicon Gate for Fast Switching Speeds

- Low rDS(on) to Minimize On-Losses
 Rugged SOA is Power Dissipation Limited
 Source-to-Drain Diode Characterized for Use With Inductive Loads



IRFZ40 IRFZ42

TMOS POWER FETS 46 and 51 AMPERES rDS(on) = 0.028 OHM 50 VOLTS rDS(on) = 0.035 OHM





MAXIMUM RATINGS

Rating			Symbol	Des	Device	
nating			Symbol	IRFZ40	IRFZ42	Unit
Drain-Source Voltage	17	Jr. A. 00	VDSS	5	0	Vdc
Drain-Gate Voltage ($R_{GS} = 1 M\Omega$)	Oholist	(8)	VDGR	5	0 acet vale	Vdc
Gate-Source Voltage	N.		VGS	±	20	Vdc
Drain Current — Continuous @ T _C = 25°C — Continuous @ T _C = 100°C — Pulsed @ T _C = 25°C	Q _Q g	VDSS- Rated ID	ID beta 8 0 = 20 = 0 Mol la	51 32 160	46 29 145	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	bgD		PD	12 RACTERISTICS	Cherge 25	Watts W/°C
Operating and Storage Temperature Range	geV		TJ, T _{stq}	- 65 1	to 150	°C

TIETHIAE CHARACTERIOTICS			
Thermal Resistance — Junction to Case	R _Ø JC	1 emiT yrevose	°C/W
Junction to Ambient	R _θ JA	62.5	Later Tarristy
Maximum Lead Temperature for Soldering Purposes,	TL	300 INF240	VEO DOC III
1/8" from Case for 5 Seconds			

See the MTP50N05E Designer's Data Sheet for a complete set of design curves for these devices.



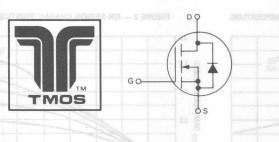
	Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS			Service Control	the state where the	- 10 10 mark	
Drain-Source Breakdown Volt	age (V _{GS} = 0, I _D = 0.25 m/		V(BR)DSS	50	MeH.	Vdc
Zero Gate Voltage Drain Curro (VDS = Rated VDSS, VGS (VDS = 0.8 Rated VDSS, V	IDSS	nce <u>m</u> er OS-	0.2 1	mAdc		
Gate-Body Leakage Current, F	Forward (VGSF = 20 Vdc, VD	os = 0)	IGSSF	_	100	nAdc
Gate-Body Leakage Current, F	Reverse (VGSR = 20 Vdc, VD	s = 0) (988)	IGSSR	ars <u>de</u> signe	100	nAdc
N CHARACTERISTICS*		Bung	divid en rique à	applications	ver syntching	app soute
Gate Threshold Voltage (VDS	= V _{GS} , I _D = 0.25 mA)		V _{GS(th)}	2	4	Vdc
$ \begin{array}{lll} \text{Static Drain-Source On-Resistance} & \text{IRFZ40} \\ \text{(V}_{\text{GS}} = \text{10 Vdc, I}_{\text{D}} = \text{29 Adc)} & \text{IRFZ42} \\ \end{array} $			rDS(on)	On-Lossas Dissipation	0.028	Ohm
On-State Drain Current (V _{GS} = 10 V) (V _{DS} ≥ 1.4 Vdc) (V _{DS} ≥ 1.6 Vdc) IRFZ40 IRFZ42			ID(on)	51 45	ain Diode Ch .oads—	G-o Adc
Forward Transconductance $(V_{DS} \ge 1.4 \text{ V, } I_D = 29 \text{ A})$ IRFZ40 $(V_{DS} \ge 1.6 \text{ V, } I_D = 29 \text{ A})$ IRFZ42			9FS	17 17	=	mhos
YNAMIC CHARACTERISTICS						
Input Capacitance	8.0		Ciss	_	3000	pF
Output Capacitance	(V _{DS} = 25 V, V _G f = 1 MHz	S = 0,	Coss	_	1200	
Reverse Transfer Capacitance			C _{rss}		400	AR MUMI
WITCHING CHARACTERISTICS	Symbol *2			Reting		
Turn-On Delay Time	047-340		td(on)		25	ns
Rise Time	(V _{DD} ≈ 25 V, I _D =	29 Apk,	t _r		60	in-Source \
Turn-Off Delay Time	R _{gen} = Ohn	ns)	td(off)	(DM	= 270 988	in-Gasa Vol
Fall Time	sov		tf		25	V saruos-at
Total Gate Charge	id di		Qg	40 (Typ)	euou 60 m3 -	Janan nC mi
Gate-Source Charge	(V _{DS} = 0.8 Rated V _{GS} = 10 Vdc, I _D =	Rated In)	Qgs	22 (Typ)	- Pulsed in T	
Gate-Drain Charge	09		Q _{gd}	18 (Typ)	T ib) goitsgiss	C rewo? Is
OURCE-DRAIN DIODE CHARA	CTERISTICS*				26°C	erate above
Forward On-Voltage	(IS = Rated	In.	V _{SD}	1.3 (Typ)	2.2(1)	Vdc
Forward Turn-On Time	V _{GS} = 0)	D.	ton	Limite	d by stray indu	uctance
Reverse Recovery Time	Rasc		t _{rr}	350 (Typ)	ance Junet	aiasA ns
Pulse Test: Pulse Width ≤ 300 µs, 1) Add 0.3 V for IRFZ40.	Duty Cycle ≤ 2%.		Purpases,	on to Ambient for Seldering	Тегорогалига	simum Lead
D A A U	R NOTES:	CASE 221A-04 TO-220AB	STYLE 5: PRI 1. GATE 2. DRAIN 3. SOURCE 4. BRAIN		MELIMETERS IN MAX	0.620 0.405 0.190 0.035 0.147 0.105 0.155 0.022 0.552 0.056 0.210 0.110 0.110 0.110 0.110 0.110 0.110 0.110 0.110

MFE910 MPF910

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

This TMOS FET is designed for high-voltage, high-speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor of TTL-to-high voltage interface and high voltage display drivers.

- Fast Switching Speed $t_{on} = t_{off} = 6.0 \text{ ns Typ}$
- Low On-Resistance 2.0 Ohms Typ
- Low Drive Requirement, V_{GS(th)} = 2.5 V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices



MAXIMUM RATINGS			
Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	60	Vdc
Gate-Source Voltage	VGS	901 ± 15	Vdc
Drain Current — Continuous (1) Pulsed (2)	I _D	0.5	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C MFE910	PD	6.25 50	Watts mW/°C
Total Power Dissipation @ T _A = 25°C Derate above 25°C MPF910	PD	1.0 8.0	Watts mW/°C
Operating and Storage Temperature Range	TJ, Tsta	-55 to +150	°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.

(2) Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

60 VOLTS

N-CHANNEL TMOS

MFE910



CASE 79-02 TO-205AD

MPF910 - 5 BRUDE



CASE 29-03 TO-226AE

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS				Add Falled T	37-442-19-19
Drain-Source Breakdown Voltage (VGS = 0, I _D = 100 μA)	V _{(BR)DSS}	60	90	_	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 40 V, V _{GS} = 0)	IDSS	-	0.1	10	μAdc
Gate-Body Leakage Current (VGS = 10 V, V _{DS} = 0)	IGSS	_	0.01	10	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1.0 mA)	VGS(th)	0.3	1.5	2.5	Vdc
Drain-Source On-Voltage (VGS = 10 V, I _D = 500 mA)	V _{DS(on)}	ge interface	to-hig t velta	2.5	Vdc
On-State Drain Current (V _{DS} = 25 V, V _{GS} = 10 V)	I _{D(on)}	500	$d - t_{on} = t_{on} - b$	tchin g Spee Rasistance	MA S
Forward Transconductance (V _{DS} = 15 V, I _D = 500 mA)	9FS	100	ent, Ves(in)	meriu p añ e	mmhos

FIGURE 1 — V_{GS(th)} NORMALIZED versus TEMPERATURE

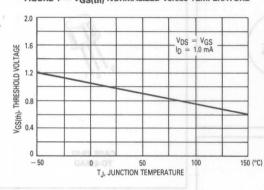


FIGURE 2 — ON-REGION CHARACTERISTICS

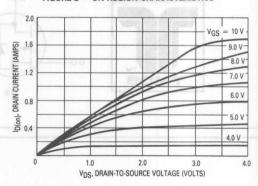


FIGURE 3 — OUTPUT CHARACTERISTICS

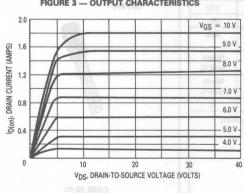
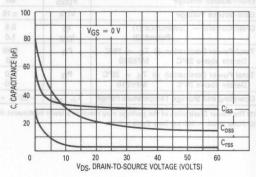
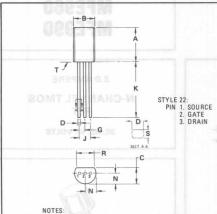


FIGURE 4 — CAPACITANCE versus DRAIN-TO-SOURCE VOLTAGE



OUTLINE DIMENSIONS

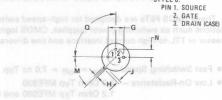


- 1. DIMENSIONS -A- AND -B- ARE DATUMS.
- TO IS SEATING PLANE.
 POSITIONAL TOLERANCE FOR LEADS: ♦ Ø 0.10 (0.004) M T A M B M
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIM	ETERS	INCHES			
DIM	MIN	MAX	MIN	MAX		
A	7.37	7.87	0.290	0.310		
В	4.44	5.21	0.175	0.205		
C	3.18	4.19	0.125	0.165		
D	0.46	0.61	0.018	0.024		
G	1.27	BSC	0.050 BSC			
J	2.54	2.54 BSC		0.100 BSC		
K	12.70	-	0.500	-		
N	2.03	2.92	0.080	0.115		
R	3.43	normal a	0.135	-		
S	0.46	0.61	0.018	0.024		

CASE 29-03 TO-226AE

R	
В	1
+ TI-II-II +	-
"E / F	K
SEATING UU	N-CHA
PEANE	STYLE 6: PIN 1. SOURCE



ı		MILLIM	ETERS	INC	HES	
1	DIM	MIN	MAX	MIN	MAX	V3
ı	A	8.89	9.40	0.350	0.370	
1	В	8.00	8.51	0.315	0.335	
I	C	6.10	6.60	0.240	0.260	
1	D	0.406	0.533	0.016	0.021	
1	E	0.229	3.18	0.009	0.125	103
1	F	0.406	0.483	0.016	0.019	13
1	G	4.83	5.33	0.190	0.210	133
1	Н	0.711	0.864	0.028	0.034	
1	J	0.737	1.02	0.029	0.040	
ı	K	12.70	-	0.500	-	
	L	6.35	-	0.250	100 m	
1	M	450 N	MON	450 N	OM	137
1	P	-	1.27	MUT TH	0.050	
	Q	900 1	MOM	900 N	IOM	19
П	R	2.54	-	0.100	200	1 0

All JEDEC dimensions and notes apply.

CASE 79-02 TO-205AD

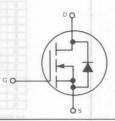
MFE930 MFE960 MFE990

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

These TMOS FETs are designed for high-speed switching applications such as switching power supplies, CMOS logic, microprocessor or TTL-to-high current interface and line drivers.

- Fast Switching Speed ton = toff = 7.0 ns Typ
- Low On-Resistance 0.9 Ohm Typ MFE930
 1.2 Ohm Typ MFE960 and MFE990
- Low Drive Requirement, V_{GS(th)} = 3.5 V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices





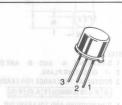
MAXIMUM RATINGS

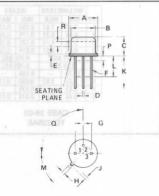
Rating	Symbol	MFE930	MFE960	MFE990	Unit
Drain-Source Voltage	V _{DSS}	35	60	90	Vdc
Drain-Gate Voltage	V _{DGO}	35	60	90	Vdc
Gate Source Voltage	VGS		± 30		Vdc
Drain Current Continuous (1) Pulsed (2)	I _D	2.0 3.0			Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	6.25 50			Watts mW/°C
Operating and Storage Temperature Range	T _J ,T _{stg}	- 55 to 150			°C

(1) The Power Dissipation of the package may result in a lower continuous drain current. (2) Pulse Width \leqslant 300 μ s, Duty Cycle \leqslant 2.0%.

2.0 AMPERE N-CHANNEL TMOS

FET 30, 60, 90 VOLTS





STYLE 6: PIN 1. SOURCE 2. GATE 3. DRAIN (CASE)

	MILLIM	ETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	8.89	9.40	0.350	0.370
В	8.00	8.51	0.315	0.335
С	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
Н	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	-	0.500	-
L.	6.35	-	0.250	-
M	450 N	IOM	450 N	MOI
P	-	1.27	-	0.050
0	90° NOM		90° NOM	
R	2.54	-	0.100	-

All JEDEC dimensions and notes apply.

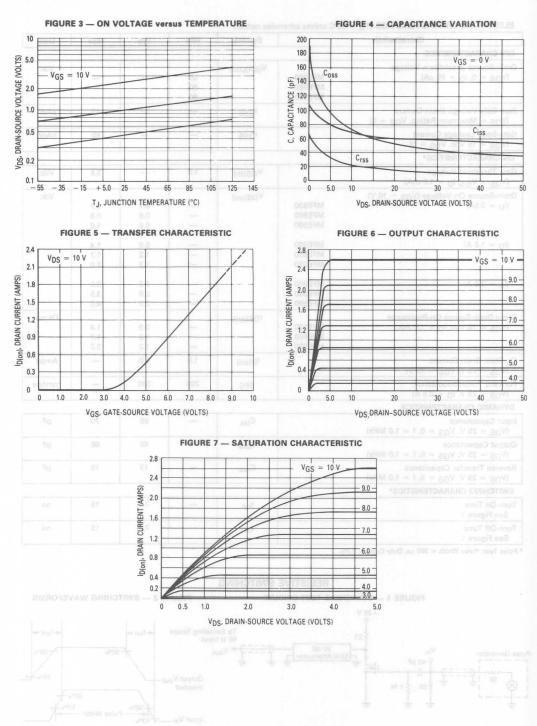
CASE 79-02 TO-205AD ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise noted.)

Characteristic	30%	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS	180					
Drain-Source Breakdown Voltage (VGS = 0, I _D = 10 μA)	MFE930 MFE960 MFE990	V(BR)DSS	35 60 90		V 08	Vdc
Zero Gate Voltage Drain Current (VDS = Maximum Rating, VGS = 0)	1000	IDSS			10	μAdc
Gate-Body Leakage Current (VGS = 15 Vdc, VDS = 0)	703	IGSS			50	nAdc
ON CHARACTERISTICS*	100					
Gate Threshold Voltage (Vps = Vgs, Ip = 1.0 mA)	0	V _{GS(th)}	1.0		3.5	Vdc
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 0.5A)	MFE930 MFE960 MFE990	V _{DS(on)}	TURE (<u>°C)</u>	0.4 0.6 0.6	0.7 0.8 1.0	Vdc
(I _D = 1.0 A)	MFE930 MFE960 MFE990			0.9 1.2 1.2	1.4 1.7 2.0	
(I _D = 2.0 A)	MFE930 MFE960 MFE990		=	2.2 2.8 2.8	3.0 3.5 4.0	0
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 1.0 Adc)	MFE930 MFE960 MFE990	rDS(on)		0.9 1.2 1.2	1.4 1.7 2.0	Ohms
On-State Drain Current (VDS = 25 V, VGS = 10 V)	108	I _{D(on)}	1.0	2.0	-	Amps
Forward Transconductance (V _{DS} = 25 V, I _D = 0.5 A)		9FS	200	380	20 30	mmhos
DYNAMIC CHARACTERISTICS			- /SC 40WA 30 A	TION SOCIOS	Ven CATE	
Input Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)		C _{iss}	_	60	70	pF
Output Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)	N CHARACTERIS	Coss	FIGURE	49	60	pF
Reverse Transfer Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)	V 01 = 80V	C _{rss}		13	18	pF
SWITCHING CHARACTERISTICS*				1, 2		
Turn-On Time See Figure 1		ton	-	7.0	15	ns
Turn-Off Time See Figure 1		toff		7.0	15	ns

^{*} Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

RESISTIVE SWITCHING





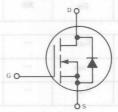
MFE9200

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD EFFECT TRANSISTOR

This TMOS FET is designed for high-voltage, high-speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor or TTL-to-high voltage interface and high-voltage display drivers.

- Fast Switching Speed ton = toff = 6.0 ns Typ
- Low On-Resistance 4.5 Ohms Typ
- Low Drive Requirement, VGS(th) = 4.0 V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices





MAXIMUM RATINGS

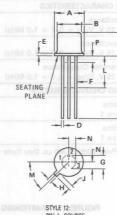
Rating	Symbol	Value	Unit
Drain-Source Voltage	VDSS	200	Vdc
Gate-Source Voltage	VGS	± 20	Vdc
Drain Current Av Danis (1) Continuous (1) Pulsed (2)	I _D I _{DM}	400 800	mAdc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD squad	1.8 14.4	Watts mW/°C
Operating and Storage Temperature Range	T _J ,T _{stg}	- 55 to 150	°C

(1) The Power Dissipation of the package may result in a lower continuous drain current. (2) Pulse Width \leqslant 300 μs , Duty Cycle \leqslant 2.0%.

200 VOLTS

N-CHANNEL TMOS





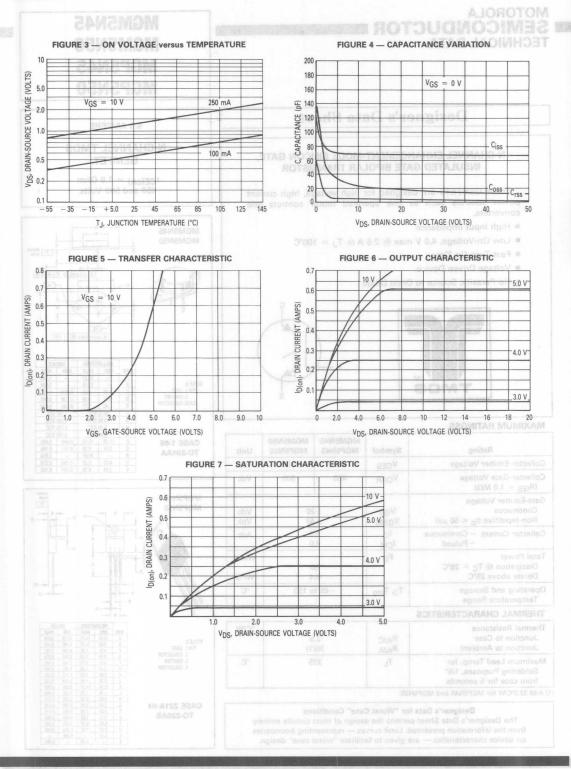
STYLE 12: PIN 1. SOURCE 2. GATE 3. DRAIN (CASE)

	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	5.31	5.84	0.209	0.230	
В	4.52	4.95	0.178	0.195	
C	4.32	5.33	0.170	0.210	
D	0.406	0.533	0.016	0.021	
E	-	0.762	-	0.030	
F	0.406	0.483	0.016	0.019	
G	2.54	BSC	0.100 BSC		
Н	0.914	1.17	0.036	0.046	
J	0.711	1.22	0.028	0.048	
K	12.70	-	0.500	-	
L	6.35	-	0.250	-	
M	450	45º BSC		BSC	
N	1.27 BSC		0.050 BSC		
P		1.27	-	0.050	

All JEDEC notes and dimensions apply.

CASE 22-03 TO-18

Characteristic		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 10 μA)		V _{(BR)DSS}	200	_	_	Vdc
Zero Gate Voltage Drain Current (VDS = 200 V, VGS = 0)		IDSS	_	0.1	10	μAdc
Gate-Body Leakage Current (VGS = 15 Vdc, VDS = 0)		IGSS	VOEMENT	0.01	50	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1.0 mA)	-rtotive	VGS(th)	1.0 agatlov-rigi	rigned for h	4.0 ob al 133 30	Vdc
Drain-Source On-Voltage (VGS = 10 V) (ID = 100 mA) (ID = 250 mA) (ID = 500 mA)	oltage	VDS(on)	ers, relay o taga <u>in</u> terfa —	0.45 1.20 3.0	0.6 1.60	Vdc
On-State Drain Current (VDS = 25 V, VGS = 10 V)		I _{D(on)}	400	700	tching Spar	MA MA
State Drain-Source On-Resistance (VGS = 10 Vdc)		rDS(on)	1 V 0 V 1	ent, Vosin	resistance e Requirem	Ohms
(I _D = 100 mA) (I _D = 250 mA) (I _D = 500 mA)	lo gni	Easy Parallel	lifty Permits	4.5 4.8 6.0	6.0 6.4 —	 Inhetent Many De
Forward Transconductance		9fs	200	400	_	mmhos
(V _{DS} = 25 V, I _D = 250 mA) DYNAMIC CHARACTERISTICS				1238	100 A	
Input Capacitance (VDS = 25 V, VGS = 0, f = 1.0 MHz)		C _{iss}	-	72	90	pF
Output Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)		Coss	L=00	15	20	pF
Reverse Transfer Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)		C _{rss}	_	2.8	3.5	pF
SWITCHING CHARACTERISTICS*						
Turn-On Time See Figure 1		ton	-	6.0	15	ns
Turn-Off Time See Figure 1		toff		6.0	15	ns
Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.						T PROPRESSA
	RESISTIVE	SWITCHING	3			
	TIEGIO TIVE	SWITCHING	•			
FIGURE 1 — SWITCHING TEST C	DDAM			URE 2 — SI		AVEFORMS
Ise Generator 800.0 Vin 16.4 A 500.0	20 dB		ampling Scope	e ton >		3 104 2
50 1	Attenuator	10 150 ±		pteT T	-90% agardi	
### ##################################			Output Vo	50% 10%		10%



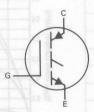
Designer's Data Sheet

N-CHANNEL ENHANCEMENT-MODE SILICON GATE, INSULATED GATE BIPOLAR TRANSISTOR

These GEMFETS are designed for high voltage, high current power controls such as line operated motor controls and converters

- High Input Impedance
- Low On-Voltage, 4.0 V max @ 2.5 A @ T_J = 100°C
- Fast Turn-On Time
- Voltage Driven Device
- No Parasitic Source to Drain Diode





MAXIMUM RATINGSS

Rating	Symbol	MGM5N45 MGP5N45	MGM5N50 MGP5N50	Unit
Collector-Emitter Voltage	VCES	450	500	Vdc
Collector-Gate Voltage (RGS = 1.0 M Ω)	VCGR	450 500		Vdc
Gate-Emitter Voltage Continuous Non-repetitive ($t_p \le 50 \mu s$)	V _{GE} V _{GEM}	the Control of the Co	20 40	Vdc Vpk
Collector Current — Continuous — Pulsed	I _C	5.0 8.0		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		50 .4	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	- 65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case Junction to Ambient	R ₀ JC R ₀ JA	2.5 30(1)	20114
Maximum Lead Temp. for Soldering Purposes, 1/8"	TL	275	°C

(1) Add 32.5°C/W for MGP5N45 and MGP5N50.

Designer's Data for "Worst Case" Conditions

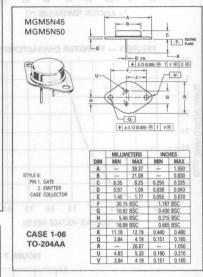
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

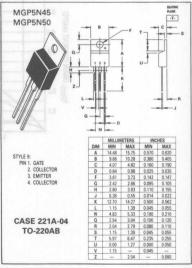
MGM5N50 MGP5N45 MGP5N50

5.0 AMPERE

N-CHANNEL TMOS GEMFET

rCE(on) = 1.6 Ohm 450 and 500 Volts

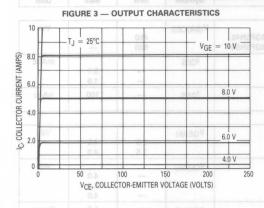


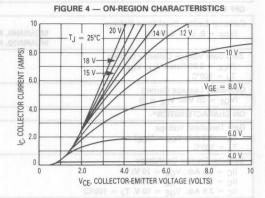


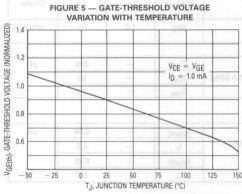
EL ECTRICAL	CHARACTERISTICS	/To - 25	oc unlace	othonwico	notec

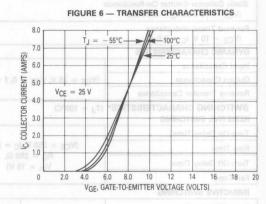
Characteristic			Symbol	Min	Max	Unit
OFF CHARACTERISTICS	— N SRUDR	- 8	PACLEMENT	AND TUSTU	GURE 3 — OI	JS .
Collector-Emitter Breakdown Voltage (VGE = 0, IC = 5.0 mA)		145, MGP5N45 150, MGP5N50	V(BR)CES	450 500	<u> </u>	Vdc
Zero Gate Voltage Collector Current ($V_{CE} = 0.85$ Rated V_{CE} , $V_{GE} = 0$) $T_{J} = 100$ °C	-V 81 5.8 S		ICES		0.1 1.0	mAdc
Gate-Body Leakage Current (VGE = 20 Vdc, VCE = 0)		V-0.8	IGES	-	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (I _C = 1.0 mA, V _{CE} = V _{GE}) T _J = 100°C	0.5 0	, V88_	VGE(th)	2.0 1.5	4.5 4.0	Vdc
Collector-Emitter On-Voltage (I _C = 2.5 Adc, V _{GE} = 10 V) (I _C = 5.0 Adc, V _{GE} = 15 V) (I _C = 2.5 Adc, V _{GE} = 10 V, T _J = 100°C)			VCE(on)	00 RBT <u>D4</u> 3 ROT	4.0 5.0 4.0	Vdc
Static Collector-Emitter On-Resistance (VGE = 10 Vdc, IC = 2.5 Adc)	a sauam	3	rCE(on)	NEST FRESH	1.6	Ohms
Forward Transconductance (V _{CE} = 10 V, I _C = 5.0 A)	- = 1 1 38		9FS	1.0	Ī	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	0.00		Ciss		300	pF
Output Capacitance	$V_{CE} = 25 \text{ V}, V_{GE} = 0, f = 1.0 \text{ MHz}$		Coss	-	50	
Reverse Transfer Capacitance	V65 = 25 V	C _{rss}	_	10		
SWITCHING CHARACTERISTICS* RESISTIVE SWITCHING	$(T_{J} = 100^{\circ}C)$					
Turn-On Delay Time	2.0		td(on)	-	0.04	μs
Rise Time	(VCE = 250 V,		tr	-	0.5	5 - 18 -
Turn-Off Delay Time	$R_G = 2!$ $V_{in} = 1$		td(off)	_	0.25	
Fall Time M VI OI 08 0	0 20 40	125 150	tf	0.0	5.0	
INDUCTIVE SWITCHING	40 HON		(D') BRUTA	CTON TOWNE	MUL-IJ.	
Turn-Off Delay Time	/V . 252.V	$R_G = 0.25 \text{ k}\Omega$	td(off)	_	0.25	μs
Crossover Time	$V_{clamp} = 250 V,$ $V_{clamp} = 5.0 A,$	J.G SIZO KAZ	t _c	AN CENTRE	5.0	1
Turn-Off Delay Time	$L = 180 \mu H$,	$R_G = 1.0 \text{ k}\Omega$	td(off)		1.0	
Crossover Time	$V_{in} = 15 V$		t _C		5.0	
*Pulse Test: Pulse Width ≤ 300 μs, Duty C	ycle ≤ 2.0%.	700	307			
	RESISTI	VE SWITCHING	310			
FIGURE 1 — SWITCHING TES	\$ 120 H	F	IGURE 2 — SV	VITCHING V	VAVEFORMS	
Copp	RL Vout	[‡] d(on) ton	– t _r – 90%	td(off)	toff • tf • 90%
Pulse Generator Rgen 50 Ω RG	DUT	Output, Vout Inverted	10%	O.A (O.D.)	90%	0.0

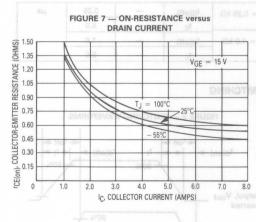












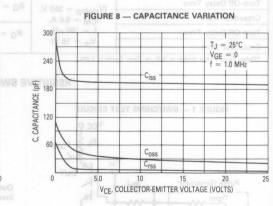
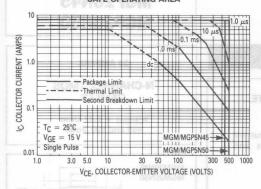


FIGURE 9 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable collector current (ICM) may be calculated with the aid of the following equation:

$$I_{CM} = I_{C}(25^{\circ}C) \left[\frac{T_{J(max)} - T_{C}}{P_{D} \cdot R_{\theta JC} \cdot r(t)} \right]$$

where

I_C(25°C) = the dc collector current at T_C = 25°C from

Figure 9. T_{J(max)} = rated maximum junction temperature

= device case temperature TC

PD = rated power dissipation at T_C = 25°C $R_{\theta JC}$ = rated steady state thermal resistance

r(t) = normalized thermal response from Figure 11

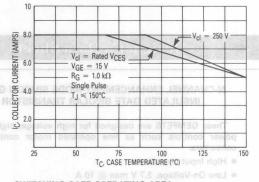


FIGURE 10 - MAXIMUM RATED SWITCHING SAFE OPERATING AREA

SWITCHING SAFE OPERATING AREA

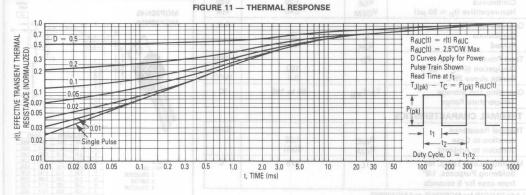
The switching safe operating area (SSOA) of a GEM-FET device is a composite function of gate turn-off time, inductive clamp voltage (Vcl) and device junction temperature (T_J). Figure 10 illustrates that I_C is 8.0 A for Vcl \leq 250 V and T_J \leq 90°C, and for Vcl \leq 500 V and T_J ≤ 65°C. Additionally, it is seen that for a peak collector current of 6.0 A, TJ must be maintained less than 130°C for $V_{cl} = 250 \text{ V}$, and less than 120°C for $V_{cl} = 500 \text{ V}$. T_J may be calculated from the equation:

$$T_J = T_C + P_{D^{\bullet}}R_{\theta J}C^{\bullet r}(t)$$

where

PD is the power averaged over a complete switching cycle.

Generally, SSOA current declines with decreasing gate turn-off time. Gate turn-off time is controlled by RG; lowering RG decreases gate turn-off time. A suggested rule-of-thumb is to derate the IC of Figure 10 by 1.0 A for every 250 ohms of RG below 1.0 $k\Omega$ for case temperatures greater than 65°C.



MGM20N45 MGM20N50 MGP20N45 MGP20N50

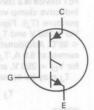
Designer's Data Sheet

N-CHANNEL ENHANCEMENT-MODE SILICON GATE, INSULATED GATE BIPOLAR TRANSISTOR

These GEMFETS are designed for high voltage, high current power controls such as line operated motor controls and converters.

- High Input Impedance
- Low On-Voltage, 2.7 V max @ 10 A
- High Peak Current Capability 30 A
- Voltage Driven Device





MAXIMUM RATINGSS

gnizeeroek diw zeniloeb to vol bellom Rating amit Ho-nn	Symbol	MGM20N45 MGP20N45	MGM20N50 MGP20N50	Unit
Collector-Emitter Voltage	VCES	450	500	Vdc
Collector-Gate Voltage $(R_{GS} = 1.0 \text{ M}\Omega)$	VCER	450	500	Vdc
Gate-Emitter Voltage Continuous Non-repetitive (t _p ≤ 50 μs)	V _{GE} V _{GEM}	22000000	20 40	Vdc Vpk
Collector Current Continuous Pulsed	I _C	20 30		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		00	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	R_{θ} JC	1.25	
Junction to Ambient	$R_{\theta JA}$	30(1)	
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	ga gaTLgs	275 as as	o, °C

(1) Add 32.5°C/W for MGP20N45 and MGP20N50.

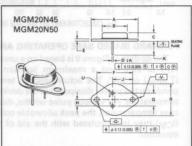
Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

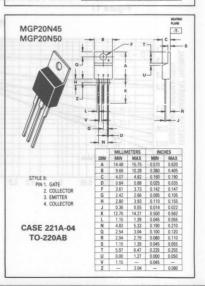
20 AMPERE

N-CHANNEL TMOS GEMFET

rCE(on) = 0.27 Ohm 450 and 500 Volts

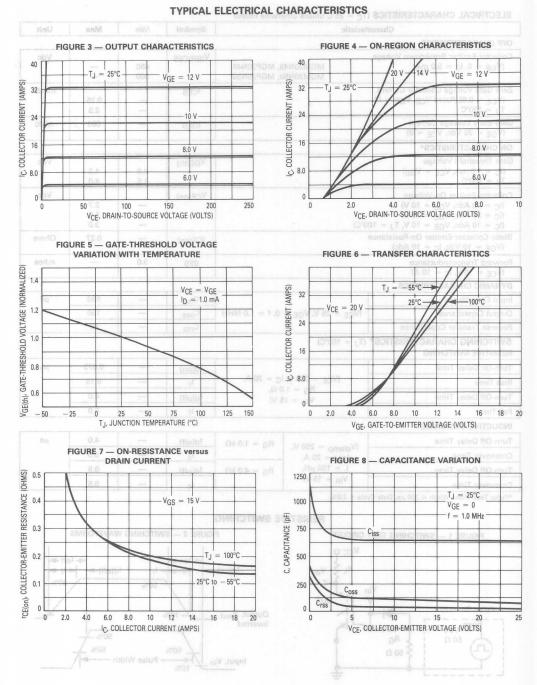


		MILLIN	METERS	INC	HES
	DIM	MIN	MAX	MIN	MAX
STYLE 6:	A	-	39.37	-	1.550
PIN 1. GATE	В	-	21.08	-	0.830
2. EMITTER	C	6.35	8.25	0.250	0.325
CASE COLLECTOR	D	0.97	1.09	0.038	0.043
	E	1.40	1.77	0.055	0.070
	F	30.15 BSC		1.187 BSC	
CASE 1-06	G	10.92 BSC		0.430 BSC	
TO-204AA	H	5.46	BSC	SC 0.215 B	
2000 000 000 000	J	16.89	BSC	0.665 BSC	
	K	11.18	12.19	0.440	0.480
	Q	3.84	4.19	0.151	0.165
	R	-	26.67	-	1.050
	U	4.83	5.33	0.190	0.210
	V	3.84	4.19	0.151	0.165



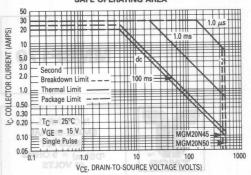
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

	cteristic		Symbol	Min	Max	Unit		
OFF CHARACTERISTICS	- A BILLIOR		ACTERISTICS	PUT CHAR	18E 3 OUT	EGR		
Collector-Emitter Breakdown Voltage (VGE = 0, IC = 5.0 mA)		5, MGP20N45 0, MGP20N50	V(BR)CES	450 500	F8S = <u>1</u> 1	Vdc		
Zero Gate Voltage Collector Current (VCE = 0.85 Rated VCE, VGE = 0) T.J = 100°C	- 3'88 A (1 - 35'C -	ICES		0.25 2.5	mAdc			
Gate-Body Leakage Current (VGE = 20 Vdc, VCE = 0)					500	nAdc		
ON CHARACTERISTICS*	CV 11 10 8		Vos			10		
Gate Threshold Voltage (I _C = 1.0 mA, V _{CE} = V _{GE}) T _J = 100°C	V _{GE(th)}	2.0 1.5	4.5 4.0	Vdc				
Collector-Emitter On-Voltage (I _C = 10 Adc, V _{GE} = 10 V) (I _C = 20 Adc, V _{GE} = 15 V) (I _C = 10 Adc, V _{GE} = 10 V, T _J = 100°C)			VCE(on)	OOI V BOR UO S OT	2.7 5.0 3.0	Vdc		
Static Collector-Emitter On-Resistance (V _{GE} = 10 Vdc, I _C = 10 Adc)	9 200 200		rCE(on)	E-THRESH	0.27	Ohms		
Forward Transconductance (V _{CE} = 10 V, I _C = 10 A)			9FS	3.0	1 1011	mhos		
DYNAMIC CHARACTERISTICS	10		Mor - Vox					
Input Capacitance			Ciss		950	pF		
Output Capacitance	(VCE = 25 V, VGE =	0, f = 1.0 MHz)	Coss	_	150	2		
Reverse Transfer Capacitance	4 景	C _{rss}	-	60				
SWITCHING CHARACTERISTICS* RESISTIVE SWITCHING	* (T _J = 100°C)							
Turn-On Delay Time			td(on)		0.075	μs		
Rise Time	(V _{CE} = 250 V, I _C = 20 A,		t _r	_	0.15	-		
Turn-Off Delay Time	$R_G = 1$ $V_{in} = 1$		td(off)	_	4.0	8.0		
Fall Time	1 20 40	125 150	nor t _f	6- 1	8.0			
INDUCTIVE SWITCHING	Rep. G		ION BRUTAS	CHON TEARER	MUL-LIT			
Turn-Off Delay Time		td(off)	_	4.0	μs			
Crossover Time	$V_{clamp} = 250 V,$ $V_{clamp} = 20 A,$	$R_G = 1.0 \text{ k}\Omega$	t _c	ATRIBER IN	6.0			
Turn-Off Delay Time	$L = 180 \mu H$	$R_G = 4.0 \text{ k}\Omega$	td(off)	QUISUO M	9.5			
Crossover Time	$V_{in} = 15 V$		t _C		9.5	30		
*Pulse Test: Pulse Width ≤ 300 μs, Duty C	cycle ≤ 2.0%.		V31 = 25V					
	RESISTIN	E SWITCHING						
FIGURE 1 — SWITCHING TES				WITCHING	WAVEFORMS	\$ C.		
Pulse Generator	VCC O RL Vout td(on) ton tr td(off) 90%							
Rgen 50 Ω RG 50 Ω		Inverted Input, V	50%	- Pulse Wid	90% 50%			



3

FIGURE 9 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable collector current (I_{CM}) may be calculated with the aid of the following equation:

$$I_{CM} = I_{C}(25^{\circ}C) \left[\frac{T_{J(max)} - T_{C}}{P_{D} \cdot R_{\theta JC} \cdot r(t)} \right]$$

where

 $I_C(25^{\circ}C)$ = the dc collector current at $T_C = 25^{\circ}C$ from Figure 9.

T_{J(max)} = rated maximum junction temperature

T_C = device case temperature

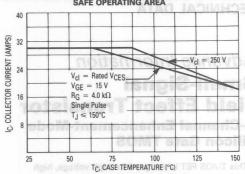
PD = rated power dissipation at T_C = 25°C

 $R_{\theta JC}$ = rated steady state thermal resistance

r(t) = normalized thermal response from

Figure 11

FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



SWITCHING SAFE OPERATING AREA

The switching safe operating area (SSOA) of a GEMFET device is a composite function of gate turn-off time, inductive clamp voltage (Vcl) and device junction temperature (T_J). Figure 10 illustrates that I_C is 30 A for Vcl \approx 250 V and T_J \approx 87.5°C, and for Vcl < 500 V and T_J < 62.5°C. Additionally, it is seen that for a peak collector current of 24 A, T_J must be maintained less than 118°C for Vcl = 250 V, and less than 106°C for Vcl = 500 V.

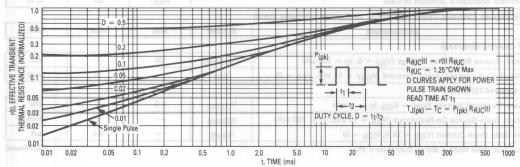
 $T_J = T_C + P_D R_{\theta J} C^{\bullet r}(t)$

where

P_D is the power averaged over a complete switching cycle.

Generally, SSOA current declines with decreasing gate turn-off time. Gate turn-off time is controlled by RG; lowering RG decreases gate turn-off time. A suggested rule-of-thumb is to derate the IC of Figure 10 by 25 A for every 1100 ohms of RG below 4.0 k Ω for case temperatures greater than 55°C.





Advance Information

Small-Signal Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate TMOS

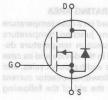
This TMOS FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

Silicon Gate for Fast Switching Speeds





N-CHANNEL SMALL-SIGNAL TMOS FET rDS(on) = 5 OHMS 60 VOLTS





CASE 318-02 SOT-23

MAXIMUM RATINGS upe ed most betslusted ed years T

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	60	Vdc
Gate-Source Voltage	VGS VGS	10130±20	Vdc
Drain Current — Continuous — — — — — — — — — — — — — — — — — — —	ID IDM	0.5	Adc (xsm)
Total Power Dissipation FR5 Board 1" x 0.75" x 0.62" Derate above 25°C	PD at TC = 28°C	550 4.4	mW mW/°C
Operating Temperature Range	mon eano. Jan ter	-55 to +125	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta}JC$	60	°C/W
ELECTRICAL CHARACTERISTICS (To = 25°C unless otherwise noted)			

Characteristic Symbol Min Max Unit OFF CHARACTERISTICS Drain-Source Breakdown Voltage (VGS = 0, ID = 100 μ A) V(BR)DSS 60 — Vdc Gate-Body Leakage Current, Forward (VGSF = 15 Vdc, VDS = 0) IGSS — 10 nAdc ON CHARACTERISTICS* Gate Threshold Voltage (VDS = VGS, ID = 1 mA) VGS(th) 0.8 3 Vdc

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA)	VGS(th)	0.8	3	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 200 mA)	rDS(on)		10.0 5	Ohm
On-State Drain Current (V _{DS} = 25 V, V _{GS} = 0)	ID(off)	- 1	0.5	μΑ

^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (TC = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
DYNAMIC CHARACTERISTICS					
Input Capacitance (V _{DS} = 10 V, V _{GS} = 0 V, f =	1 MHz)	C _{iss}	matic	60	o pF
SWITCHING CHARACTERISTICS*			16	mois	-Hs
Turn-On Delay Time	(V _{DD} = 25 V, I _D = 500 mA,	td(on)	arran 8° d	10	ns
Turn-Off Delay Time	R _{gen} = 50 Ohms) Figure 1	td(off)	DE NE C	10	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

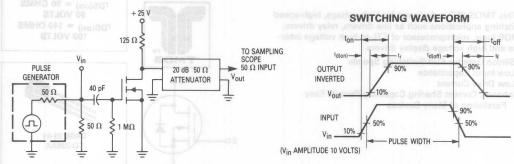
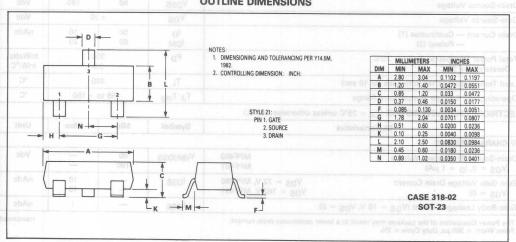


Figure 1. Switching Test Circuit

OUTLINE DIMENSIONS



Advance Information

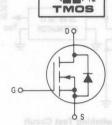
Small-Signal Field Effect Transistor

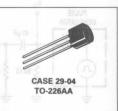
N-Channel Enhancement-Mode Silicon Gate TMOS

This TMOS FET is designed for high-voltage, high-speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor of TTL-to-high voltage interface and high voltage display drivers.

- Silicon Gate for Fast Switching Speeds
- Low Input Capacitance
- Low Drive Current
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

SMALL-SIGNAL N-CHANNEL **TMOS FETs** rDS(on) = 80 OHMS 80 VOLTS rDS(on) = 140 OHMS 180 VOLTS





MAXIMUM RATINGS

AND THE				
Rating	Symbol	MPF480	MPF481	Unit
Drain-Source Voltage	V _{DSS}	80	180	Vdc
Gate-Source Voltage	VGS	±	± 20	
Drain Current — Continuous (1) — Pulsed (2)	I _D	50 80	10 20	nAdc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		50	mWatts mW/°C
Lead Temperature (1/16" from case for 10 sec)	TL	3	00	°C
Operating and Storage Temperature Range	TJ, T _{stg}	-55 to	+ 150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

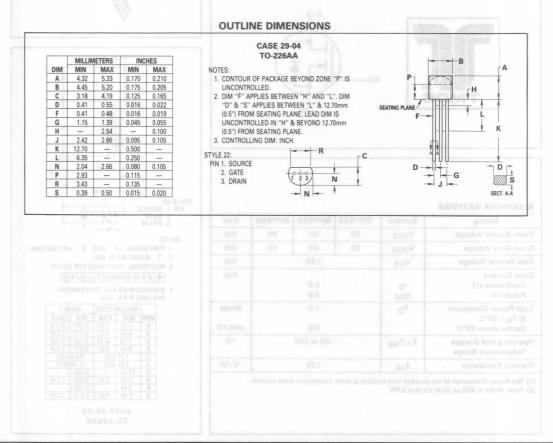
Characteristics		Symbol	Min	Max	Unit
OFF CHARACTERISTICS	2000		140	0	1000
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 1 μA)	MPF480 MPF481	V(BR)DSS	80 180		Vdc
Zero Gate Voltage Drain Current (VGS = 0)	V _{DS} = 72 V, MPF480 V _{DS} = 162 V, MPF481	IDSS	(I)	10 10	nAdc
Gate-Body Leakage Current (VGS = 15 V, VDS = 0))	IGSS	_	1	nAdc

(1) The Power Dissipation of the package may result in a lower continuous drain current. (2) Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Characteristics		Symbol	Min	Max	Unit
N CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = 3 V, I _D = 10 μA)		VGS(th)	0.5	3	Vdc
Static Drain-Source On Resistance (V _{GS} = 10 V, I _D = 10 mA)	MPF480 MPF481	rDS(on)	-	80 140	Ohm
On-State Drain Current (V _{DS} = 10 V, V _{GS} = 10 V)	MPF480 MPF481	ID(on)	50 10	TMOS	mA
Forward Transconductance (V _{DS} = 15 V, I _D = 10 mA)	ed switching appli-	9fs	8 ere designi	TMOS FETS	mmhos
APACITANCE	US logic, micropro-	r supplies, UM a and line delv			
Input Capacitance (V _{GS} = 0, V _{DS} = 10 V, f = 1 MHz)		C _{iss}	_	8	pF
Reverse Transfer Capacitance (V _{DS} = 0 V, V _{GS} = 0 V)	clo	C _{rss}		witdl y ng Spa en-Nasistang	les.
WITCHING CHARACTERISTICS	and MPF990	m typ MPF980	1.2 Olu		
Turn-On Time $(\text{V}_{DD} = 25 \text{ V, I}_{D} = 50 \text{ mA, R}_{L} = 500 \ \Omega, \text{R}_{G} = 50$	Easy Faralleling of $(\Omega$	t(on)	ment_VGS(haring Cap	20	ns
Turn-Off Time $(V_{DD} = 25 \text{ V}, I_{D} = 50 \text{ mA}, R_{L} = 500 \Omega, R_{G} = 50$	Ω)	t(off)	_	20	ns

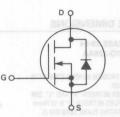


N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

These TMOS FETs are designed for high-speed switching applications such as switching power supplies, CMOS logic, microprocessor or TTL to current interface and line drivers.

- Fast Switching Speed ton = toff = 7.0 ns typ
- Low On-Resistance 0.9 Ohm typ MPF930
 - 1.2 Ohm typ MPF960 and MPF990
- Low Drive Requirement, VGS(th) = 3.5 V max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices





MAXIMUM RATINGS

Rating	Symbol	MPF930	MPF960	MPF990	Unit
Drain-Source Voltage	V _{DSS}	35	60	90	Vdc
Drain-Gate Voltage	V _{DGO}	35	60	90	Vdc
Gate Source Voltage	VGS	±30			Vdc
Drain Current Continuous (1) Pulsed (2)	I _D	2.0 3.0			Adc
Total Power Dissipation @ T _A = 25°C Derate above 25°C	PD	1.0		Watts mW/°C	
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C	
Thermal Resistance	θЈΑ	125			°C/W

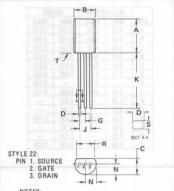
- (1) The Power Dissipation of the package may result in a lower continuous drain current.
- (2) Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

2.0 AMPERE

N-CHANNEL TMOS FETs

35, 60, 90 VOLTS





NOTES:

- 1. DIMENSIONS -A- AND -B- ARE DATUMS.
- 2. -T- IS SEATING PLANE.
- 3. POSITIONAL TOLERANCE FOR LEADS:

♦ Ø 0.10 (0.004) M T A M B M

4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIM	ETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	7.37	7.87	0.290	0.310
В	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.46	0.61	0.018	0.024
G	1.27	BSC	0.050	BSC
J	2.54	BSC	0.100	BSC
K	12.70	-	0.500	-
N	2.03	2.92	0.080	0.115
R	3.43	-	0.135	-
S	0.46	0.61	0.018	0.024

CASE 29-03 TO-226AE

Characteristic		Symbol	Min	Тур	Max	Unit	9 0
OFF CHARACTERISTICS		1087					1
Drain-Source Breakdown Voltag	ge	V(BR)DSS				Vdc	
$(V_{GS} = 0, I_{D} = 10 \mu A)$ MPF930	/	35					
	MPF960	F ON S	60		_		
	MPF990	Hosr 8 L	90	_			
Zero Gate Voltage Drain Curren	t /	IDSS			10	μAdc	
(VDS = Maximum Rating, Vo	is = 0)	1 2					1
Gate-Body Leakage Current	1	IGSS			50	nAdc	18
(Vac = 15 Vdc Vac = 0)		-A 08 - 1					

$(V_{GS} = 15 \text{ Vdc}, V_{DS} = 0)$		7 100 0				
ON CHARACTERISTICS*	223	- 00				.02
Gate Threshold Voltage (ID = 1.0 mA, VDS = VGS)		VGS(th)	1.0		3.5	Vdc
Drain-Source On-Voltage (VGS = (ID = 0.5 A)		VDS(on)	=	0.4 0.6 0.6	0.7 0.8 1.0	Vdc
(I _D = 1.0 A)	MPF930 MPF960 MPF990	25	DITRIRG	0.9 1.2 1.2	1.4 1.7 2.0	24 VOS = 10 V
(I _D = 2.0 A)	MPF930 MPF960 MPF990	ENT 128		2.2 2.8 2.8	3.0 3.5 4.0	1.5
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 1.0 Adc)	MPF930 MPF960 MPF990	r _{DS(on)}	=	0.9 1.2 1.2	1.4 1.7 2.0	Ohms gr
On State Drain Current (VDS = 25 V, VGS = 10 V		ID(on)	1.0	2.0	(E)	Amps

Forward Transconductance $(V_{DS} = 25 \text{ V}, I_{D} = 0.5 \text{ A})$ **DYNAMIC CHARACTERISTICS**

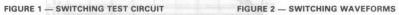
Input Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz)	C _{iss}	-	60	70	pF
Output Capacitance (VDS = 25 V, VGS = 0, f = 1 MHz)	Coss	E 7 — SAT	AUDR 49	60	pF
Reverse Transfer Capacitance (VDS = 25 V, VGS = 0, f = 1 MHz)	Crss		13	18	pF

SWITCHING CHARACTERISTICS*

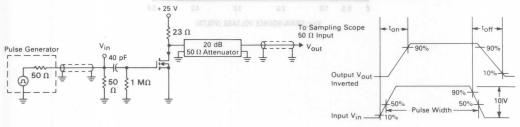
Turn-On Time See Figure 1	ton	7.0	15	ns
Turn-Off Time See Figure 1	toff	7.0	15	ns

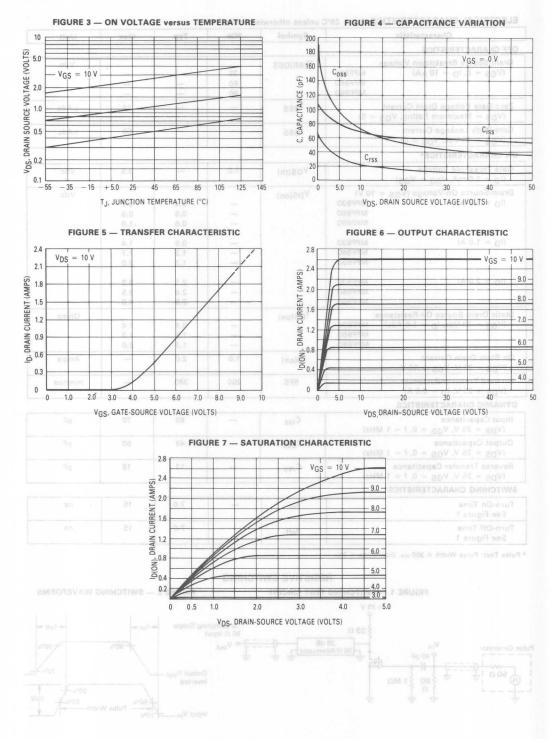
^{*} Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

RESISTIVE SWITCHING



mmhos





Advance Information

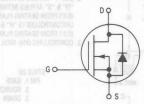
Small-Signal Field Effect Transistor Silicon Gate TMOS

- Normally Closed Relay
- Telephone Line Switching
- Fail Safe Systems
- Current Regulator Circuits





625 mW TMOS FET rDS(on) = 12 OHMS 150 VOLTS N-CHANNEL **DEPLETION MODE**



MAXIMUM RATINGS

Rating	Symbol	Value	Unit	
Drain-Source Voltage	VDS	150	Vdc	
Drain-Gate Voltage	V _{DG}	150	Vdc	
Drain Current — Continuous — Pulsed (1)	I _D	250 500	mA	
Total Device Dissipation @ T _A = 25°C Derate above 25°C	PD	625 5	mW mW/°C	
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150	°C	



CASE 29-04 TO-226AA PLASTIC PACKAGE

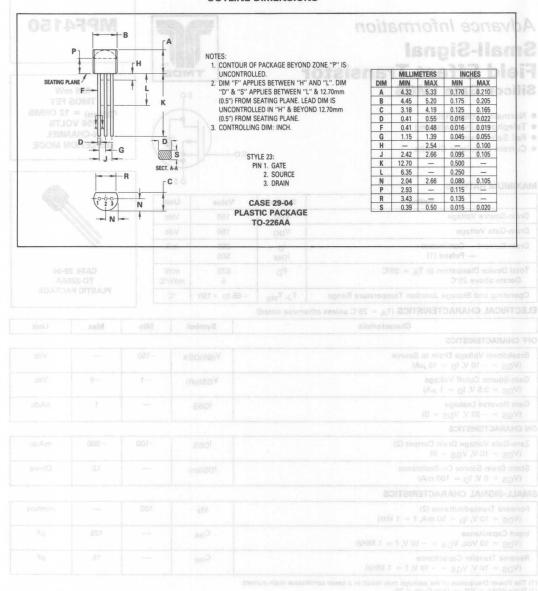
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS				
Breakdown Voltage Drain to Source (VGS = -10 V, ID = $10~\mu$ A)	V(BR)DSX	-150	_	Vdc
Gate-Source Cutoff Voltage (V _{DS} = 3.5 V, I _D = 1 μ A)	VGS(off)	-1	-6	Vdc
Gate Reverse Leakage (V _{GS} = -20 V, V _{DS} = 0)	IGSS	-	1	nAdc
N CHARACTERISTICS				
Zero-Gate Voltage Drain Current (2) (V _{DS} = 10 V, V _{GS} = 0)	IDSS	-100	- 800	mAdc
Static Drain-Source On-Resistance (VGS = 0 V, I _D = 100 mA)	rDS(on)	-	12	Ohms
MALL-SIGNAL CHARACTERISTICS				
Forward Transadmittance (2) $(V_{DS} = 10 \text{ V, } I_{D} = 50 \text{ mA, } f = 1 \text{ kHz})$	Yfs	100	-	mmhos
Input Capacitance (VDS = 10 Vdc, V GS = -10 V, f = 1 MHz)	C _{iss}	_	125	pF
Reverse Transfer Capacitance	C _{rss}	_	15	pF

⁽¹⁾ The Power Dissipation of the package may result in a lower continuous drain current. (2) Pulse Width \leqslant 300 μ s, Duty Cycle \leqslant 2%.

 $(V_{DS} = 10 \text{ V}, V_{GS} = -10 \text{ V}, f = 1 \text{ MHz})$

This document contains information on a new product. Specifications and information herein are subject to change without notice.



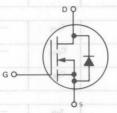
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N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

This TMOS FET is designed for high voltage, high speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor or TTL to high voltage interface and high voltage display drivers.

- Fast Switching Speed ton = toff = 6.0 ns typ
- Low On-Resistance 4.5 Ohms typ
- Low Drive Requirement, VGS(th) = 4.0 V max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices





MAXIMUM RATINGS

PROVINCE A - SWITTER WAVEVORMS	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	200	Vdc
Gate-Source Voltage	VGS	±20	Vdc
Drain Current — Continuous (1) Pulsed (2)	I _D	400 800	mAdc
Total Power Dissipation @ T _A = 25°C Derate above 25°C	PD	0.6 4.8	Watts mW/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C
Thermal Resistance Junction to Ambient	θΔΑ	208	°C/W

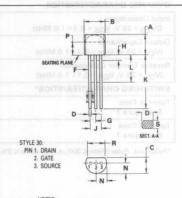
(1) The Power Dissipation of the package may result in a lower continuous drain current.

(2) Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

200 VOLTS

N-CHANNEL TMOS FET V AGO





- VOTES:

 1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS

 UNCONTROLLED.

 2. DIM "" APPLIES BETWEEN "H" AND "L". DIM
 "D" & "S" APPLIES BETWEEN "L" & 12.70mm
 (0.5") FROM SEATING PLANE. LEAD DIM IS

 UNCONTROLLED IN "I" & BEYOND 12.70mm
 (AST INDIA ASTRUM) ALGERIA DIA IS
- (0.5") FROM SEATING PLANE.
 3. CONTROLLING DIM: INCH.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.32	5.33	0.170	0.210
В	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
Н	-	2.54	-	0.100
J	2.42	2.66	0.095	0.105
K	12.70	-	0.500	-
L	6.35	-	0.250	_
N	2.04	2.66	0.080	0.105
P	2.93	_	0.115	_
R	3.43	_	0.135	_
S	0.39	0.50	0.015	0.020

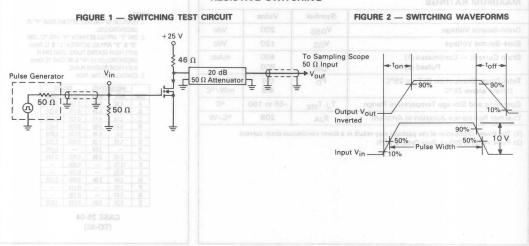
CASE 29-04 (TO-92)

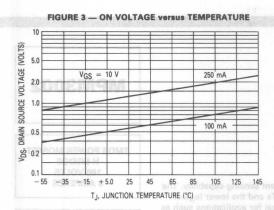
ELECTRICAL	CHARACTERISTICS	(TA = 25°C unless otherwise note	d.)

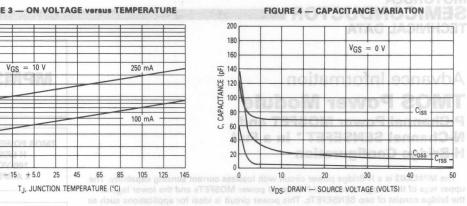
Characteristic		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 10 μA)		V(BR)DSS	200	-1	_	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 200 V, V _{GS} = 0)		IDSS	_	0.1	10	μAdc
Gate-Body Leakage Current (V _{GS} = 15 Vdc, V _{DS} = 0)		IGSS	-	0.01	50	nAdc
ON CHARACTERISTICS*		BULSISIA	ART TOAS:	19.0 JUNE	ROMT	
Gate Threshold Voltage (I _D = 1.0 mA, V _{DS} = V _{GS})		V _{GS(th)}	1.0	_	4.0	Vdc
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 100 mA)	swaching micropro-	V _{DS(on)}	r high voltar rela <u>y d</u> rivers		88 d 0.6 878	Vdc
(I _D = 250 mA) (I _D = 500 mA)	ge display	id high volta	interface a	3.0	1.60 T	sessor o drivers.
On State Drain Current (V _{DS} = 25 V, V _{GS} = 10 V		ID(on)	400	700	8 onidativi	mA
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc) (I _D = 100 mA) (I _D = 250 mA) (I _D = 500 mA)		rDS(on) max mits Easy P	S(tin)=4.0 N			1
Forward Transconductance (V _{DS} = 25 V, I _D = 250 mA)		9FS	200	400	_	mmhos
DYNAMIC CHARACTERISTICS		90		processors and a		7
Input Capacitance OV _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)	1	C _{iss}	-	72	90	pF
Output Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)		Coss	_	15	20	pF
Reverse Transfer Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)	1	C _{rss}	-0 -	2.8	3.5	pF
SWITCHING CHARACTERISTICS*				Can Carl	EAS 1	
Turn-On Time See Figure 1		ton	-	6.0	15	ns
Turn-Off Time See Figure 1		toff	-	12	15	ns

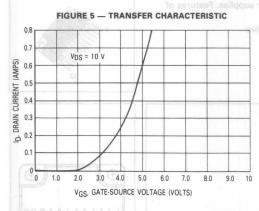
^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

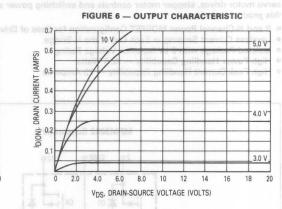
RESISTIVE SWITCHING

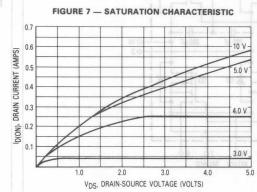












Advance Information

TMOS Power Module

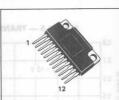
P-Channel Power MOSFET and N-Channel SENSEFET™ in a Full H-Bridge Configuration

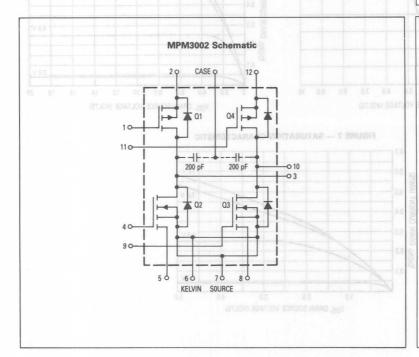
The MPM3002 is a H-Bridge power circuit with lossless current sensing capability. The upper legs of the bridge consists of P-Channel power MOSFETs and the lower legs of the bridge consist of two SENSEFETs. This power circuit is ideal for applications such as servo motor drives, stepper motor controls and switching power supplies. Features of this product include:

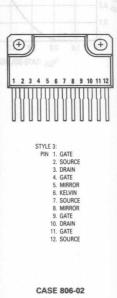
- P and N-Channel Power MOSFET Configuration for Ease of Drive
- Lossless Current Sensing in Each Leg of the H-Bridge
- Isolated Package with 2 kV Isolation Voltage Rating
- High Power Handling Capability 62.5 Watts
- High Peak Current Handling Capability 25 Amperes



TMOS POWER MOSFET
H-BRIDGE
100 VOLTS
8 AMPERES







This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

	Rat	ing	Symbol	Value	Unit
Drain-to-So	urce Voltage	(All Types)	V _{DSS}	100	Volts
Drain-to-Ga	te Voltage (RGS = $1M\Omega$)	(All Types)	VDGR	100	Drain-to-Sol
Gate-to-Sou	rce Voltage — Continuous — Non-repetitive	P. Carlotte and C. Carlotte an	V _{GS} V _{GSM}	± 20 ± 40	Volts Vpk
Drain-to-Mir	rror Voltage	(Q2 and Q3)	V _{DM}	100	Volts
Gate-to-Mire	ror Voltage	(Q2 and Q3)	VGM	± 20	Drain-to-Ser
Drain Curre	nt — Continuous — Pulsed	(Q2 and Q3)	I _D	12 30	Amps
Ninos	— Continuous — Pulsed	(Q1 and Q4) (80 bns 80)	I _D	8 25	Forward Tra (Vps = 1)
Mings	— Continuous — Pulsed	(N/P-Channel Combination)	I _D		Forward Tru (Vps = 1
Sense Curre	ent — Continuous — Pulsed	(Q2 and Q3) (Vino EO bns EO)	IM IMM	13 A 33	Am MA
RMS Isolation	on Voltage	(Any Pin to Case)	VISO	2000	Volts
Operating a	nd Storage Temperature Rang	ge 12	T _J , T _{stq}	-40 to 150	oags3°C anl

THERMAL CHARACTERISTICS

Power Dissipation — T _C = 25°C (Any single device)	PD	62.5	Watts
(Q1 and Q3 or Q1 and Q4 or Q2 and Q3 or Q2 and Q4 "On") (Q1 and Q2 and/or Q3 and Q4 "On")		62.5	Turn-On Dela
Power Derating — Derate above T _C = 25°C (Any single device) (Q1 and Q3 or Q1 and Q4 or Q2 and Q3 or Q2 and Q4 "On") (Q1 and Q2 and/or Q3 and Q4 "On")	1/R _θ JC	0.5 0.5 0.25	W/°C
Thermal Resistance — Junction to Case — Junction-to-Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2 35	°C/W
Thermal Coupling Coefficient (Q1 to Q2 or Q4 to Q3) See Table 1 (Q1 to Q3, Q1 to Q4, Q2 to Q3 or Q2 to Q4)	α β	0.5 0.01	t) nier0 - rs0
Maximum Lead Temperature for Soldering Purposes 1/8" from case for 5 seconds	TL	260	Cure-On Dear

ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{MS} = 0 unless otherwise noted)

Characteris	tics		Symbol	Min	Тур	Max	Unit
FF CHARACTERISTICS	1/					90	RH HEY-
Drain-to-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	500	(All Devices)	V _{(BR)DSS}	100	6 6 9 1	ata <u>C</u> harg ource Cha	Vdc
Drain-to-Mirror Breakdown Voltage (VGS = 0, I _D = 0.25 mA)	DgO	(Q2 and Q3)	V(BR)DMS	100	- 9 AHO 200	rain -C han	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 80 V, V _{GS} = 0) (V _{DS} = 80 V, V _{GS} = 0, T _J = 125°C)	VSD	(Any Single Device)	IDSS	=	888 17	0.2	mAdd
Gate-Body Leakage Current — Forward (VGSF = 20 Vdc, VDS = 0)	117	(Any Single Device)	IGSSF	electrons	y Ti m e one caa	100	nAdc
Gate Body Leakage Current — Reverse (VGSR = 20 Vdc, VDS = 0)	dsV	(Any Single Device)	IGSSR	-	epe	100	Fonsa
N CHARACTERISTICS*	rior	[A 8 =	311		(983)11	Ormet b	iswied.
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mAdc) (T _J = 125°C)	117	(Any Single Device)	VGS(th)	2	3	4.5 3.5	Vdc
Static Drain-to-Source On-Resistance (VGS = 10 Vdc, ID = 4 Adc)	o inacter	(Q2 and Q3)	rDS(on)	prist <u>iab</u> rii T t sannin ud	Finding of Fig.	0.15	Ohms
Static Drain-to-Mirror On-Resistance (VGS = 10 Vdc, ID = 4 Adc)		(Q2 and Q3)	rDM(on)	_	-	140	Ohms

(continued)

ELECTRICAL CHARACTERIST	CS — continued (T.)	= 25°C, VMS	= 0	unless otherwise noted)
--------------------------------	---------------------	-------------	-----	-------------------------

Value Unit	Characteristics			Symbol	Min	Тур	Max	Unit
N CHARACTERISTICS*								
Drain-to-Source On-Voltage	(VGS = 10 Vdc)	(Q2 and Q3)	(283)	VDS(on)	(QMt =	age (Ros	date Vol	Vdc
$(I_D = 8 A)$ $(I_D = 4 A, T_J = 125^{\circ}C)$				yF IIA)	ontimious	htag <u>a</u> — 0	1.2	l-or-erai
Static Drain-to-Source On-Resistance (Q1 and Q4) (VGS = 10 Vdc, ID = 4 Adc)				rDS(on)	GSQ81-NO	itage	0.4	Ohm
Drain-to-Source On-Voltage	(ED t	V _{DS(on)}		lage	oV ramily	Vdc		
$(I_D = 8 A)$ $(I_D = 4 A, T_J = 125^{\circ}C)$	al Mai			(Q.2 an	=	iontinuou leised	3.2 3.2	rain Cu
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 4 A	dc)	(Q2 and Q3)		9FS	3	Jontinuous Pulsed		Mho
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 4 A	dc)	(Q1 and Q4)	ennal Cor	9FS	2	ontinuou ulsed) —	Mho
Current Mirror Ratio (Cell Ratio (RSENSE = 0, ID = 8 A, V		(Q2 and Q3 only)	(50)	na so)n	750	Continuos Pulsed	850	io os Tie
YNAMIC CHARACTERISTICS	(All Types)		n to Case	(Anv Pi		enet	loV noite	lool 2Mil
Input Capacitance		(V _{DS} = 25 V, V _{GS} = 0			en Tores	nel soci	900	pF
Output Capacitance	(VDS				-		450	to to torce
Transfer Capacitance	f = 1 MHz)			C _{oss}	801	Oliva i Os	200	RIVINIS
WITCHING CHARACTERISTIC	S* (N-Channel, C	02 and Q3)			13490	(ep)	ingle dev	a vnA)
Turn-On Delay Time			''.O'' #D	td(on)	or <u>02</u> an	D bns 10	30	ns
Rise Time	(Vpr	(V== = 25 V l= = 4.4			n0" +0 1	ne 60 tol	130	a (0)
Turn-Off Delay Time		$(V_{DD} = 25 \text{ V}, I_D = 4 \text{ A})$ $R_{gen} = 50 \text{ Ohms})$		t _r	OT over	Dorete e	120	rewol
Fall Time		("#0" \$0			ne <u>20</u> 10	11 a <u>nd</u> Q4	125	ns (O)
Total Gate Charge				t _f	Inol No t	38	45	nC
Gate-Source Charge	$(V_{DS} = 80 \text{ V}, I_{D} = 8 \text{ A})$			Q _{gs}	tion to Ca	15	Resistant	narma
Gate-Drain Charge	700-	V _{GS} = 10 V)			es tem es	23	sellame?	lsmrad"
10.0	1	or 02 to 04)	Q2 to Q3	Q _{gd}	or (O)	BINESON	Logging I pide	See T
WITCHING CHARACTERISTIC	S* (P-Channel, U	11 and Q4)		paragrafi grine	VIUG JUT 6	esta respirite	T beggt m	printage
Turn-On Delay Time				^t d(on)	abi	от Б весоя	25	ns
Rise Time	(VDI	0 = 25 V, ID = 4 A		tr	n corre	HOTOAN	130	ECTR
Turn-Off Delay Time	nitV lodm	R _{gen} = 50 Ohms)			(Operation	-	40	
Fall Time				tf		9011	60	NO T
Total Gate Charge	Who Who	2 = 80 V Ip = 8 A		Qg	Voltage	23	30	nC
Gate-Source Charge	$(V_{DS} = 80 \text{ V}, I_{D} = 8 \text{ A})$ $V_{GS} = 10 \text{ V}$			Qgs		Am 10.0	nio e	(Ves
Gate-Drain Charge	100 I 100		(ED bns	O Q _{gd}	RostoV	13	a ro ttilyl-	Drain-to
OURCE-DRAIN DIODE CHAR						Am 85.0 =	01.0 =	(Ves
Forward On-Voltage	380	(IS = 8 A)		V _{SD}	tosm	1.2	ite Voltag	Vdc
Forward Turn-On Time				ton (3	1.25	25	. V 08 =	ns
Reverse Recovery Time	- 1 788F	Device) la	signi2 y	(A) trr by	Wio T —	155	ede T vb e	Gata-Br
OURCE-DRAIN DIODE CHAR	ACTERISTICS (P-0	Channel, Q1 and Q4)			(0	do, Vps =	t = 20 V	SOAI
Forward On-Voltage	HSSR			V _{SD}	1— <u>B</u> ever	nemi40 eg	adea Lybe	Vdc
Forward Turn-On Time	(I _S = 8 A)		ton	- 10	25	a na - b	ns	
Reverse Recovery Time	transal testing to the			t _{rr}		150	0.713 1.074	N CHA
*Indicates Pulse Test: Pulse Width Note 1: Handling precautions to pr Note 2: Do not use the mirror FET Note 3: It is recommended that the	rotect against electro	ostatic discharge is mai	merchanic entre			Am I = Ql	ed.	

TYPICAL CHARACTERISTICS

N-CHANNEL

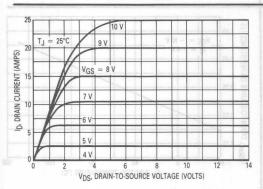


Figure 1. On-Region Characteristics

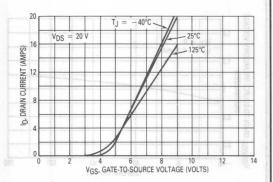


Figure 3. Transfer Characteristics

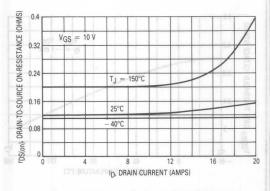


Figure 5. On-Resistance versus Drain Current

P-CHANNEL

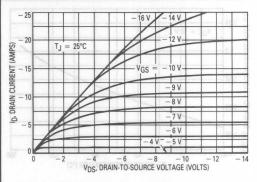


Figure 2. On-Region Characteristics

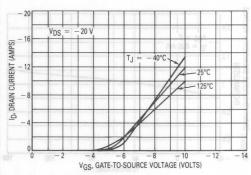


Figure 4. Transfer Characteristics

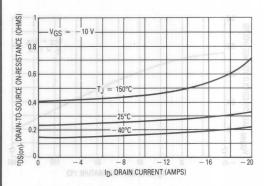


Figure 6. On-Resistance versus Drain Current

TYPICAL CHARACTERISTICS

N-CHANNEL 0.24 VGS = 10 V ID = 4 A 0.10 0.1

Figure 7. On-Resistance Variation with Temperature

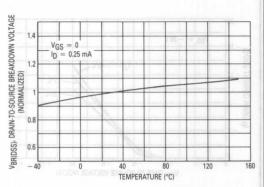


Figure 9. Drain-To-Source Breakdown Voltage Variation

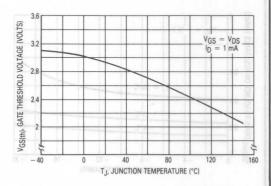


Figure 11. Gate Threshold Voltage Variation with Temperature

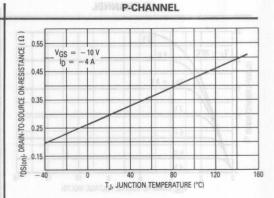


Figure 8. On-Resistance Variation with Temperature

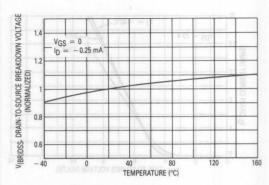


Figure 10. Drain-To-Source Breakdown Voltage Variation

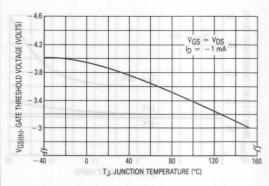


Figure 12. Gate Threshold Voltage Variation with Temperature

TYPICAL CHARACTERISTICS

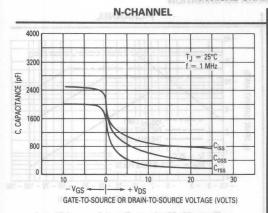


Figure 13. Capacitance Variation

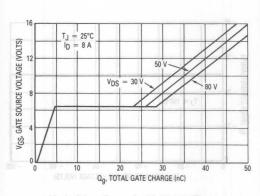


Figure 15. Stored Charge Variation

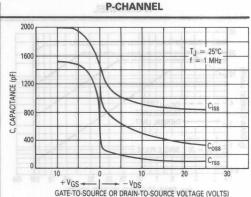


Figure 14. Capacitance Variation

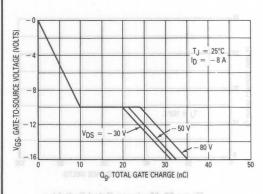


Figure 16. Stored Charge Variation

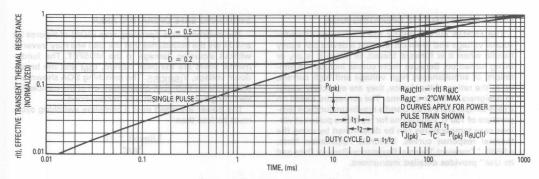


Figure 17. Thermal Response

3

SAFE OPERATING AREA INFORMATION

N-CHANNEL

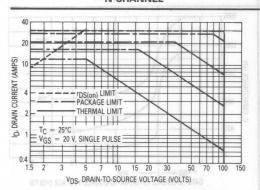


Figure 18. Maximum Rated Forward Biased Safe Operating Area

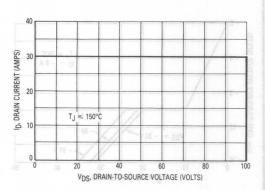


Figure 20. Maximum Rated Switching Safe Operating Area

P-CHANNEL

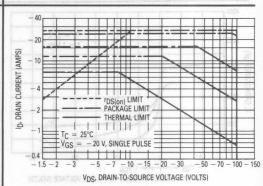


Figure 19. Maximum Rated Forward Biased Safe Operating Area

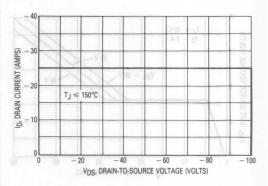


Figure 21. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, ANS69, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

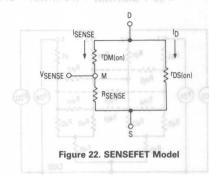
The switching safe operating area (SOA) of Figures 20 and 21 are the boundaries that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown are applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

 $T_{J(max)} - T_{C}$ $R_{\theta JC}$

The MPM3002 consists of two n-channel and reTESENSE BRISU used, assume that devices 01 and 0.3 are dissi

In practical applications, less sense current will flow than that calculated by using the current mirror ratio, n. Shown in Figure 22 is a model of the SENSEFET. It is seen that RSENSE decreases the voltage across rDM(on) and decreases the sense current. An additional decrease



in sense current occurs due to the decreased voltage across the mirror transistors. For this reason, a modified current mirror ratio, n' must be calculated. The equation to calculate n' is derived from the MOSFET square law model in the linear region,

$$n' = \frac{n}{1 - \frac{V_{SE}(V_{GS} - V_{T} - 1/2 \ V_{SE})}{V_{DS(on)}(V_{GS} - V_{T} - 1/2 \ V_{DS(on)})}}$$

$$n' \approx \frac{n}{1 - V_{SE}/V_{DS(on)}}$$
(1)

(for VSE, VDS(on) << VGS - VT).

Where, V_{GS} = Gate-to-Source Voltage, V_T = Gate-to-Source Threshold Voltage

and
$$V_{SE}$$
 = Sense Voltage = $\frac{RSENSE \mid D}{n'}$. (2)

Hence, n' can be calculated from equation (1) and the result used in equation (2) to find the value of RSENSE. The value of RSENSE should be kept below 100 Ω for most accurate results.

These equations were derived using die level source as the ground reference, neglecting contact and wire bond resistance to the source pin. In practice these parasitic resistances can cause significant errors at high currents, therefore it is mandatory to reference the gate drive signal and measure VDS(on) and VSENSE with respect to the Kelvin pin.

Figure 23 shows the sense voltage versus drain current for various values of RSENSE.

Figure 24 illustrates the correct SENSEFET configuration.

Figure 25 shows a typical current sensing circuit with a SENSEFET.

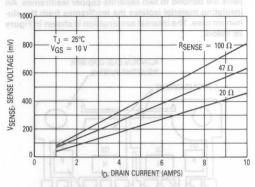


Figure 23. Sense Voltage versus Drain Current

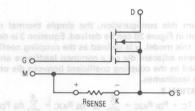
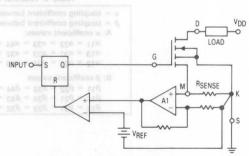


Figure 24. SENSEFET Configuration



Set A1 gain to match sense voltage to $V_{\mbox{REF}}$ at max $I_{\mbox{D}}$.

Figure 25. Typical Current Sensing with a SENSEFET

26 below.

3

ALUMINUM CASE CLAD WITH INSULATING MATERIAL COPPER LEADFRAME 03

Figure 26. Internal Construction of the MPM3002

P-CHANNEL POWER

MOSFET DIE

From this configuration, the simple thermal model shown in Figure 26 can be derived. Equation 3 is derived from this model. α is defined as the coupling coefficient between adjacent die on a common leadframe and β is defined as the coupling coefficient between die on separate leadframes.

EQUATION 3.

N-CHANNEL

SENSEFET

T_{Ji} = T_C + P_{Di} R<sub>$$\theta$$
JC</sub> + $\sum_{i=1}^{4} \alpha_{ik}$ P_{Dk} R _{θ} JC + $\sum_{i=1}^{4} \beta_{ik}$ P_{Dk} R _{θ} JC

 α and β values for different die combinations are listed in the maximum ratings. As an example of how the equation is used, assume that devices Q1 and Q3 are dissipating 10 watts each at a case temperature of 25°C, then calculate the junction temperature of Q1 and Q4.

FROM EQUATION 3,

$$T_{J1} = T_C + P_{D1}R_{\theta JC} + \beta_{13} P_{D3}R_{\theta JC}$$

= 25 + (10)(2) + (0.01)(10)(2) = 47°C

 $T_{J4} = T_C + \alpha_{43}P_{D3}R_{\theta JC} + \beta_{41}P_{D1}R_{\theta JC}$ = 25 + (0.5)(10)(2) + (0.01)(10)(2) = 37°C.

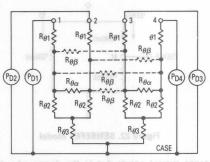


Figure 27. Thermal Model of the MPM3002

 $R_{\theta 1}$ = junction to leadframe thermal resistance

 $R_{\theta 2}$ = leadframe to isolator thermal resistance

 $R_{\theta 3}$ = isolator to case thermal resistance

= coupling thermal resistance between adjacent die on common leadframe

 $R_{\theta\beta}$ = coupling thermal resistance between die on separate leadframes

 $R_{\theta JC} = R_{\theta 1} + R_{\theta 2} + R_{\theta 3}$

Table 1. Thermal Coupling Coefficients actual of the state of the stat

 α = coupling coefficient between adjacent die on same leadframe β = coupling coefficient between die on separate leadframes A: α coefficient values: $\alpha_{11} = \alpha_{22} = \alpha_{33} = \alpha_{44} = 0$ $\alpha_{13} = \alpha_{31} = \alpha_{23} = \alpha_{32} = \alpha_{14} = \alpha_{41} = \alpha_{24} = \alpha_{42} = 0$ $\alpha_{12} = \alpha_{21} = \alpha_{34} = \alpha_{43} = 0.5$

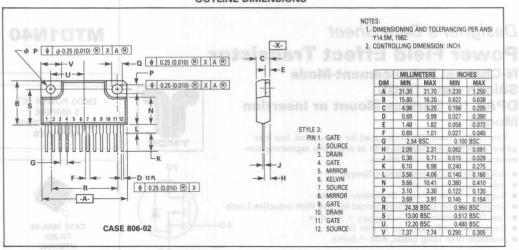
B: β coefficient values

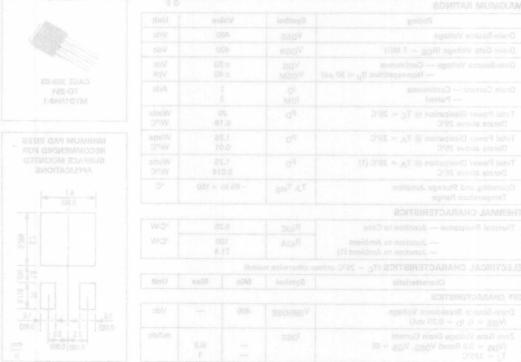
 $\beta_{11} = \beta_{22} = \beta_{33} = \beta_{44} = 0$ $\beta_{12} = \beta_{21} = \beta_{34} = \beta_{43} = 0$

 $\beta_{13} = \beta_{31} = \beta_{23} = \beta_{32} = \beta_{14} = \beta_{41} = \beta_{24} = \beta_{42} = 0.01$

MOTOROLA TMOS POWER MOSFET DATA

OUTLINE DIMENSIONS





MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS DPAK for Surface Mount or Insertion Mount

This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low ${\rm rDS(on)}-5~\Omega$ max
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement VGS(th) = 4 V max
- Surface Mount Package on 16 mm Tape
- Available With Long Leads, Add -1 Suffix

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	400	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	V _{DGR}	400	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	I _D		
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	20 0.16	Watts W/°C
Total Power Dissipation @ T _A = 25°C Derate above 25°C	PD	1.25 0.01	Watts W/°C
Total Power Dissipation @ T _A = 25°C (1) Derate above 25°C	PD	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	6.25	°C/W
 Junction to Ambient 	$R_{\theta JA}$	100	°C/W
 Junction to Ambient (1) 		71.4	

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	V _{(BR)DSS}	400	_	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 0) T _J = 125°C	IDSS	=	0.2	mAdd

(1) These ratings are applicable when surface mounted on the minimum pad size recommended. (continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MTD1N40

TMOS POWER FET 1 AMPERE rDS(on) = 5 OHMS 400 VOLTS

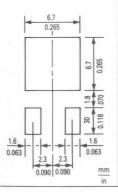


TMOS



CASE 369-03 TO-251 MTD1N40-1

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^{\circ}C$ unless otherwise noted)

Cha	racteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS — continue	d	V1	1 Set Voi		
Gate-Body Leakage Current, Forwa	ard (V _{GSF} = 20 Vdc, V _{DS} = 0)	IGSSF	11/1	100	nAdc
Gate-Body Leakage Current, Rever	se (V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR	1 7/3	100	nAdc
N CHARACTERISTICS*	V V				
Gate Threshold Voltage ($V_{DS} = V_{J} = 100^{\circ}C$	GS, ID = 1 mA)	VGS(th)	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	(V _{GS} = 10 Vdc, I _D = 0.5 Adc)	rDS(on)		5	Ohms
Drain-Source On-Voltage (VGS = (ID = 1 Adc) (ID = 0.5 Adc, TJ = 100°C)	VDS(on)		6.5 . 5	Vdc	
Forward Transconductance (VDS	gFS 44	0.5	VOST DRAIN	mhos	
YNAMIC CHARACTERISTICS					
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0,	Ciss	Regi <u>o</u> n Cha	300	pF
Output Capacitance	f = 1 MHz	Coss		30	
Reverse Transfer Capacitance	See Figure 11	C _{rss}	_	10	
WITCHING CHARACTERISTICS* (T.	J = 100°C)	- K - V - V			2
Turn-On Delay Time	90 12	td(on)		20	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	tr	200	15	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 13 and 14	td(off)		35	
Fall Time	988	tf		30	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Ωg	9 (Typ)	11	nC
Gate-Source Charge	ID = Rated ID, VGS = 10 V)	Qgs	7 (Typ)		
	See Figure 12				

See Figure 12

(Is = Rated ID

 $V_{GS} = 0$

 Q_{gd}

VSD

ton

trr

2 (Typ)

1 (Typ)

250 (Typ)

Limited by stray inductance

ns

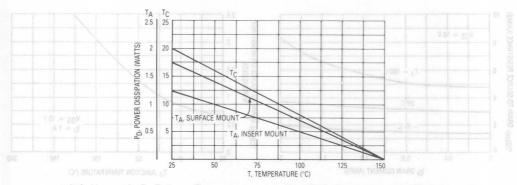
Reverse Recovery Time 1/1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/2019 | 1/20

SOURCE DRAIN DIODE CHARACTERISTICS*

Gate-Drain Charge

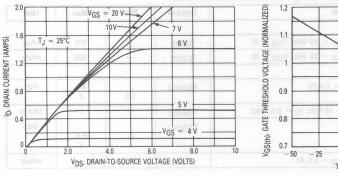
Forward On-Voltage

Forward Turn-On Time



3

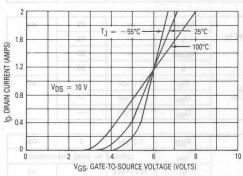
TYPICAL ELECTRICAL CHARACTERISTICS

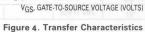


 $V_{DS} = V_{GS}$ ID = 1 mA 25 125 50 75 100 TJ, JUNCTION TEMPERATURE (°C)

Figure 2. On-Region Characteristics

Figure 3. Gate-Threshold Voltage Variation With Temperature





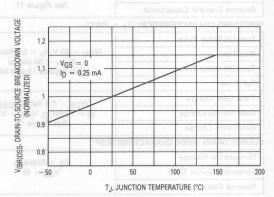


Figure 5. Breakdown Voltage Variation With Temperature

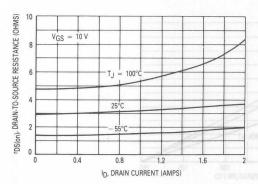


Figure 6. On-Resistance versus Drain Current

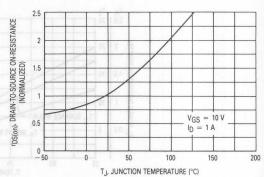


Figure 7. On-Resistance Variation With Temperature



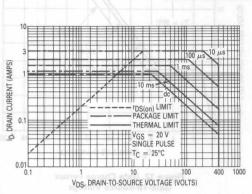


Figure 8. Maximum Rated Forward Biased Safe Operating Area

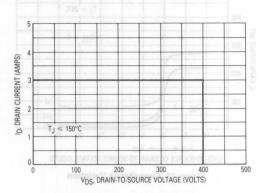


Figure 9. Maximum Rated Switching Safe Operating Area

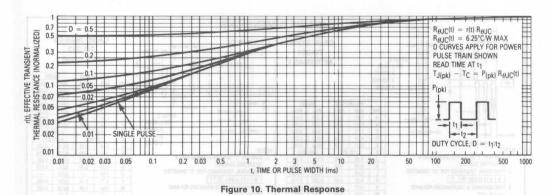
FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$



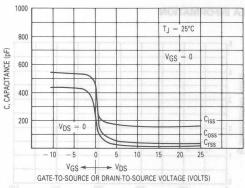
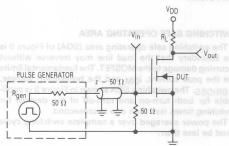


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-To-Source Voltage

toff→

RESISTIVE SWITCHING



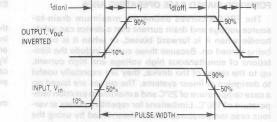
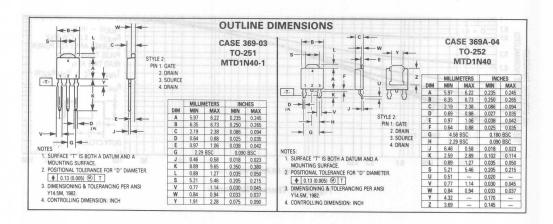


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms



MOTOROLA ■ SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS **DPAK for Surface Mount or Insertion** Mount

This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $rDS(on) 4 \Omega max$
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

- Available With Long Leads, Add -1 Suffix







MTD2N50

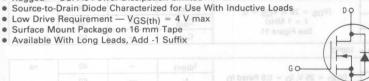
TMOS POWER FET

2 AMPERES rDS(on) = 4 OHMS 500 VOLTS

CASE 369A-04 TO-252 MTD2N50



CASE 369-03 TO-251 MTD2N50-1



MAXIMUM RATINGS

Rating	Symbol	MTD2N50	Unit
Drain-Source Voltage	V _{DSS}	500	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	500	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	2 4	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	20 0.16	Watt W/°C
Total Power Dissipation @ T _A = 25°C Derate above 25°C	PD	1.25 0.01	Watt W/°C
Total Power Dissipation @ T _A = 25°C (1) Derate above 25°C	PD	1.75 0.014	Watt W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150	°C
HERMAL CHARACTERISTICS	7	Tyrouw suaskue ja	
Thermal Desistance Lucation to Con-	- TAUUW	MSEM AT A SEM	2000

THERMAL CHARACTERISTICS		THOUN SUAMUE	All a lan
Thermal Resistance — Junction to Case	$R_{\theta JC}$	6.25	°C/W
 Junction to Ambient 	$R_{\theta JA}$	100	°C/W
 Junction to Ambient (1) 	100f EV	71.4	15

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS 0.265 0.063 0.063

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

	Characteristic						Max	Unit
OFF CHARACTERISTICS								
Drain-Source Breakdown V (VGS = 0, ID = 0.25 mA					V _{(BR)DSS}	500	-	Vdc
Zero Gate Voltage Drain Co (VDS = 0.8 Rated VDSS, TJ = 125°C						Big Si	0.2	mAdc
Gate-Body Leakage Curren	t, Forward	(VGSF =	20 Vdc, V _{DS} = 0)	IGSSF	_	100	nAdc
	te-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)						100	nAdc
ON CHARACTERISTICS*					IGSSR	E 67 153	1 2700	MOOH
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C						2 1.5	4.5 4	Vdc
Static Drain-Source On-Res	istance (V	GS = 10	Vdc, I _D = 1 Adc)		rDS(on)	_	4	Ohms
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 2 Adc) (I _D = 1 Adc, T _{.J} = 100°C)						is designed ions <u>su</u> ch a ly drivers.	10 10 18 8	Vdc
Forward Transconductance	(V _{DS} = 1	5 V, ID =	1 A)		9FS	witching Sp	la for East 8	mhos
OYNAMIC CHARACTERISTIC	S				Inedieni Leu	Actionionii	SOA is Pro	DISUIT WOOD
Input Capacitance	1 5	08 ()	700 - 25 V V00 -	th Industi	Ciss	Char ac teriz	500	pF
Output Capacitance		(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 11			Coss	11)8 <u>5V</u> — 7	100	
Reverse Transfer Capacitar	ice /				C _{rss}	to hha shed	50	
WITCHING CHARACTERIST	CS* (TJ =	100°C)			755	100000 1000000	Della Control Control	
Turn-On Delay Time	\1	(V _{DD} = 25 V, I _D = 0.5 Rated I _D			td(on)	_	40	ns
Rise Time	16				tr	_	60	
Turn-Off Delay Time		s s	$R_{gen} = 50 \text{ ohms}$ see Figures 13 and		td(off)	-	60	
Fall Time			3		tf	_	30	
Total Gate Charge		()//	DS = 0.8 Rated V _E		Qq	17 (Typ)	25	nC
Gate-Source Charge			Rated ID, VGS =		Qgs	9 (Typ)	19/5/08/2004	
Gate-Drain Charge			See Figure 12		Q _{gd}	8 (Typ)		
SOURCE DRAIN DIODE CHAI	RACTERIST	rics*	DEVELOTED .	toconyo		- 0		
Forward On-Voltage	- 00		(Is = Rated Ip	SEU 4	V _{SD}	1 (Typ)	2	Vdc
Forward Turn-On Time	00		$V_{GS} = 0$		ton	Limited	by stray indu	ictance
Reverse Recovery Time	201				(matrr = ad)	200 (Typ)	N	ns
Pulse Test: Pulse Width ≤ 300 µ	s, Duty Cyc	le ≤ 2%.	2	al al		80	nt — Continuo	rain Currer
	TA	TC						
	2.5	25	28	Qq		TC = 25°C		
	ATTS)	20	81.1	g#		0785 - AT 0		
	M) NOI 1.5		TC	-0	1	Totale L. T.		
	PATI(15 IC						
	POWER DISSIPATION (WATTS)					netion		
	Po, Pov	5	TA, INSERT	MOUNT		STICS notion to Case		
	VVV		100	ua8		No notes		
		25	50 75	100	125	150		

Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

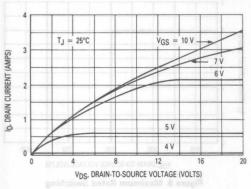


Figure 2. On-Region Characteristics

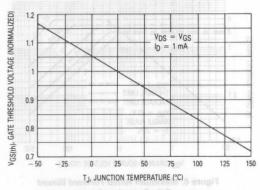


Figure 3. Gate-Threshold Voltage Variation With Temperature

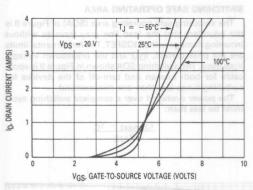


Figure 4. Transfer Characteristics

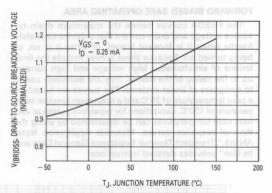


Figure 5. Breakdown Voltage Variation
With Temperature

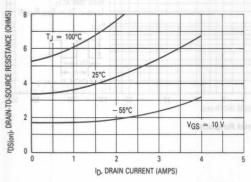


Figure 6. On-Resistance versus Drain Current

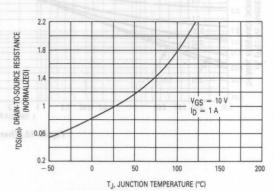


Figure 7. On-Resistance Variation With Temperature

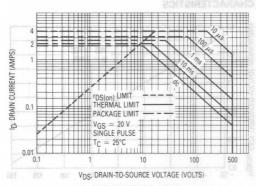


Figure 8. Maximum Rated Forward Biased Safe Operating Area

Figure 9. Maximum Rated Switching Safe Operating Area

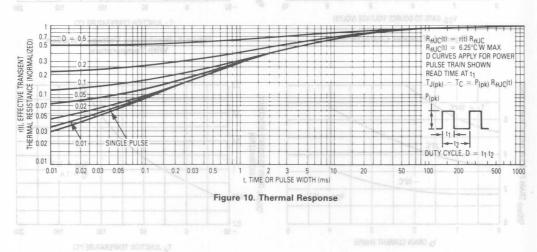
FORWARD BIASED SAFE OPERATING AREA

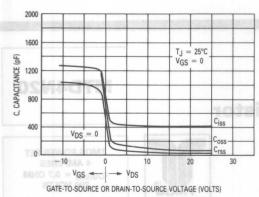
The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$





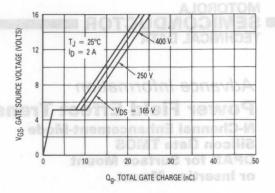


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus

Gate-to-Source Voltage

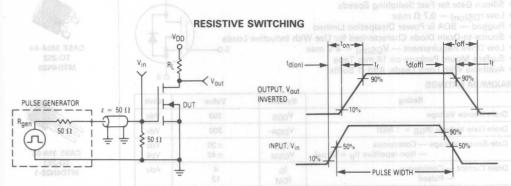
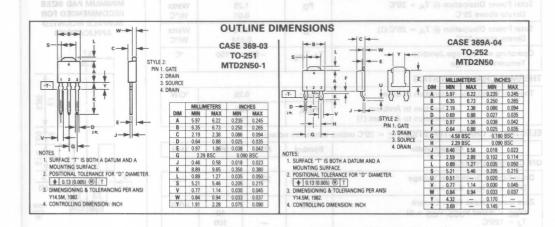


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms



MOTOROLA SEMICONDUCTOR I **TECHNICAL DATA**

Advance Information

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS **DPAK for Surface Mount** or Insertion Mount



DQ

TMOS POWER FET 4 AMPERES rDS(on) = 0.7 OHM

200 VOLTS

MTD4N20

This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ 0.7 Ω max
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement V_{GS(th)} = 4 V max
 Surface Mount Package on 16 mm Tape
- Available With Long Leads, Add -1 Suffix









CASE 369-03 TO-251 MTD4N20-1

MAXIMUM RATINGS

Rating	Symbol	Value Tug	Unit
Drain-Source Voltage	V _{DSS}	200	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	200	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	IDM	4 12	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	20 0.16	Watts W/°C
Total Power Dissipation @ T _A = 25°C Derate above 25°C	PD	1.25 0.01	Watts W/°C
Total Power Dissipation @ T _A = 25°C (1) Derate above 25°C	PD	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	R _θ JC	6.25	°C/W
— Junction to Ambient	R ₀ JA	100	Type Big
— Junction to Ambient (1)		71.4	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	A STOR OF THE BOTHS A STORE OF THE BOTH A	1500	675.0 SF.0	30.0 L
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	V _(BR) DSS	200	80.0 VS.1 00.0 80.2 100.0 Nt.1	Vdc
Zero Gate Voltage Drain Current (V _{DS} = Rated V _{DSS} , V _{GS} = 0) T _J = 125°C	IDSS	980.5	10 100	μAdd

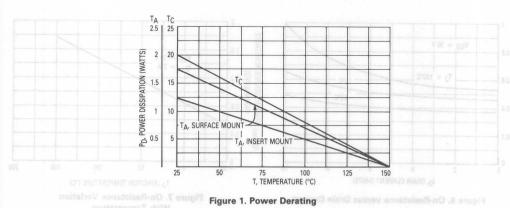
MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED **APPLICATIONS** 0.265 0.265 6.7 8 20 1.6 0.063 0.063

⁽¹⁾ These ratings are applicable when surface mounted on the minimum pad size recommended. (continued)
This document contains information on a new product. Specifications and information herein are subject to change without notice.

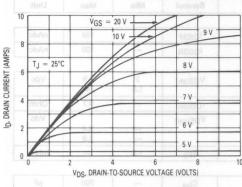
ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Cha	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS — continue	d		L-Lvas	Ves =	
Gate-Body Leakage Current, Forw	IGSSF	4-4- VD	100	nAdc	
Gate-Body Leakage Current, Reve	rse (V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR	1/3//	100	nAdc
ON CHARACTERISTICS*		V8			ofas = gT
Gate Threshold Voltage (V _{DS} = V T _J = 100°C	(GS, ID = 1 mA)	V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	(VGS = 10 Vdc, ID = 2 Adc)	rDS(on)		0.7	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 4 Adc) (I _D = 2 Adc, T _{.I} = 100°C)				3.4 2.9	Vdc
Forward Transconductance (VDS	9 _{FS}	1.5	<u>-</u>	mhos	
YNAMIC CHARACTERISTICS	2 0 05 - 05 - 01	(27)(00, 20	AT INV STIEL INS INV	LINE CONTRACT	
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0,	Ciss	[700	pF
Output Capacitance	f = 1 MHz)	Coss	Region Char	300	9
Reverse Transfer Capacitance	See Figure 11	C _{rss}		80	1
WITCHING CHARACTERISTICS* (T	J = 100°C)				
Turn-On Delay Time	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	td(on)		50	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	tr	II	150	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 13 and 14	td(off)		100	Y
Fall Time	Am S.O = of H H H	tf		50	
Total Gate Charge	(VDS = 0.8 Rated VDSS,	Qg	9 (Typ)	20	nC
Gate-Source Charge	ID = Rated ID, VGS = 10 V)	Qgs	4 (Typ)		
Gate-Drain Charge	See Figure 12	Qgd	5 (Typ)		
OURCE DRAIN DIODE CHARACTER	RISTICS*		MITT		
Forward On-Voltage	(IS = Rated ID	V _{SD}	1.5 (Typ)	3	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	uctance
Reverse Recovery Time	0 02-001	t _{rr}	300 (Typ)	- 5	ns

^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



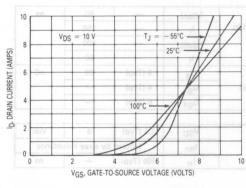
TYPICAL ELECTRICAL CHARACTERISTICS - 2017249170A8AM0 JAOISTOR B



1.1 Vps = Vgs | Vps = 1 mA | Vp

Figure 2. On-Region Characteristics

Figure 3. Gate-Threshold Voltage Variation With Temperature



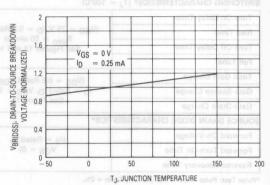
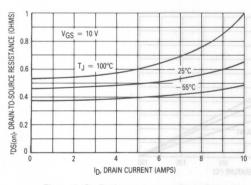


Figure 4. Transfer Characteristics

Figure 5. Breakdown Voltage Variation With Temperature



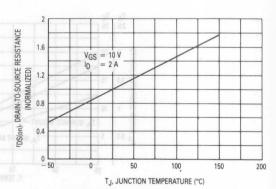


Figure 6. On-Resistance versus Drain Current

Figure 7. On-Resistance Variation
With Temperature

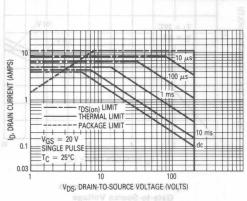


Figure 8. Maximum Rated Forward Biased Safe Operating Area

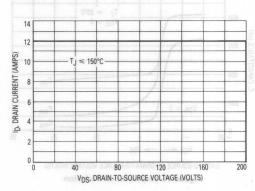


Figure 9. Maximum Rated Switching
Safe Operating Area

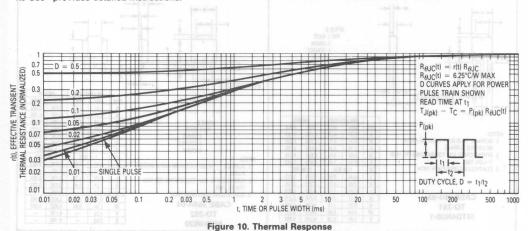
FORWARD BIASED SAFE OPERATING AREA

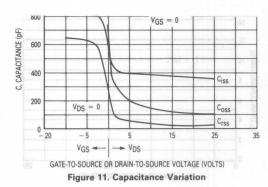
The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, V_{BR} DSS. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$





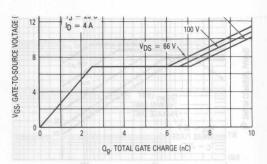


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

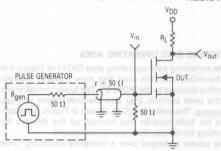


Figure 13. Switching Test Circuit

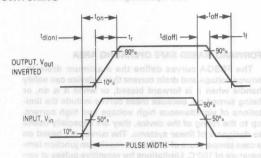
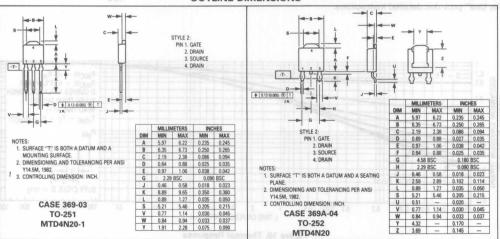


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



3

MOTOROLA SEMICONDUCTOR **TECHNICAL DATA**

Designer's Data Sheet

Power Field Effect Transistors

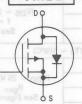
P-Channel Enhancement Mode Silicon Gate TMOS DPAK for Surface Mount or Insertion Mount

These TMOS Power FETs are designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low rDS(on) 0.3 Ω max
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement VGS(th) = 4 V max
- Surface Mount Package on 16 mm Tape
- Available With Long Leads, Add -1 Suffix

MTD4P05 MTD4P06

TMOS POWER FETs **4 AMPERES** rDS(on) = 0.6 OHM 50 and 60 VOLTS



TMOS



CASE 369A-04 TO-252 MTD4P05 MTD4P06



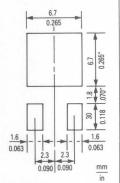
TO-251 MTD4P05-1



CASE 369-03 MTD4P06-1

MINIMUM PAD SIZES RECOMMENDED FOR

SURFACE MOUNTED **APPLICATIONS**



MAXIMUM RATINGS

	Rating	0g 12	Symbol	MTD4P05	MTD4P06	Unit
Drain-Source Vo	Itage	Q _{gs} 7	VDSS	50	60	Vdc
Drain-Gate Volta	VDGR	50	60	Vdc		
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)			V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed			IDM	14		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C			PD	20 0.16		Watt:
Total Power Dissipation @ T _A = 25°C Derate above 25°C			PD	1.25 0.01		Watts W/°C
Total Power Dissipation @ T _A = 25°C (1) Derate above 25°C			PD	1.75 0.014		Watt:
Operating and Storage Junction Temperature Range			T _J , T _{stg}	-65 to	o +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	R _θ JC	6.25	°C/W
 Junction to Ambient 	$R_{\theta JA}$	100	
 Junction to Ambient (1) 		71.4	16

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS			TINU	SURFACE MO	A1.
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	MTD4P05 MTD4P06	V(BR)DSS	50 60		Vdc
Zero Gate Voltage Drain Current (Vps = 0.85 Rated Vpss, Vgs = TJ = 125°C	= 0)	IDSS	T, TEM	0.2	mAdc

Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design

(1) These ratings are applicable when surface mounted on the minimum pad size recommended. Designer's Data for "Worst Case" Conditions - The Designer's Data Sheet permits the design of most circuits entirely from the information presented.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted) Characteristic Symbol

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continue	od .			ATAC J	CHNICA
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		IGSSF	_	100	nAdc
Gate-Body Leakage Current, Reve	rse (VGSR = 20 Vdc, VDS = 0)	IGSSR	10 Ch	100	nAdc
N CHARACTERISTICS*		100	3110 101	10-00	andie.
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C		V _{GS(th)}	1.5	4.5	Vdc
Static Drain-Source On-Resistance	e (V _{GS} = 10 Vdc, I _D = 2 Adc)	rDS(on)	POTTERNA	0.6	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 4 Adc) (I _D = 2 Adc, T _J = 100°C)		V _{DS(on)}	nol l e:	2.4	Vdc
Forward Transconductance (VDS	= 15 V, I _D = 2 A)	9FS	0.75	_	mhos
YNAMIC CHARACTERISTICS	need, low loss	d for high sp	are designe	Power FETs	nese TMOS
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0,	Ciss	s su <u>ch</u> as s	700	pF ² 18
Output Capacitance	f = 1 MHz)	Coss	Approx.	400	lers, solenor
Reverse Transfer Capacitance	See Figure 12	C _{rss}	ando Bumo	150	(do)S(I) WO
WITCHING CHARACTERISTICS* (T	J = 100°C)	Limited	Dissipation	A is Power	ugged — SC
Turn-On Delay Time	T Sales Teansure	td(on)	aracterized -	40	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r eq	n 16 mim Te	120	urface Moul
Turn-Off Delay Time	$R_{gen} = 50 \text{ ohms}$ See Figures 10, 14 and 15	td(off)	s, Add -1 St	80 01 4	riW eldeliev
Fall Time		tf	_	70	DOMUM RAT
Total Gate Charge	(VDS = 0.8 Rated VDSS,	Qg	12 (Typ)	16	nC
Gate-Source Charge	ID = Rated ID, VGS = 10 V)	Qgs	7 (Typ)	Tegstlo	ain-Source \
Gate-Drain Charge	See Figure 13	Q _{gd}	5 (Typ)	= a: \ ana	rain-Gate Vol

(IS = Rated ID

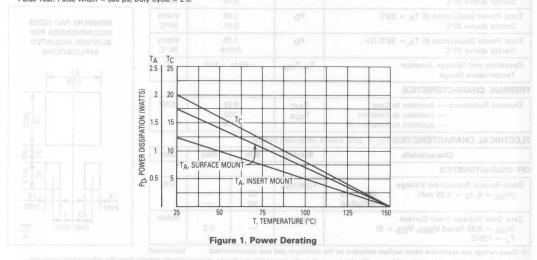
 $V_{GS} = 0$

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

Forward On-Voltage

Forward Turn-On Time

Reverse Recovery Time



1.8 (Typ)

325 (Typ)

5

Limited by stray inductance

VSD

ton

NILLAMPON, OC

3

TYPICAL ELECTRICAL CHARACTERISTICS

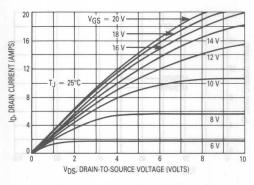


Figure 2. On-Region Characteristics

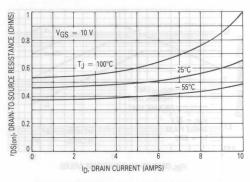


Figure 3. Gate-Threshold Voltage Variation With Temperature

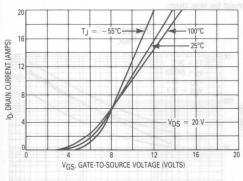


Figure 4. Transfer Characteristics

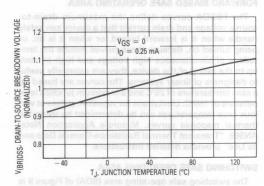


Figure 5. Breakdown Voltage Variation
With Temperature

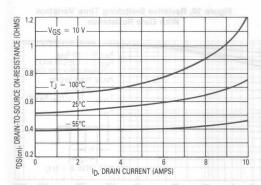


Figure 6. On-Resistance versus Drain Current

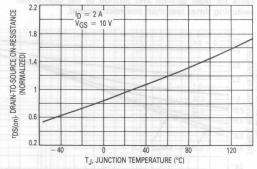


Figure 7. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

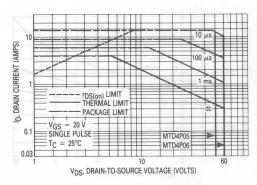


Figure 8. Maximum Rated Forward Bias
Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

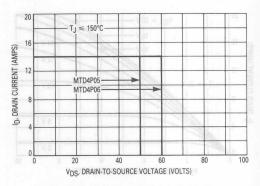


Figure 9. Maximum Rated Switching Safe Operating Area

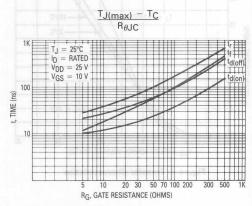


Figure 10. Resistive Switching Time Variation
With Gate Resistance

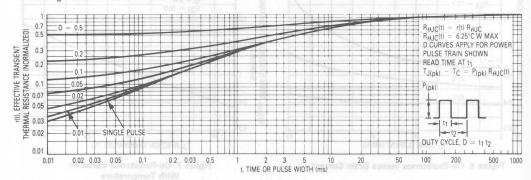
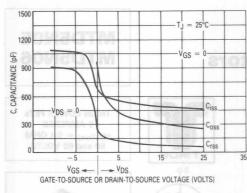


Figure 11. Thermal Response

TYPICAL CHARACTERISTICS

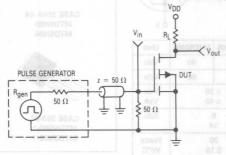


0 TJ = 25°C | 10 RATED | 10 RATED

Figure 12. Capacitance Variation

Figure 13. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING



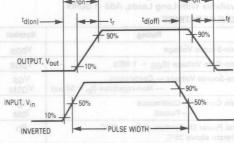
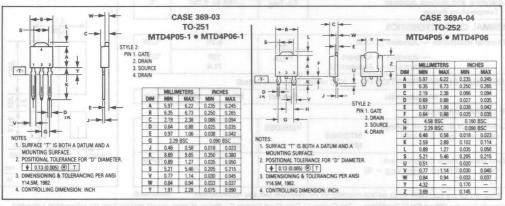


Figure 14. Switching Test Circuit

Figure 15. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR **TECHNICAL DATA**

Designer's Data Sheet

Power Field Effect Transistors

N-Channel Enhancement Mode Silicon Gate TMOS **DPAK for Surface Mount or Insertion**

TMOS

MTD5N05 MTD5N06

TMOS POWER FETS 5 AMPERES rDS(on) = 0.4 OHM 50 and 60 VOLTS

These TMOS Power FETs are designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low rps(on) 0.4 Ω max
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement V_{GS(th)} = 4 V max
 Surface Mount Package on 16 mm Tape
- · Available With Long Leads, Add -1 Suffix

MAXIMUM RATINGS

Rating	Symbol	MTD5N05	MTD5N06	Unit
Drain-Source Voltage	VDSS	50	60	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	50	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}		20 40	Vdc Vpk
Drain Current — Continuous — Pulsed	IDM		5	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	20 0.16		Watts W/°C
Total Power Dissipation @ T _A = 25°C Derate above 25°C	PD	1.25 0.01		Watts W/°C
Total Power Dissipation @ T _A = 25°C (1) Derate above 25°C	PD	1.75 0.014		Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	- 65 to	o +150	°C

THERMAL CHARACTERISTICS

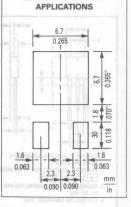
Thermal Resistance — Junction to Case	R _O JC	6.25	°C/W
— Junction to Ambient	$R_{\theta JA}$	100	°C/W
— Junction to Ambient (1)	0071	71.4	30/00/02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS	Mid	11-10-14	387.0	2017 1813	SER L R
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	MTD5N05 MTD5N06	V(BR)DSS	50 60	106 80 107 201 107 201 108 8	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.8$ Rated V_{DSS} , $V_{GS} = 0$) $T_{J} = 125^{\circ}C$	NEE FOR "O" (BLAMETER [T] HEREMOND FER ANNI	IDSS	080 0 - 2 0.0 - 3 0.0 - 3 0.0	0.2	mAdc

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.





MINIMUM PAD SIZES **RECOMMENDED FOR** SURFACE MOUNTED

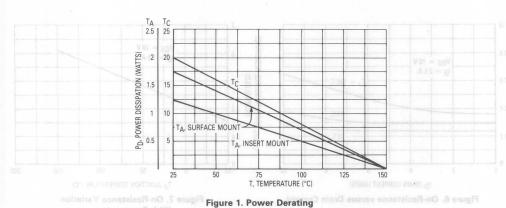
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continue	1 3 8 7 1			20 V /	
Gate-Body Leakage Current, Forwa	rd (V _{GSF} = 20 Vdc, V _{DS} = 0)	IGSSF	GB. T	100	nAdc
Gate-Body Leakage Current, Rever	se (V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR	-	100	nAdo
ON CHARACTERISTICS*		V.8		1/1/	
Gate Threshold Voltage (V _{DS} = V _{DS}	3S, ID = 1 mA)	V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	(V _{GS} = 10 Vdc, I _D = 2.5 Adc)	rDS(on)	_	0.4	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 5 Adc) (I _D = 2.5 Adc, T _J = 100°C)		VDS(on)		2.4	Vdc
Forward Transconductance (VDS =	= 15 V, I _D = 2.5 A)	9FS	1		mhos
YNAMIC CHARACTERISTICS	0 8- 00- < 01		9		0
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz)	Ciss	DUY SUMPLE UT	300	pF
Output Capacitance		Coss	r-Reg <u>io</u> n Ch	160	
Reverse Transfer Capacitance	See Figure 11	C _{rss}	-	50	1
WITCHING CHARACTERISTICS* (T	j = 100°C)				
Turn-On Delay Time	2	td(on)		25	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	tr	-	25	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 13 and 14	td(off)	+	50	
Fall Time		tf	-	50	
Total Gate Charge	(VDS = 0.8 Rated VDSS,	Q_g	6 (Typ)	15	nC
Gate-Source Charge	ID = Rated ID, VGS = 10 V)	Qgs	3 (Typ)		
Gate-Drain Charge	See Figure 12	Q _{gd}	3 (Typ)	- -	
SOURCE DRAIN DIODE CHARACTER	ISTICS*				
Forward On-Voltage	(Is = Rated In	V _{SD}	2 (Typ)	3	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	luctance

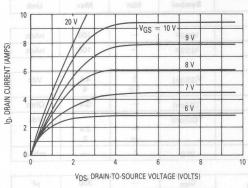
^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

Reverse Recovery Time



300 (Typ)

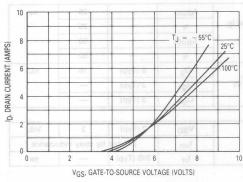
TYPICAL ELECTRICAL CHARACTERISTICS CONTRIBUTION AND INDICATE AND INDIC



GATE THRESHOLD VOLTAGE (NORMALIZED) $V_{DS} = V_{GS}$ $I_{D} = 1 \text{ mA}$ 1.1 0.9 0.8 VGS(th), (0.7 25 100 - 50 50 75 TJ, JUNCTION TEMPERATURE (°C)

Figure 2. On-Region Characteristics

Figure 3. Gate-Threshold Voltage Variation With Temperature



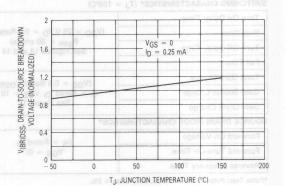
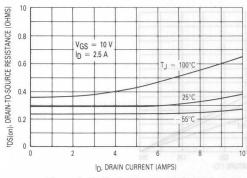


Figure 4. Transfer Characteristics

Figure 5. Breakdown Voltage Variation With Temperature



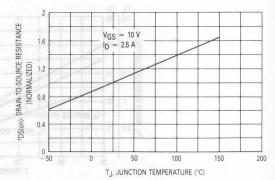


Figure 6. On-Resistance versus Drain Current

Figure 7. On-Resistance Variation With Temperature

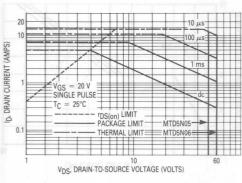


Figure 8. Maximum Rated Forward Biased
Safe Operating Area

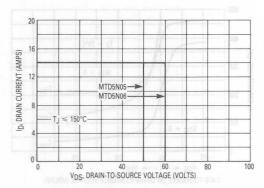


Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

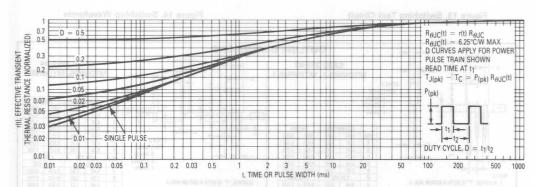


Figure 10. Thermal Response

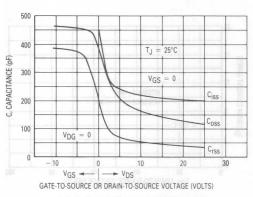


Figure 11. Capacitance Variation

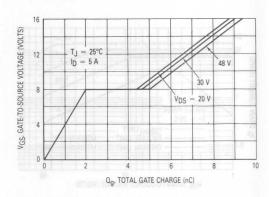


Figure 12. Gate Charge versus

Gate-to-Source Voltage

RESISTIVE SWITCHING

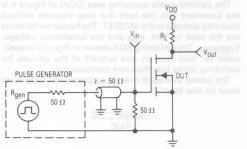


Figure 13. Switching Test Circuit

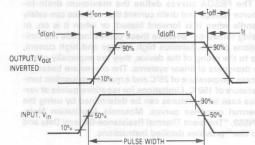
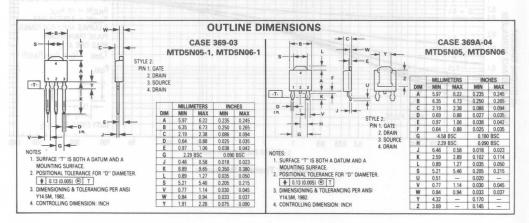


Figure 14. Switching Waveforms



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS DPAK for Surface Mount or Insertion Mount

TMOS

TMOS POWER FETS
6 AMPERES
rDS(on) = 0.25 OHM
80 and 100 VOLTS

MTD6N08

MTD6N10

These TMOS Power FETs are designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low r_{DS(on)} 0.25 Ω max
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement VGS(th) = 4 V max
- Surface Mount Package on 16 mm Tape
- Available With Long Leads, Add -1 Suffix



MAXIMUM RATINGS

Rating	Symbol	MTD6N08	MTD6N10	Unit
Drain-Source Voltage	VDSS	80	100	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}		20 40	Vdc Vpk
Drain Current — Continuous — Pulsed (QYT) 5.1 — QaV	I _D		6 20	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	20 0.16		Watts W/°C
Total Power Dissipation @ T _A = 25°C Derate above 25°C	PD		25 01	Watts W/°C
Total Power Dissipation @ T _A = 25°C (1) Derate above 25°C	PD		75 014	Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	- 65 to	+ 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	R_{θ} JC	6.25	°C/W
 Junction to Ambient 	$R_{\theta JA}$	100	°C/W
— Junction to Ambient (1)		71.4	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS			1	7	- 01
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	MTD6N08 MTD6N10	V(BR)DSS	80 100	DW SOAHHUE	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) TJ = 125°C	11 651	DSS 000	ET	10 100	μAdd

Zero Gate Voltage Drain Current
(VDS = Rated VDSS, VGS = 0)
T J = 125°C

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

Continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented.

Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

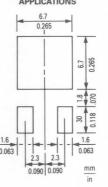


TO-251 MTD6N08-1 MTD6N10-1



TO-252 MTD6N08 MTD6N10

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic

OFF CHARACTERISTICS — continued				
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	IGSSF		100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	10-511	100	nAdc
ON CHARACTERISTICS*	ow'll troub!	4-7 b	Jail .	e dicent
Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_{D} = 1$ mA) $T_{J} = 100$ °C	V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 3 Adc)	rDS(on)	801	0.25	Ohm
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_{D} = 6 \text{ Adc}$) ($I_{D} = 3 \text{ Adc}$, $T_{J} = 100^{\circ}\text{C}$)	V _{DS(on)}	ce Mo un <u>t</u>	1.6 1.5	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 3 A)	g _{FS}	giaab _l ens s	Powar HET	mhos
DYNAMIC CHARACTERISTICS	switching regula	ns such ps	distribute g	invalue
			T	_

Min

Symbol

Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 11	Ciss	tchina Son	600	pF
Output Capacitance		Coss	— ×80	400	mg)201 W
Reverse Transfer Capacitance		C _{rss}	Dis <u>si</u> patio	80	gged — S

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time		td(on)	mm-21 no	50	JoM ns shu
Rise Time //301///	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r	ids, Add -118	150	W eldslisv
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 13 and 14	td(off)	-	100	DARWING BAD
Fall Time	Symbol MTDeWes MTDGW10 Uint	tf	8	50	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V) See Figure 12	Ωg	13 (Typ)	30	nC
Gate-Source Charge		Qgs	6 (Typ)	sau Wes	rain-Cate Ve
Gate-Drain Charge		Q _{gd}	7 (Typ)	Itago_—Co	ate-Source Vo

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	(IS = Rated ID	V _{SD}	1.7 (Typ)	3	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited I	by stray ind	luctance
Reverse Recovery Time	0.16 W ² C	trr	100 (Typ)	_3765	ns

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

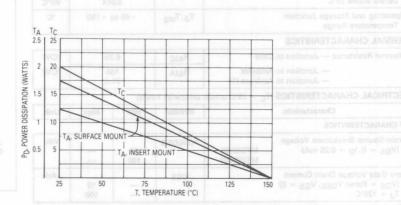


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

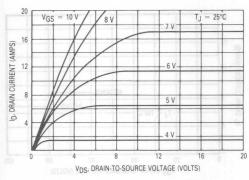


Figure 2. On-Region Characteristics

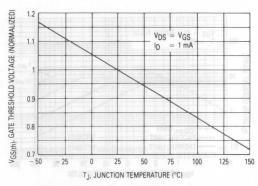


Figure 3. Gate-Threshold Voltage Variation With Temperature

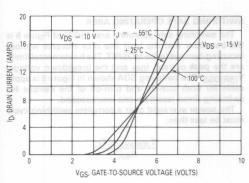


Figure 4. Transfer Characteristics

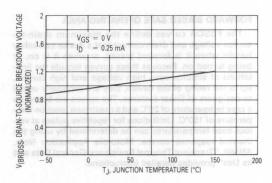


Figure 5. Breakdown Voltage Variation With Temperature

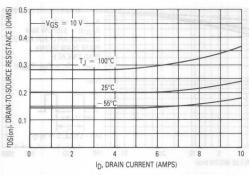
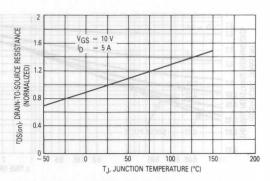


Figure 6. On-Resistance versus Drain Current and American Figure 7. On-Resistance Variation



With Temperature

SAFE OPERATING AREA INFORMATION

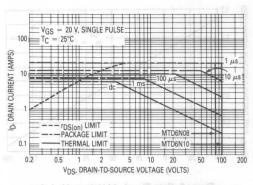


Figure 8. Maximum Rated Forward Biased Safe Operating Area

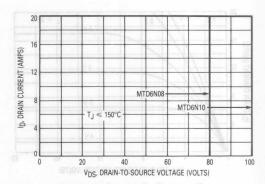


Figure 9. Maximum Rated Switching Safe Operating Area

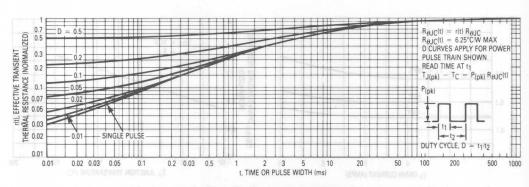
FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

$$\frac{\mathsf{T}\mathsf{J}(\mathsf{max}) - \mathsf{T}\mathsf{C}}{\mathsf{R}_{\theta}\mathsf{J}\mathsf{C}}$$



nottainaV sonetalasA-nO X shapR Figure 10. Thermal Response when graves sonetalasR-nO & shapR

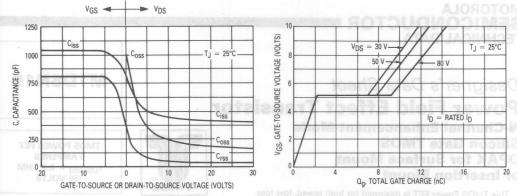


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-To-Source Voltage

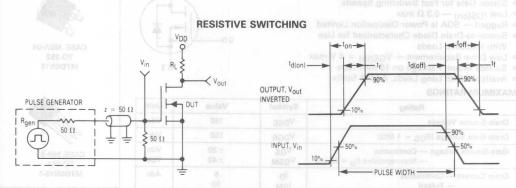
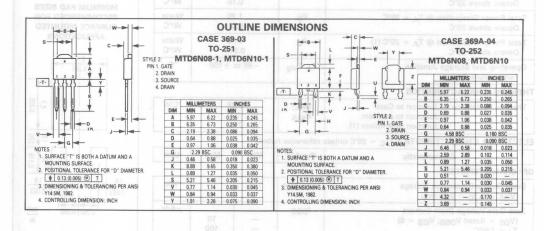


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS DPAK for Surface Mount or Insertion Mount

This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- · Silicon Gate for Fast Switching Speeds
- Low r_{DS(on)} 0.3 Ω max
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement VGS(th) = 4 V max
- Surface Mount Package on 16 mm Tape
- Available With Long Leads, Add -1 Suffix

MAXIMUM RATINGS

Rating	Symbol	Value 100 =	Unit
Drain-Source Voltage	V _{DSS}	150	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	150	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	6 20	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	20 0.16	Watts W/°C
Total Power Dissipation @ T _A = 25°C Derate above 25°C	PD	1.25	Watts W/°C
Total Power Dissipation @ T _A = 25°C (1) Derate above 25°C	PD	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	TJ, T _{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	6.25	°C/W
— Junction to Ambient	$R_{\theta JA}$	100	
— Junction to Ambient (1)		71.4	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	DIAMETRO DE PROCESO E	500 T	era ita	83 3
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)	V _{(BR)DSS}	150	00 H3 00 H3	Vdc
Zero Gate Voltage Drain Current (V _{DS} = Rated V _{DSS} , V _{GS} = 0) T _J = 125°C	IDSS	=	10 100	μAdc

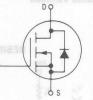
(1) These ratings are applicable when surface mounted on the minimum pad size recommended. (continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MTD6N15



TMOS POWER FET
6 AMPERES
rDS(on) = 0.3 OHM
150 VOLTS



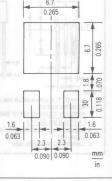


TO-252 MTD6N15



TO-251 MTD6N15-1





ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued	1 22 22 22 22				
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		IGSSF		100	nAdc
Gate-Body Leakage Current, Reverse	e (V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR		100	nAdc
ON CHARACTERISTICS*		78.			
Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_{D} = 1$ mA) $T_{J} = 100$ °C		V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (\	V _{GS} = 10 Vdc, I _D = 3 Adc)	rDS(on)		0.3	Ohm
Drain-Source On-Voltage (V _{GS} = 10 (I _D = 6 Adc) (I _D = 3 Adc, T _J = 100°C)	(V 0	V _{DS(on)}		1.8 1.5	Vdc
Forward Transconductance (V _{DS} =	15 V, I _D = 3 A)	9 _{FS}	2.5	13-	mhos
YNAMIC CHARACTERISTICS	0 08 08	02 GA	66	00 00	
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss	10 SOURCE VOLUM	1200	pF
Output Capacitance	f = 1 MHz	Coss	sered 7 noise	500	
Reverse Transfer Capacitance	See Figure 11	C _{rss}		120	
WITCHING CHARACTERISTICS* (TJ	= 100°C)				
Turn-On Delay Time		td(on)	_	50	ns
Rise Time	$(V_{DD} = 25 \text{ V}, I_{D} = 3 \text{ A},$	= t _r		180	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 13 and 14	td(off)		200	
Fall Time		tf	1 4 1	100	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Ωg	15 (Typ)	30	nC
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 V)	Qgs	8 (Typ)		
Gate-Drain Charge	See Figure 12	Q _{gd}	7 (Typ)		
OURCE DRAIN DIODE CHARACTERIS	STICS*				
Forward On-Voltage	$V_{GS} = 6 \text{ A, di/dt} = 25 \text{ A/}\mu\text{s}$	V _{SD}	1.3 (Typ)	2	Vdc
Forward Turn-On Time		ton	Limited	by stray ind	uctance
Reverse Recovery Time		t _{rr}	325 (Typ)		ns

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

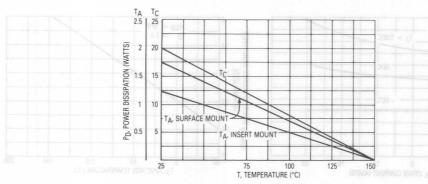
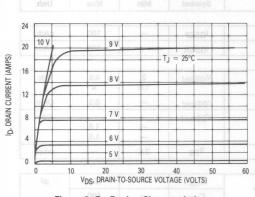


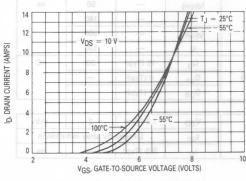
Figure 1. Power Derating and State Described and Advance of Figure 1. Power Derating



VGS(th), GATE THRESHOLD VOLTAGE (VOLTS) $V_{DS} = V_{GS}$ $I_{D} = 1 \text{ mA}$ 3.2 2.8 2.4 OT 100 - 50 50 TJ, JUNCTION TEMPERATURE (°C)

Figure 2. On-Region Characteristics

Figure 3. Gate-Threshold Voltage Variation With Temperature



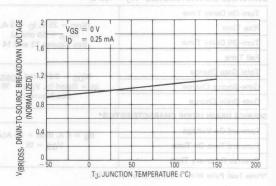
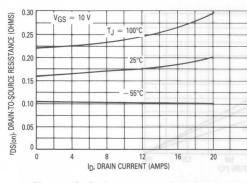


Figure 4. Transfer Characteristics

Figure 5. Breakdown Voltage Variation With Temperature



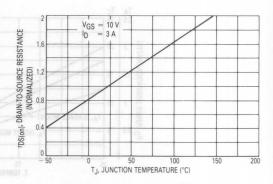


Figure 6. On-Resistance versus Drain Current 1880 8 1880 Figure 7. On-Resistance Variation

With Temperature

3

SAFE OPERATING AREA INFORMATION

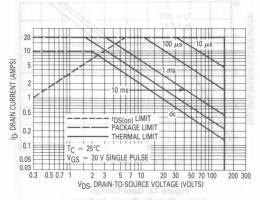


Figure 8. Maximum Rated Forward Biased Safe Operating Area

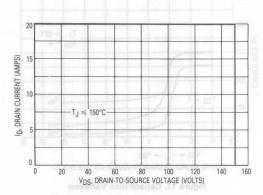


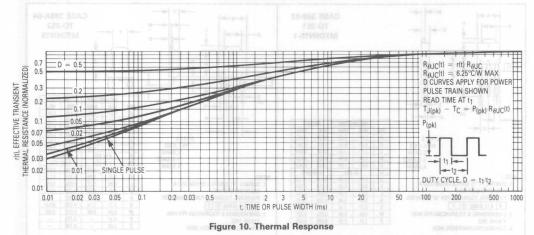
Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

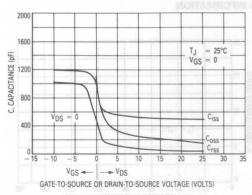
The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

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TJ = 25°C
ID = 6 A

VDS = 50 V

VDS = 50 V

Qg, TOTAL GATE CHARGE (nC)

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

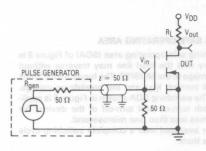


Figure 13. Switching Test Circuit

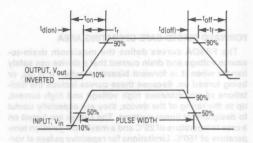
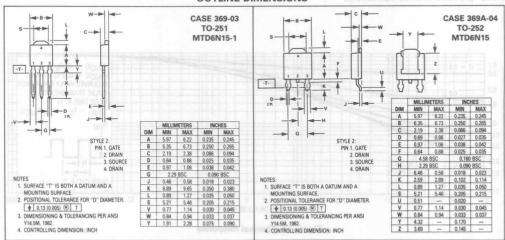


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

TMOS IV

Power Field Effect Transistor

N-Channel Enhancement-Mode

DPAK for Surface Mount or Insertion Mount

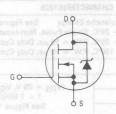
This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits.
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode.
- · Diode is Characterized for Use in Bridge Circuits.
- · Available With Long Leads, Add -1 Suffix

MTD10N05E

TMOS POWER FETS 10 AMPERES rDS(on) = 0.1 OHM 50 VOLTS







MAXIMUM RATINGS (T,J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	VDSS	batter 850 _ anvi	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	50 50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous OVT P	I _D	10 24	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	20 0.16	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C

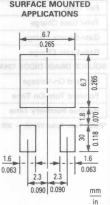
THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	R _θ JC R _θ JA	6.25 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

(1) These ratings are applicable when surface mounted on the minimum pad size recommended. (contin

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Cha	racteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS				100	1975	
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)			V(BR)DSS	50	1 S_LD/6 83.F	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0,		ene'	IDSS	HEFF	10 100	μΑ
Gate-Body Leakage Current, Forw	ard (V _{GSF} = 20 Vdc, V _{DS} = 0)		IGSSF	emeene	100	nAdc
Gate-Body Leakage Current, Reve	rse (V _{GSR} = 20 Vdc, V _{DS} = 0)	iserti	IGSSR	rol li es	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$ $T_{J} = 100^{\circ}\text{C}$	anne anne	ls is and vices	VGS(th)	0 30MT to	4.5	Vdc
Static Drain-Source On-Resistance	e (V _{GS} = 10 Vdc, I _D = 5 Adc)	.somi	rDS(on)	odes with h	0.1	Ohm
Drain-Source On-Voltage (V _{GS} = (I _D = 10 Adc) (I _D = 5 Adc, T _J = 100°C)	10 V)	don- idge	VDS(on)	verters and cularly well	1.1 0.9	Day Service
Forward Transconductance (VDS	= 15 V, I _D = 5 A)	ni	9FS	4.5	ito b n s ,las	mhos
DRAIN-TO-SOURCE AVALANCHE CI	HARACTERISTICS			transients.	ed voltage	st unexpect
Unclamped Drain-to-Source Avalanche Energy See Figures 16 and 17 (ID = 24 A, V_{DD} = 6 V, T_{C} = 25°C, Single Pulse, Non-repetitive) (ID = 10 A, V_{DD} = 6 V, T_{C} = 25°C, P_{C} , P_{C} = 10 μ s, Duty Cycle \leq 1%) (ID = 4 A, V_{DD} = 6 V, T_{C} = 100°C, P_{C} . \leq 10 μ s, Duty Cycle \leq 1%)			WDSR	node Desig it Su <u>pp</u> ressi e Mo <u>de</u> — t S) En <u>argy</u> C	5 6 2.5	Lm Curting Courts of the Court
DYNAMIC CHARACTERISTICS	THE STATE OF THE S	not he	Ninna2 /MO2	Store Area (C	Sale Degre	anite turns
Input Capacitance	(Van - 25 V Van -	0	C _{iss}	ariuar il0 egb	850	MeH pF as
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 1 \text{ MHz})$	8 00 1	Coss	cove <u>ry</u> Tim	350	IstO-ot-earling
Reverse Transfer Capacitance	See Figure 14		C _{rss}	in8 nTesti	100	iscrete rande is Chara
SWITCHING CHARACTERISTICS* (T	J = 100°C)		xiftix	is, Add -1 Si	Long Lead	ritiW sidslii
Turn-On Delay Time			td(on)	_	30	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Ra	ted ID	t _r	-	90	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figure 18	(list	td(off)	25°C unless	45	TAR MUMI
Fall Time	roti Value Urot	Symbo	tf	- pr	35	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DS}	COV.	Q_g	14 (Typ)	17 _{psilo}	nC
Gate-Source Charge	ID = Rated ID, VGS = 1		Qgs	7 (Typ)	= 23 70 ops	in-Cata Volu
Gate-Drain Charge	See Figure 15	apV	Q _{gd}	7 (Typ)	itage - Cor	e-Sourge Vo
SOURCE DRAIN DIODE CHARACTE	RISTICS*	MSDV	(au, 03 ≥)) evinneger-	nol/!—	
Forward On-Voltage	(I _{FM} = 0.5 Rated I _D ,	Ol	V _{SD}	1 (Typ)	mounigned -	Vdc
Forward Turn-On Time	dls/dt = 100 A/μs, VGS		ton	Limited	by stray inc	ductance
Reverse Recovery Time	0.16 W/C	0.1	t _{rr}	50 (Typ)	25°C-	ns
*Pulse Test: Pulse Width = 300 μs, Duty	r Cycle ≤ 2%.	TJ. Tstg	54	perature Rani	storage Tem	
7.8 2.3 0.063						

3

TYPICAL ELECTRICAL CHARACTERISTICS

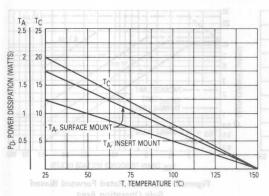


Figure 1. Power Derating

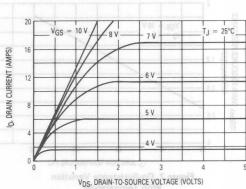


Figure 2. On-Region Characteristics

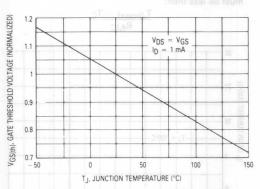


Figure 3. Gate-Threshold Voltage Variation
With Temperature

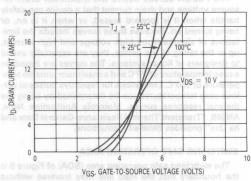


Figure 4. Transfer Characteristics

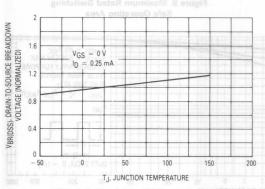


Figure 5. Breakdown Voltage Variation With Temperature

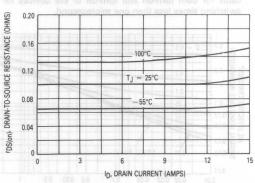


Figure 6. On-Resistance versus Drain Current

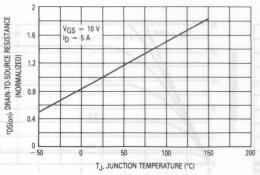


Figure 7. On-Resistance Variation With Temperature

Figure 8. Maximum Rated Forward Biased Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V(\mbox{\footnotesize BR})_{\mbox{\footnotesize DSS}}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

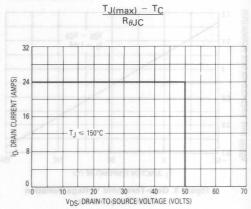


Figure 9. Maximum Rated Switching Safe Operating Area

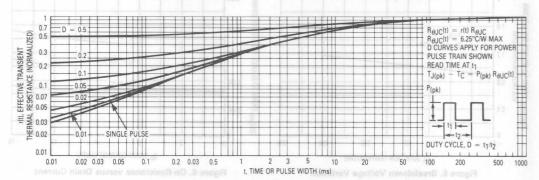


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of $I_{\mbox{FM}}$ and peak $V_{\mbox{R}}$ for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM} , peak V_{R} or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

VDS(pk) is the peak drain-to-source voltage that the device must sustain during commutation; IFM is the maximum forward source-drain diode current just prior to the onset of commutation.

 V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

RGS should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, Li in Motorola's test circuit are assumed to be practical minimums.

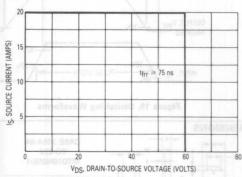


Figure 12. Commutating Safe Operating Area (CSOA)

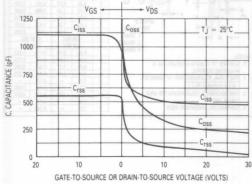


Figure 14. Capacitance Variation

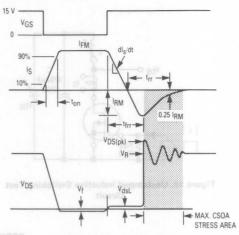


Figure 11. Commutating Waveforms

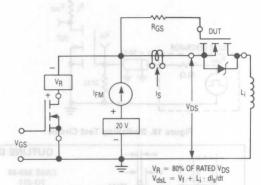


Figure 13. Commutating Safe Operating Area Test Circuit

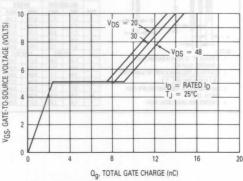


Figure 15. Gate-Charge versus Gate-to-Source Voltage

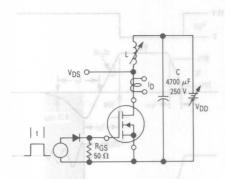


Figure 16. Unclamped Inductive Switching Test Circuit

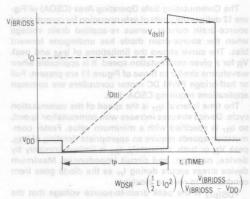


Figure 17. Unclamped Inductive Switching

RESISTIVE SWITCHING

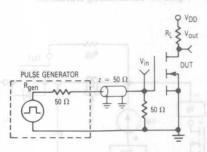


Figure 18. Switching Test Circuit

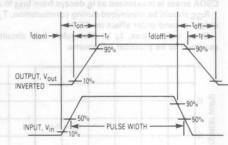
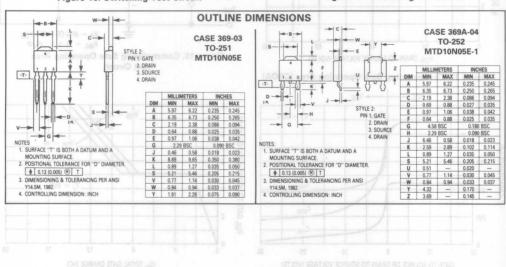


Figure 19. Switching Waveforms



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

TMOS IV N-Channel Enhancement-Mode Power Field Effect Transistor DPAK for Surface or Insertion Mount

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- · Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits.
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode.
- · Diode is Characterized for Use in Bridge Circuits.
- Available With Long Leads, Add -1 Suffix

MAXIMUM RATINGS (T.) = 25°C unless otherwise noted)

Rating	Symbol	MTD3055E	Unit
Drain-Source Voltage	V _{DSS}	60	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	being 860 anv	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed (qvT) V.F (qvT)	I _D	8 20	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	20 0.16	Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	R_{θ} JC R_{θ} JA	6.25 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS			IONA ROADEN	
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	V _{(BR)DSS}	60	1-1	Vdc
Zero Gate Voltage Drain Current (V _{DS} = Rated V _{DS} , V _{GS} = 0) (V _{DS} = 0.8 Rated V _{DS} , V _{GS} = 0, T _J = 125°C)	IDSS	87 = 1 87 = 1	10 80	μΑ

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

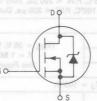
(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves - representing boundaries on device characteristics - are give to facilitate "worst case" design

MTD3055E

TMOS POWER FET 8 AMPERES rDS(on) = 0.15 OHM 60 VOLTS





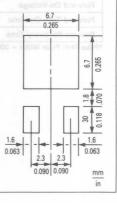


CASE 369A-04 TO-252 MTD3055E



CASE 369-03 TO-251 MTD3055E-1





ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

	Char	acte	ristic					Symbo	ol	Min	Max	Unit	3
FF CHARACTERISTICS (cor	ntinued)												
Zero Gate Voltage Drain C (VDS = Rated VDSS, VC (VDS = Rated VDSS, VC	s = 0	TJ =	125°C)					IDSS	eed	sta_S	10 100	μΑ	31
Gate-Body Leakage Currer	nt, Forwa	ard (GSF =	20 V	dc, VDS	= 0)		IGSS	F	171-1	100	nAdc	N
Gate-Body Leakage Curren	nt, Rever	se (\	GSR =	20 Vc	dc, VDS	= 0)		IGSSI	-	Long	100	nAdc	
N CHARACTERISTICS*	-										13.75 1.1.	125	
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C		V _{GS(t)}	h)	2 1.5	4.5	Vdc							
Static Drain-Source On-Re	sistance	(V _G	s = 10	Vdc, I	D = 4	Adc)	bne r	rDS(o	n)	h on er gy ii	0.15	Ohm	315
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 4 Adc) Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 8 Adc) (I _D = 4 Adc, T _J = 100°C)				V _{DS(o}	9 VO 1	e new ene diod <u>es</u> with high <u>s</u> pee	1.3	Vdc	dia.				
Forward Transconductano	e (V _{DS} =	= 15	V, ID =	4 A)			achin	9FS	to Hou	4	en ese seni	mhos	al-
RAIN-TO-SOURCE AVALAR	NCHE ST	RES	S CAPA	BILITY			-Janagr	ing safe o	mutat	imos bns t	diode speed	gredy sti	ur
Unclamped Inductive Switching Energy See Figures 16 and 17 (ID = 20 A, VDD = 6 V, TC = 25°C, Single Pulse, Non-repetitive) (ID = 8 A, VDD = 6 V, TC = 25°C, P.W. \leq 200 μ s, Duty Cycle \leq 1%) (ID = 3.2 A, VDD = 6 V, TC = 100°C, P.W. \leq 200 μ s, Duty Cycle \leq 1%)				W _{DS}	R	ffer addition e tra <u>ns</u> ient Dio de Des ent S u ppre	3 10 4	temal Sour	a j				
YNAMIC CHARACTERISTIC	cs		-					baqmels	mU -	ne Made	arialisvA sri	Energy in	
Input Capacitance		1	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$			Ciss	080 K	Bleug (cir	500	pF			
Output Capacitance		1	()		= 1 MI		not bell	Coss	(CS)	enin g A rea	300	ditem mo	
Reverse Transfer Capacita	nce	1		See	e Figur	e 14		C _{rss}	-	ridge_Circu	100	Use in Hal	
WITCHING CHARACTERIS	TICS* (T.	1 =	100°C)				8 07 9	derequio	O pini	T y ibvoolet	sbuid nie	7	
Turn-On Delay Time		T	30					td(on	apbin 5	I mi sa U 10	20	ns	ac.
Rise Time			(V _{DD}		v, I _D =		ited ID	tr	muz.	ids, <u>A</u> dd -	60	W aldsliev	
Turn-Off Delay Time					= 50 e Figur	0 18		td(off	F)	seeling O'ds	65	AS MUM	
Fall Time		- 1		21000				tf			65	-	
Total Gate Charge			. /\/		0.0 0-4	1 \/	SOUY	Qg		12 (Typ)	17	nC	a in
Gate-Source Charge					0.8 Rat d I _D , V			Qgs		6.5 (Typ)	- SPIII - B	n-Gats Vel	
Gate-Drain Charge		70			e Figur			Qgd		5.5 (Typ)	100 - 000	-Source V	
OURCE DRAIN DIODE CHA	RACTER	ISTI	CS*			-	ed a] 90	-1	7 041314101	mayo.	1	
Forward On-Voltage		T					Mal	V _{SD}		1.7 (Typ)	2.5	Vdc	
Forward Turn-On Time		8206			= 0.5 R 00 A/μ			ton		2000	by stray inc		(3)
Reverse Recovery Time	+	200	N. O		1.0	. 00		t _{rr}		50 (Typ)	90	ns	
Pulse Test: Pulse Width = 300	μs, Duty	Cycle	≤ 2%.	037 o	- 29-		MA OF	- 11	SHI	and entitioner	nugT sign or	Syrin gride	
	TA	TC											
	2.5	25		- 85	0.0		Bus			ion to Case			
	(S) 2	20		, b,	TV		AUR		1) 208	dn A ot noi			
	WATT	20	1	a	27		1		ani	for Solder			
	NOI (WATTS	15	1	1	T _C				8	or 5 second			
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PRILITANGENERAL

3

TYPICAL FLECTRICAL CHARACTERISTICS

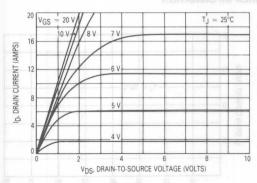


Figure 2. On-Region Characteristics

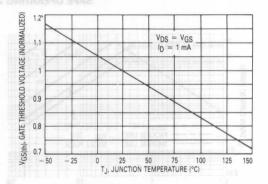


Figure 3. Gate-Threshold Voltage Variation
With Temperature

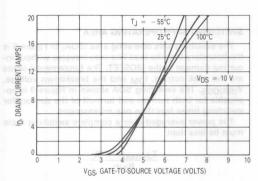


Figure 4. Transfer Characteristics

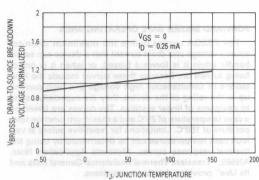


Figure 5. Breakdown Voltage Variation With Temperature

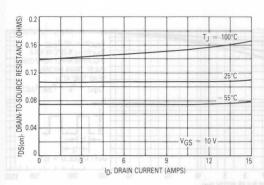


Figure 6. On-Resistance versus Drain Current

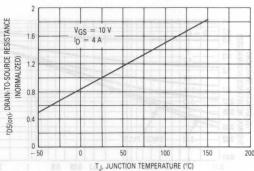


Figure 7. On-Resistance Variation With Temperature

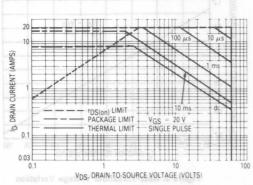


Figure 8. Maximum Rated Forward Biased Safe Operating Area

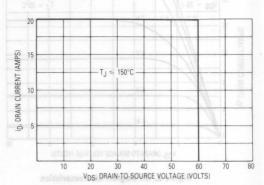


Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

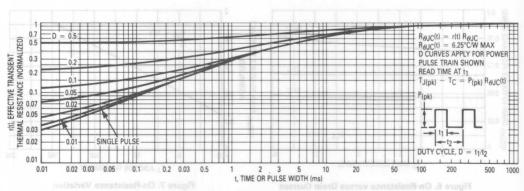


Figure 10. Thermal Response

3

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of IFM and peak VR for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

VDS(pk) is the peak drain-to-source voltage that the device must sustain during commutation; IFM is the maximum forward source-drain diode current just prior to the onset of commutation.

 V_R is specified at 80% of $V_{\left(BR\right)DSS}$ to ensure that the CSOA stress is maximized as IS decays from IRM to zero.

RGS should be minimized addring commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

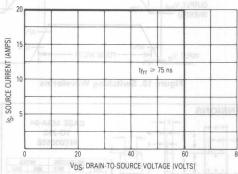


Figure 12. Commutating Safe Operating Area (CSOA)

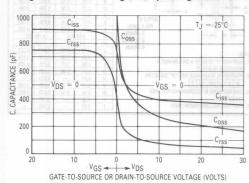


Figure 14. Capacitance Variation

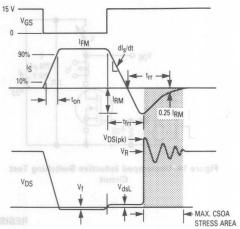


Figure 11. Commutating Waveforms

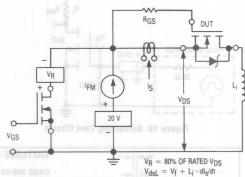


Figure 13. Commutating Safe Operating Area
Test Circuit

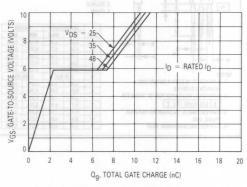


Figure 15. Gate-Charge versus Gate-to-Source Voltage

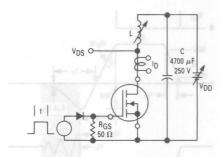


Figure 16. Unclamped Inductive Switching Test Circuit

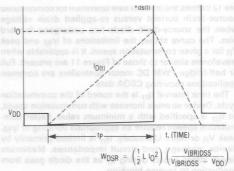


Figure 17. Unclamped Inductive Switching Waveforms

RESISTIVE SWITCHING

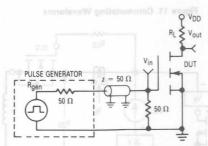


Figure 18. Switching Test Circuit

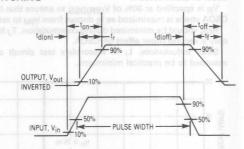
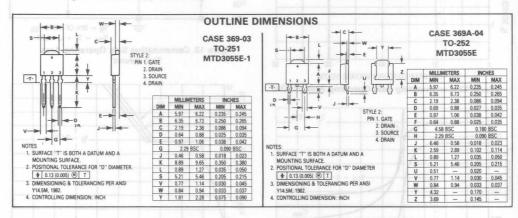


Figure 19. Switching Waveforms



MTM5N100

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor N-Channel Enhancement-Mode

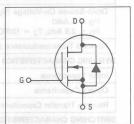
Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FETS
5 AMPERES
rDS(on) = 3 OHMS
950 and 1000 VOLTS



MAXIMUM RATINGS

200	N C I I		MTH o	I I with	
On Rating (qvT) BFF	Og	Symbol 5N95 5N1	5N100	Unit	
Drain-Source Voltage	Qgs	VDSS	950	1000	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	bgD	VDGR	950	1000	Vdc
Gate-Source Voltage — Continuous — Non-repetitive (t _p ≤	50 μs)	V _{GS} V _{GSM}		20 40	Vdc Vpk
Drain Current Continuous Pulsed	no.	I _D		5 7	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PJ	PD		50	Watts W/°C
Operating and Storage Temperature Range		T _J , T _{stg}	-65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta J A}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C



MTM5N95 MTM5N100 CASE 1-06 TO-204AA



MTH5N95 MTH5N100 CASE 340-02 TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) Characteristic Symbol Min Max Unit OFF CHARACTERISTICS Drain-Source Breakdown Voltage V(BR)DSS Vdc $(V_{GS} = 0, I_D = 0.25 \text{ mA})$ MTH/MTM5N95 950 MTH/MTM5N100 1000 mAdc Zero Gate Voltage Drain Current IDSS (VDS = Rated VDSS, VGS = 0) 0.2 $(V_{DS} = 0.8 \text{ Rated } V_{DSS}, V_{GS} = 0, T_{J} = 125^{\circ}C)$ 1 100 nAdc Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0) IGSSF Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0) 100 nAdc **IGSSR** ON CHARACTERISTICS* VGS(th) 2 4.5 Vdc Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_{D} = 1$ mA) $T_J = 100^{\circ}C$ 1.5 4 Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 2.5 Adc) 3 Ohms rDS(on) Drain-Source On-Voltage (VGS = 10 V) V_{DS}(on) Vdc (I_D = 5 Adc) (I_D = 2.5 Adc, T_J = 100°C) 15 12.5 2 Forward Transconductance (VDS = 15 V, ID = 2.5 A) mhos **gFS DYNAMIC CHARACTERISTICS** Input Capacitance Ciss 2600 pF $(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz})$ **Output Capacitance** Coss 350 See Figure 10 Crss Reverse Transfer Capacitance 200 SWITCHING CHARACTERISTICS* (T | = 100°C) Turn-On Delay Time 70 td(on) ns (V_DD = 25 V, I_D = 0.5 Rated I_D Rise Time t_r 250 R_{gen} = 50 ohms) See Figures 12 and 13 Turn-Off Delay Time td(off) 500 Fall Time tf 200 Total Gate Charge Q_g 110 (Typ) 140 nC (VDS = 0.8 Rated VDSS, Gate-Source Charge = Rated I_D, V_{GS} = 10 V) See Figure 11 Qgs 60 (Typ) Q_{gd} Gate-Drain Charge 50 (Typ) SOURCE DRAIN DIODE CHARACTERISTICS* Forward On-Voltage 1.1 (Typ) Vdc VSD 1.5 $(I_S = Rated I_D V_{GS} = 0)$ Forward Turn-On Time Limited by stray inductance ton Reverse Recovery Time 1200 (Typ) trr ns **INTERNAL PACKAGE INDUCTANCE (TO-204)** Internal Drain Inductance Ld 5 (Typ) nH (Measured from the contact screw on the header closer to the source pin and the center of the die) Internal Source Inductance Ls 12.5 (Typ) (Measured from the source pin, 0.25" from the package to the source bond pad) **INTERNAL PACKAGE INDUCTANCE (TO-218)** Internal Drain Inductance Ld nH (Measured from the contact screw on tab to center of die) 4 (Typ) (Measured from the drain lead 0.25" from package to center of die) 5 (Typ) Internal Source Inductance 10 (Typ) Ls (Measured from the source lead 0.25" from package to source bond pad.)

^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

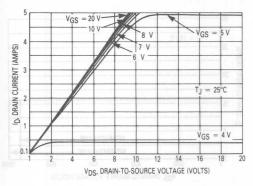


Figure 1. On-Region Characteristics

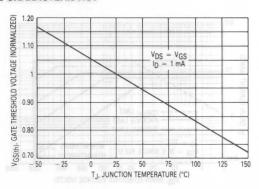


Figure 2. Gate-Threshold Voltage Variation
With Temperature

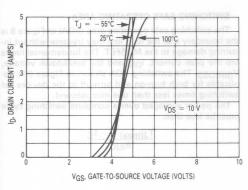


Figure 3. Transfer Characteristics

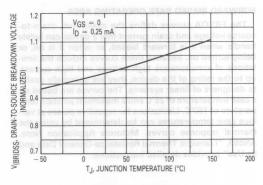


Figure 4. Breakdown Voltage Variation
With Temperature

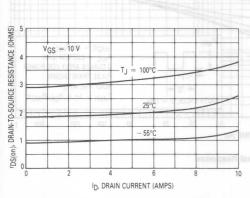


Figure 5. On-Resistance versus Drain Current

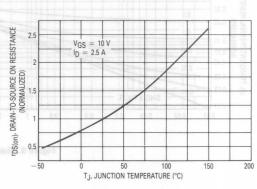


Figure 6. On-Resistance Variation With Temperature

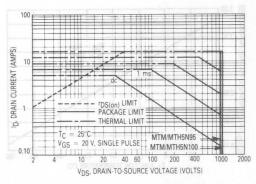


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

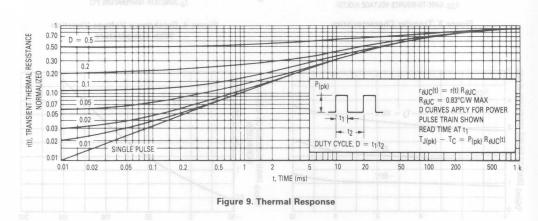
The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

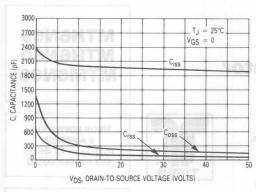
The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

 $\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$



MOTOROLA TMOS POWER MOSFET DATA



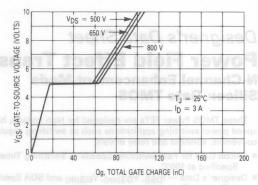


Figure 10. Capacitance Variation

Figure 11. Gate Charge versus Gate-To-Source Voltage

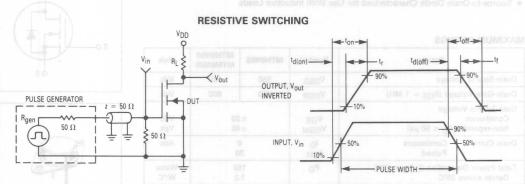
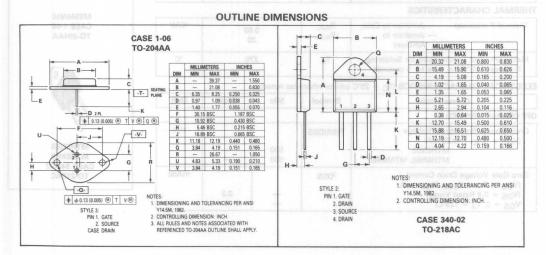


Figure 12. Switching Test Circuit

Figure 13. Switching Waveforms



Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

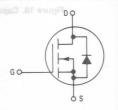
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

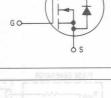
- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MTH6N55 MTH6N60 MTM6N60



TMOS POWER FETS 6 AMPERES rDS(on) = 1.2 OHMS 550 and 600 VOLTS







MTM6N60 **CASE 1-06** TO-204AA



MTH6N55 MTH6N60 **CASE 340-02** TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH6N55	MTH6N60 MTM6N60	Unit
Drain-Source Voltage	VDSS	550	600	Vdc
Drain-Gate Voltage (R _{GS} = 1 M Ω)	VDGR	550	600	Vdc
Gate-Source Voltage Continuous Non-repetitive (t _p ≤ 50 μs)	V _{GS} V _{GSM}		20 40	Vdc Vpk
Drain Current Continuous Pulsed	IDM		6 80	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		50 .2	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{sta}	- 65	to 150	°C

THERMAL CHARACTERISTICS

HEIMINE OHNING	Littorioo			
Thermal Resistance	Junction to Case Junction to Ambient	R _θ JC R _θ JA	0.83 30	°C/W
Maximum Lead Temp Purposes, 1/8" from		TL	275	°C

FLECTRICAL CHARACTERISTICS (To = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS			208 181 A 208 200 MAA 500	18 1
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA) MTH6N55 MTH6N60, MTM6N60	V _{(BR)DSS}	550 600	\$ 815.0 288 8 8860 335 6 6860 0151 7 625 0 015 1 681 0 15 1 681 0 15	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0, TJ = 125°C)	IDSS		0.2	mAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves - representing boundaries on device characteristics - are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^{\circ}C$ unless otherwise noted)

	acteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS			7 Volts J		
Gate-Body Leakage Current, Forwa (VGSF = 20 Vdc, VDS = 0)	rd 8	IGSSF		100	nAdc
Gate-Body Leakage Current, Reversion (VGSR = 20 Vdc, VDS = 0)	se de la companya de	IGSSR		100	nAdc
N CHARACTERISTICS*	I pen 9				-
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C	08.0	V _{GS(th)}	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance	(V _{GS} = 10 Vdc, I _D = 3 Adc)	rDS(on)		1.2	Ohms
Drain-Source On-Voltage ($V_{GS} = 1$) ($I_D = 6$ Adc) ($I_D = 3$ Adc, $T_J = 100^{\circ}$ C)		V _{DS(on)}	8 12 F-TO-SU UI NCE VOLT	9 7.2	Vdc
Forward Transconductance (VDS =	15 V, I _D = 3 A)	9FS	8 10 m2 98-1	7 9 1 0	mhos
YNAMIC CHARACTERISTICS					
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss	_	1800	pF
Output Capacitance	f = 1 MHz)	Coss		350	
Reverse Transfer Capacitance	See Figure 11	C _{rss} .	17 - 1	150	
WITCHING CHARACTERISTICS* (TJ	= 100°C)		Alexander	- 4	
Turn-On Delay Time		td(on)	477-	60	ns
Rise Time	= 100°C) (V _{DD} = 25 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms) See Figures 13 and 14 (V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V) See Figure 12	t _r	AVI -	150	
Turn-Off Delay Time		td(off)		200	
Fall Time		tf	- <u> </u>	120	
Total Gate Charge	(Vpc = 0.8 Rated Vpcc	Qg	55 (Typ)	65	nC
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 V)	Qgs	25 (Typ)		-
Gate-Drain Charge	See Figure 12	Q _{gd}	30 (Typ)	31-1	
OURCE DRAIN DIODE CHARACTER	STICS*		8 1	1	0
Forward On-Voltage	(Is = Rated Ip	V _{SD}	1 (Typ)	1.4	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited by st	ray inductar	nce
Reverse Recovery Time	W	t _{rr}	600 (Typ)	_	ns
TERNAL PACKAGE INDUCTANCE (TO-204)				
Internal Drain Inductance (Measured from the contact screeto the source pin and the center		Ld	5 (Typ)	1000	nH
Internal Source Inductance (Measured from the source pin, to the source bond part)	0.25" from the package	L _S	12.5 (Typ)		
NTERNAL PACKAGE INDUCTANCE (TO-218)				1
Internal Drain Inductance (Measured from screw on tab to (Measured from the drain lead 0.	center of die) 25" from package to center of die)	Ld	4 (Typ) 5 (Typ)		nH
Internal Source Inductance	0.25" from package to center of die)	Ls	10 (Typ) —		

TYPICAL ELECTRICAL CHARACTERISTICS

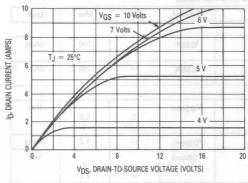


Figure 1. On-Region Characteristics

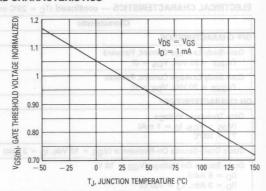


Figure 2. Gate-Threshold Voltage Variation With Temperature

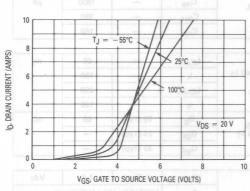


Figure 3. Transfer Characteristics

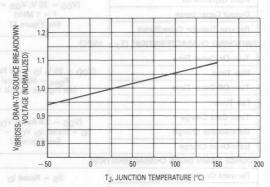


Figure 4. Breakdown Voltage Variation With Temperature

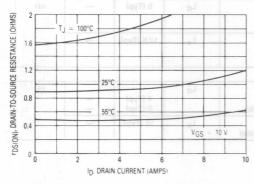


Figure 5. On-Resistance versus Drain Current

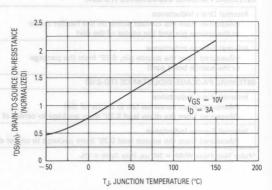


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

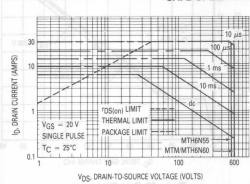


Figure 7. Maximum Rated Forward Biased Safe Operating Area

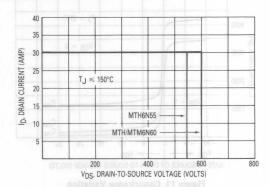


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

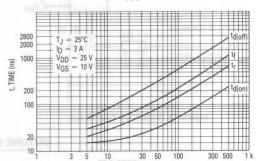


Figure 9. Resistive Switching Time Variation versus Gate Resistance

RG. GATE RESISTANCE (OHMS)

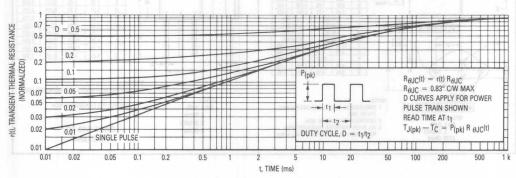
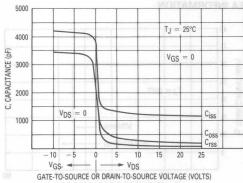


Figure 10. Thermal Response



TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 11. Capacitance Variation

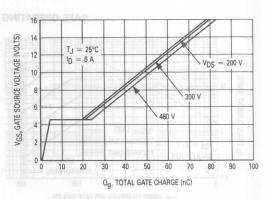


Figure 12. Gate Charge versus
Gate-to-Source Voltage

RESISTIVE SWITCHING

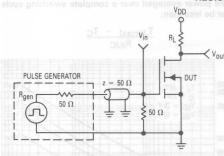


Figure 13. Switching Test Circuit

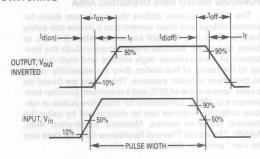
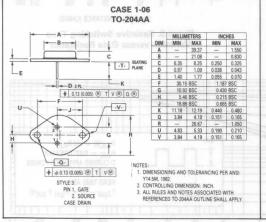
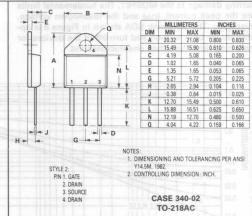


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS





MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

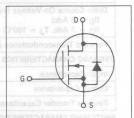
N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times
 Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FETS 6 AMPERES rDS(on) = 3 OHMS 850 and 900 VOLTS



MAXIMUM RATINGS

	2002	17		MTH o	r MTM	
	ON Rating OVER	80	Symbol	6N85	6N90	Unit
Drain-Source V	oltage	agu	V _{DSS}	850	900	Vdc
Drain-Gate Volt (RGS = 1 Ms	0	P80	V _{DGR}	850	900	Vdc
Gate-Source Vo	ltage — Continuous — Non-repetitive (t _p ≤ 50 <i>μ</i> s)	V _{GS} V _{GSM}	C1 20018021 ==	20 40	Vdc Vpk
Drain Current Continuous Pulsed	— (qyT)	412	I _D		6 2	Adc
	ssipation @ T _C = 25°C 25°C	6-J	PD		50	Watts
Operating and	Storage Temperature Ra	nge	T _J , T _{stg}	- 65 1	to 150	°C

THERMAL CHARACTERISTICS

TETRINE OF PRIDATE LINE LINE			
Thermal Resistance — Junction to Case — Junction to Ambient	R _θ JC R _θ JA	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C



MTM6N85 MTM6N90 CASE 1-06 TO-204AA



MTH6N85 MTH6N90 CASE 340-02 TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

	Characterist	ic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS		William III					
Drain-Source Breakdown V (VGS = 0, ID = 0.25 mA		MTH/MTM MTH/MTM		V(BR)DSS	850 900	er <u>'s</u> L	Vdc
Zero Gate Voltage Drain Cu (VDS = Rated VDSS, VG (VDS = 0.8 Rated VDSS,	S = 0)	= 125°C)	ran: io	IDSS	id Eff	0.2	mAdo
Gate-Body Leakage Current				IGSSF	20M	100	nAdc
Gate-Body Leakage Current	t, Reverse (VGS	R = 20 Vdc, V _{DS} = 0)		IGSSR	_	100	nAdc
ON CHARACTERISTICS*		dgli	voltage, h	ned for high	gradb era at	H TOWER HE	se rivida
Gate Threshold Voltage (V _I T _J = 100°C	THE PROPERTY OF THE PARTY OF TH			V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 3 Adc)			rDS(on)	rie Bilinerie	3	Ohms	
Drain-Source On-Voltage (\(\langle \text{ID} = 6 \text{ Adc} \right) \(\langle \text{ID} = 3 \text{ Adc, T} \text{J} = 100^{\circ} \text{C}		d SOA Specified (V 0		V _{DS(on)}	L VDS(en)- lure — er Di ss leetle	18 14.4	Vdc
Forward Transconductance		D = 3 A) about ev	its Industr	9FS	2	rain <u>Di</u> ode	mhos
DYNAMIC CHARACTERISTICS				0,0			
Input Capacitance		/Vpa = 25 V Va	. 0	C _{iss}		2600	pF
Output Capacitance		(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 10		Coss	_	350	
Reverse Transfer Capacitan	ice			C _{rss}	_	200	
SWITCHING CHARACTERIST	ICS* (TJ = 100	°C)					
Turn-On Delay Time				[†] d(on)	_	70	ns
Rise Time	(V	$I_{DD} = 25 \text{ V}, I_{D} = 0.5 \text{ R}$		t _r	_	200	IS MUM
Turn-Off Delay Time		R _{gen} = 50 ohms See Figures 12 and		td(off)	-	500	
Fall Time		MIN vo HIM		tf	-	200	
Total Gate Charge	zimU -	(VDS = 0.8 Rated VD	Symbol	Qg	110 (Typ)	140	nC
Gate-Source Charge	480/	ID = Rated ID, VGS =		Qgs	60 (Typ)	enerist	econocan
Gate-Drain Charge	5517	See Figure 11	anny	Q_{gd}	50 (Typ)	sosti	n-Gatte-V
SOURCE DRAIN DIODE CHAP	RACTERISTICS*		enuran			(63)	GS = 1 N
Forward On-Voltage	bbV	(I _S = Rated I _D	VGS	V _{SD}	1.1 (Typ)	0 —1.5 mlo	Vdc
Forward Turn-On Time	NOV.	$V_{GS} = 0$	MSbA	ton	Limited	by stray ind	uctance
Reverse Recovery Time	Adc		and the second	t _{rr}	(Typ)	_	ns
NTERNAL PACKAGE INDUCT	TANCE (TO-204	22	1001				lsed
Internal Drain Inductance (Measured from the cont to the source pin and the			gq -	L _d	5 (Typ)	Neslp ul on 6 le 26°C	16WnH
Internal Source Inductance (Measured from the sour to the source bond pad)	ce pin, 0.25" fro	om the package	Sup.	L _S	12.5 (Typ)	ARACTERIS	MAL CH
NTERNAL PACKAGE INDUCT	TANCE (TO-218	30	Atafi	109	dmA or notion	ut.—	
Internal Drain Inductance (Measured from the cont			dia)	L _d	4 (Typ)	d femperat 8' fr <u>em</u> cas	nH
(Measured from the drain Internal Source Inductance (Measured from the sour				L _S	5 (Typ) 10 (Typ)	_	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

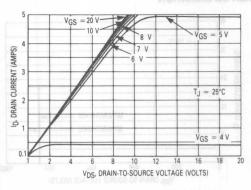


Figure 1. On-Region Characteristics

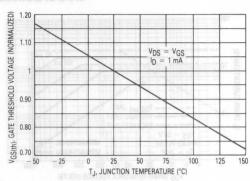


Figure 2. Gate-Threshold Voltage Variation
With Temperature

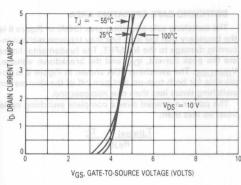


Figure 3. Transfer Characteristics

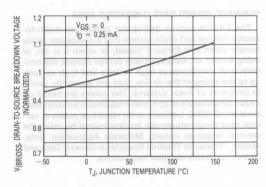


Figure 4. Breakdown Voltage Variation With Temperature

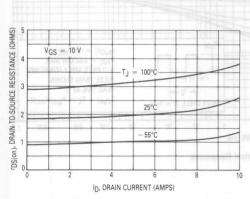


Figure 5. On-Resistance versus Drain Current

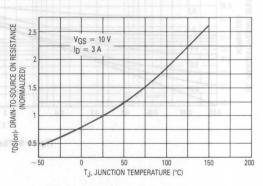


Figure 6. On-Resistance Variation With Temperature

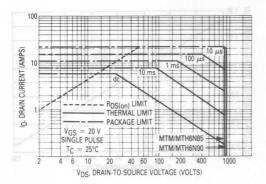


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

40 T_J ≤ 150°C 32 24 24 40 MTM/MTH6N85 40 0 0 200 400 600 806 1000 V_{DS}, DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 8. Maximum Rated Switching Safe Operating Area

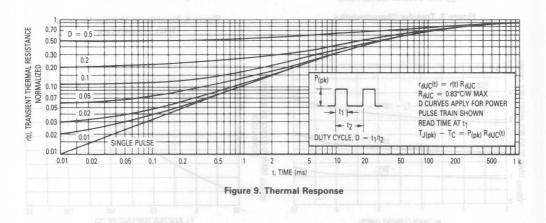
FORWARD BIASED SAFE OPERATING AREA

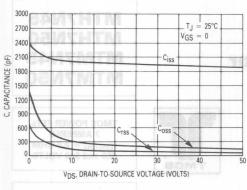
The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:





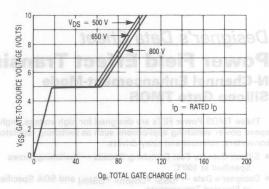


Figure 10. Capacitance Variation

Figure 11. Gate Charge versus Gate-to-Source Voltage

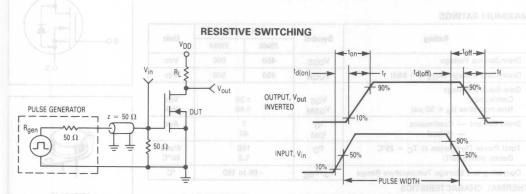
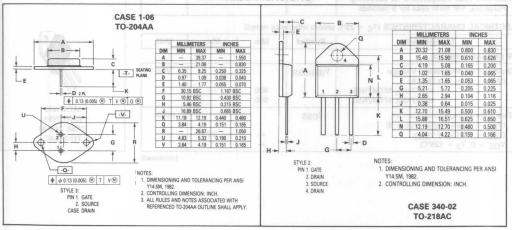


Figure 12. Switching Test Circuit

Figure 13. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

D. et	2 201	MTH o	MTH or MTM		
Rating	Symbol	7N45	7N50	Unit	
Drain-Source Voltage	V _{DSS}	450	500	Vdc	
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	450	500	Vdc	
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50~\mu s$)	V _{GS} V _{GSM}	######################################		Vdc Vpk	
Drain Current — Continuous — Pulsed	I _D	7 40		Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	ED-FEILMI	50 .2	Watts W/°C	
Operating and Storage Temperature Range	TJ, Tstg	- 65	to 150	°C	

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TENO SI	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

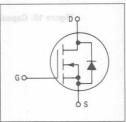
Characteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS	DALH	- 1		HAT HELL
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA) MTH7N45, MTM7N45 MTH7N50, MTM7N50	V(BR)DSS	450 500	353 369 434 32 353 73 1100 353 1100 353	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0$) ($V_{DS} = 0.8\ Rated\ V_{DSS},\ V_{GS} = 0$, $T_{J} = 125^{\circ}C$)	IDSS	- 100	0.2	mAdc

(continued)

MTH7N45 MTH7N50 MTM7N45 MTM7N50



TMOS POWER FETS 7 AMPERES rDS(on) = 0.8 OHM 450 and 500 VOLTS





MTM7N45 MTM7N50 CASE 1-06 TO-204AA



MTH7N45 MTH7N50 CASE 340-02 TO-218AC

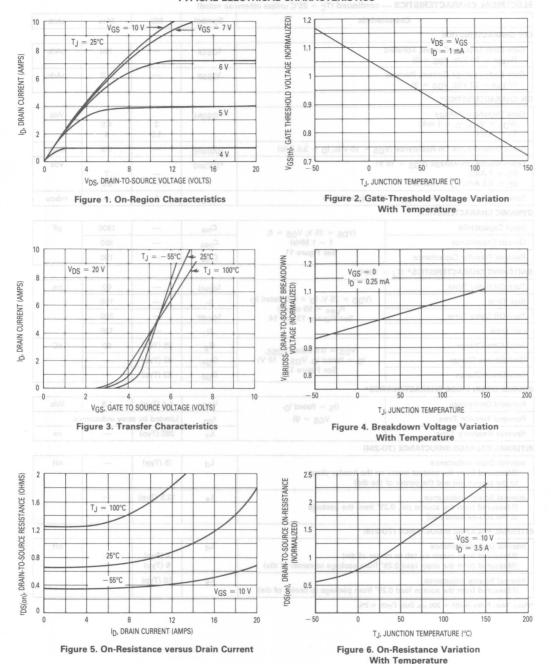
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Ch	aracteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS		GOT TO		1900	
Gate-Body Leakage Current, Forv (VGSF = 20 Vdc, VDS = 0)	vard	IGSSF		100	nAdc
Gate-Body Leakage Current, Revo	erse	IGSSR		100	nAdc
N CHARACTERISTICS*	- Log 6				
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$ $T_{J} = 100^{\circ}\text{C}$	10 55	VGS(th)	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	e (V _{GS} = 10 Vdc, I _D = 3.5 Adc)	rDS(on)	-	0.8	Ohm
Drain-Source On-Voltage (V _{GS} = $(I_D = 7 \text{ Adc})$ $(I_D = 3.5 \text{ Adc}, T_J = 100^{\circ}\text{C})$		VDS(on)	12 SOURCE VOLTAGE	7 5.6	Vdc
Forward Transconductance (VDS	= 10 V, I _D = 3.5 A)	9FS	s set 2 diper	eruo / eruo	mhos
YNAMIC CHARACTERISTICS	MIN				
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss	_	1800	pF
Output Capacitance	f = 1 MHz	Coss	_	350	
Reverse Transfer Capacitance	See Figure 11	C _{rss}	(0188 LT	150	
WITCHING CHARACTERISTICS* (T _J = 100°C)	37001 = (1 +4)	11	Vos =	Yos
Turn-On Delay Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms) See Figures 13 and 14	t _{d(on)}	W-I	60	ns
Rise Time		t _r	1/1/1-	150	
Turn-Off Delay Time		t _d (off)	1	200	
Fall Time	950 Hgarlo 10 and 1	tf		120	
Total Gate Charge	0.0 Detect V	Qq	55 (Typ)	60	nC
Gate-Source Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V)	Q _{qs}	32 (Typ)		
Gate-Drain Charge	See Figure 12	Q _{gd}	23 (Typ)		
OURCE DRAIN DIODE CHARACTE	RISTICS*	94		N.S.	
Forward On-Voltage	(IS = Rated ID	V _{SD}	1.4 (Typ)	1.8	Vdc
Forward Turn-On Time	$V_{GS} = 0$	ton	Limited by stray inductance		
Reverse Recovery Time	Figure 4. Bro	t _{rr}	280 (Typ)	gure 3. Tra	ns
TERNAL PACKAGE INDUCTANCE	E (TO-204)				
Internal Drain Inductance (Measured from the contact so to the source pin and the center		L _d	(5 (Typ)	-	nH
Internal Source Inductance (Measured from the source pin to the source bond pad)		L _S	12.5 (Typ)	1,1 = 100°C	
ITERNAL PACKAGE INDUCTANCE	E (TO-218)				
Internal Drain Inductance (Measured from screw on tab		L _d	4 (Typ) 5 (Typ)	_ 07 0	nH
Internal Source Inductance	d 0.25" from package to center of die)	Ls	10 (Typ)	2.55	
Pulse Test: Pulse Width ≤ 300 µs. Duty		1	-		

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS



SAFE OPERATING AREA INFORMATION

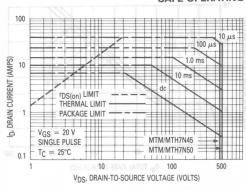


Figure 7. Maximum Rated Forward Biased Safe Operating Area

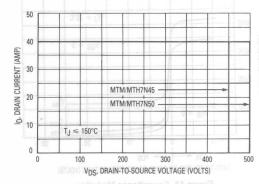


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

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SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

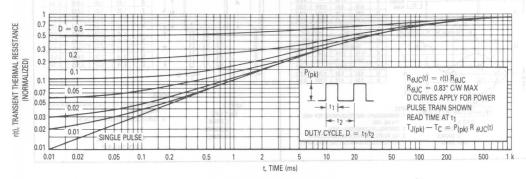
TJ(max) - TC

RG, GATE RESISTANCE (OHMS)

30 50

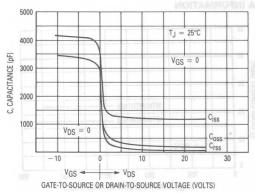
300 500 1 k

Figure 9. Resistive Switching Time Variation versus Gate Resistance



20

Figure 10. Thermal Response



T_J = 25°C 400 V V_{DS} = 165 V V_{DS} = 165 V V_{DS} = 165 V V_{DS} = 100 V_{QS}, TOTAL GATE CHARGE (nC)

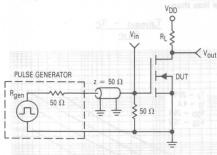
Figure 11. Capacitance Variation

Figure 12. Gate Charge versus

Gate-to-Source Voltage

-toff-

RESISTIVE SWITCHING



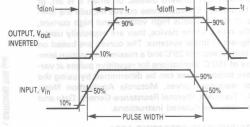
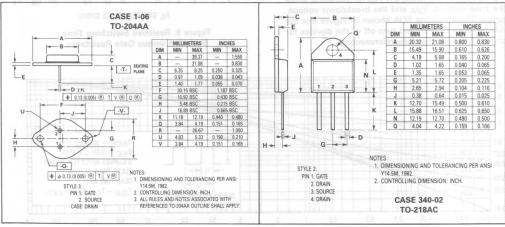


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

150	Cras	MTH or MTM		Unit
Rating	Symbol	8N35	8N40	Onit
Drain-Source Voltage	V _{DSS}	350	400	Vdc
Drain-Gate Voltage (R _{GS} = 1 MΩ)	VDGR	350	400	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	IDM	(V) = 0.8 Fa 8.0 = 20 (V) = 48 - 10 V)		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	bg ^O P _D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stg}	-65	to 150	°C

THERMAL CHARACTERISTICS

TETRINITE OTTATION OF THE STATE			
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L	275	°C

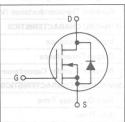
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

С	haracteristic	Symbol	Min	Max	Unit
OFF CHARACTERIS	TICS			s package	25" from ti
Drain-Source Bre		V(BR)DSS			Vdc
Hin	MTH8N35, MTM8N35 MTH8N40, MTM8N40	Pr	350 400	_ (4	
Zero Gate Voltag	e Drain Current	IDSS	(eib lib te	ckage to cant	mAdc
(V _{DS} = Rated (V _{DS} = 0.8 Ra V _{GS} = 0, T _J =		a-l	(sil o T o retr	0.2	

(continued)

MTH8N35 MTH8N40 MTM8N35 MTM8N40

TMOS POWER FETS 8 AMPERES rDS(on) = 0.55 OHM 350 and 400 VOLTS





MTM8N35 MTM8N40 CASE 1-06 TO-204AA



MTH8N35 MTH8N40 CASE 340-02 TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Rise Time

Fall Time

Turn-Off Delay Time

Total Gate Charge

Gate-Drain Charge

Gate-Source Charge

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted) Characteristic Symbol Min Max Unit **OFF CHARACTERISTICS** Gate-Body Leakage Current, Forward IGSSF 100 nAdc $(V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0)$ Gate-Body Leakage Current, Reverse 100 nAdd IGSSR $(V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0)$ **ON CHARACTERISTICS*** Gate Threshold Voltage Vdc VGS(th) (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C 4.5 1.5 4 Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 4 Adc) 0.55 Ohm rDS(on) Drain-Source On-Voltage (VGS = 10 V) Vdc VDS(on) $(I_D = 8 Adc)$ 5.3 $(I_D = 4 \text{ Adc}, T_J = 100^{\circ}\text{C})$ 4.4 Forward Transconductance (VDS = 10 V, ID = 4 A) 3 mhos 9FS DYNAMIC CHARACTERISTICS Input Capacitance Ciss 1800 pF $(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ **Output Capacitance** f = 1 MHzCoss 350 See Figure 11. Reverse Transfer Capacitance Crss 150 SWITCHING CHARACTERISTICS* (T. = 100°C) Turn-On Delay Time 60 td(on) ns ($V_{DD} = V$, $I_D = 0.5$ Rated I_D

SOURCE DRAIN DIODE CHARACTER	RISTICS*				
Forward On-Voltage	(IS = Rated ID	V _{SD}	1.4 (Typ)	1.8	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited by stray inductance		nce
Reverse Recovery Time	V/\000000	⊃L8 ² t _{rr}	280 (Typ)	onutto	ns

Rgen = 50 ohms)

See Figures 13 and 14

(VDS = 0.8 Rated VDSS,

ID = Rated ID, VGS = 10 V)

See Figure 12

tr

td(off)

tf

 Q_g

 Q_{gs}

 Q_{gd}

150

200

120

60

nC

55 (Typ)

32 (Typ)

23 (Typ)

INTERNAL PACKAGE INDUCTANCE (TO-204) Internal Drain Inductance L_d (5 (Typ) (Measured from the contact screw on the header closer to the source pin and the center of the die) Internal Source Inductance Ls 12.5 (Typ) (Measured from the source pin, 0.25" from the package to the source bond pad)

NTERNAL PACKAGE INDUCTANCE (TO-218)	and addition.			
Internal Drain Inductance (Measured from screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L _d	4 (Typ) 5 (Typ)	MTH8Nd MIH8Nd	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to center of die)	L _S	10 (Typ)	- 4 Apse-	102 = 0 a Harad A

^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

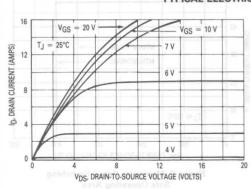


Figure 1. On-Region Characteristics

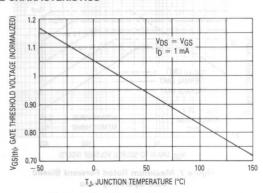


Figure 2. Gate-Threshold Voltage Variation
With Temperature

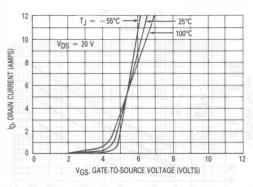


Figure 3. Transfer Characteristics

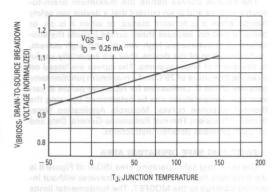


Figure 4. Breakdown Voltage Variation
With Temperature

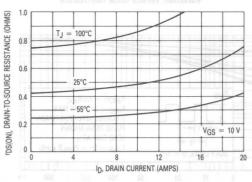


Figure 5. On-Resistance versus Drain Current

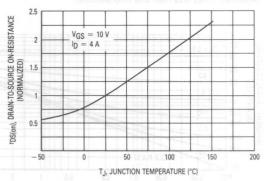


Figure 6. On-Resistance Variation With Temperature

Figure 7. Maximum Rated Forward Biased Safe Operating Area

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

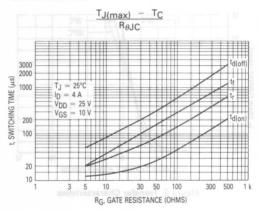


Figure 9. Resistive Switching Time Variation versus Gate Resistance

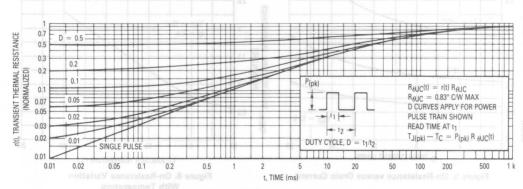
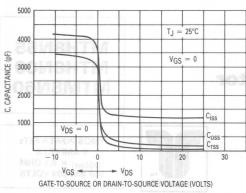


Figure 10. Thermal Response



GATE SOURCE VOLTAGE (VOLTS) T_J = 25°C $I_D = 8 A$ 400 V 250 V VDS = 165 V VGS 20 40 60 80 100 Qg, TOTAL GATE CHARGE (nC)

Figure 11. Capacitance Variation

belloged AOS bas Figure 12. Gate Charge versus Gate-to-Source Voltage

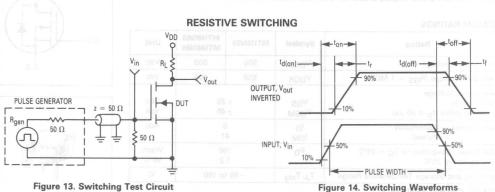
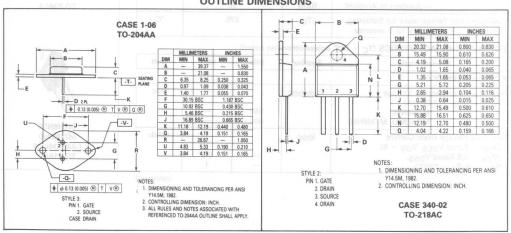


Figure 13. Switching Test Circuit

OUTLINE DIMENSIONS



Designer's Data Sheet

Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

Rating	Symbol	MTH8N55	MTH8N60 MTM8N60	Unit
Drain-Source Voltage	VDSS	550	600	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	550	600	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50~\mu s$)	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	8 41		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	150 1.2		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta J A}$	0.83	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L a	275	°C

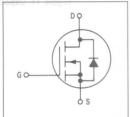
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS		DE0.0	- 1 90.75 585.0 (53.8 ft	E SIGNAL
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA) MTH8N55 MTH8N60, MTM8N60	V(BR)DSS	550 600	7000 201 5 800 77 1 0 81 7 208 61 0 62 6 208 610 61 0 208 610 61 0 208 610	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0, TJ = 125°C)	IDSS	- 14 - 150 s - 150 s - 150 s	0.2	mAdc

MTH8N55 MTH8N60 MTM8N60



TMOS POWER FETS 8 AMPERES rDS(on) = 0.5 OHM 550 and 600 VOLTS





MTM8N60 **CASE 1-06** TO-204AA



MTH8N55 MTH8N60 CASE 340-02 TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

	Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	7.00	The state of the s	1		
Gate-Body Leakage Current, For (VGSF = 20 Vdc, VDS = 0)	prward En &	IGSSF	-	100	nAdo
Gate-Body Leakage Current, R (VGSR = 20 Vdc, VDS = 0)	everse	IGSSR	-	100	nAdd
ON CHARACTERISTICS*	8.0 3				
Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 1$ mA) $I_J = 100^{\circ}C$		VGS(th)	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resista	Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 4 Adc)		e Rogino Che	0.5	Ohm
Drain-Source On-Voltage (V_{GS}) ($I_{D} = 8$ Adc) ($I_{D} = 4$ Adc, $T_{J} = 100^{\circ}$ C)	; = 10 V)	V _{DS(on)}	_	5 4	Vdc
Forward Transconductance (V	$DS = 10 \text{ V}, I_D = 4 \text{ A})$	9FS	4	_	mhos
DYNAMIC CHARACTERISTICS	100		1///	-3187 L	
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0,	C _{iss}		2300	pF
Output Capacitance	f = 1 MHz)	Coss		425	
Reverse Transfer Capacitance	See Figure 11	C _{rss}		180	
WITCHING CHARACTERISTICS	* (T _J = 100°C)				
Turn-On Delay Time	W. T. W.	t _{d(on)}		70	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r		160	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 13 and 14	td(off)	- 1	430	
Fall Time	- RO -	tf	- 1	200	
Total Gate Charge	(Vps = 0.8 Rated Vpss,	Ωg	127 (Typ)	150	nC
Gate-Source Charge	$I_D = Rated I_D, V_{GS} = 10 V$	Qgs	62 (Typ)	STAO_opV.	
Gate-Drain Charge	See Figure 12	Q _{gd}	65 (Typ)	ot s annui	
SOURCE DRAIN DIODE CHARAC	TERISTICS*	9017031000			
Forward On-Voltage	(I _S = Rated I _D	V _{SD}	1.2 (Typ)	2	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited by st	ray inductar	ice
Reverse Recovery Time	181	t _{rr}	500 (Typ)		ns
NTERNAL PACKAGE INDUCTAR	ICE (TO-204)				i i
Internal Drain Inductance (Measured from the contact to the source pin and the ce		Ld	5 (Typ)	-	nH
Internal Source Inductance (Measured from the source to the source bond pad)	pin, 0.25" from the package	L _S	12.5 (Typ)	1.11	
NTERNAL PACKAGE INDUCTAR	ICE (TO-218)	41		J'én	
Internal Drain Inductance (Measured from screw on to (Measured from the drain le	b to center of die) ad 0.25" from package to center of die)	L _d	4 (Typ) 5 (Typ)		nH
Internal Source Inductance	lead 0.25" from package to center of die)	L _S	10 (Typ)	10 17 -	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

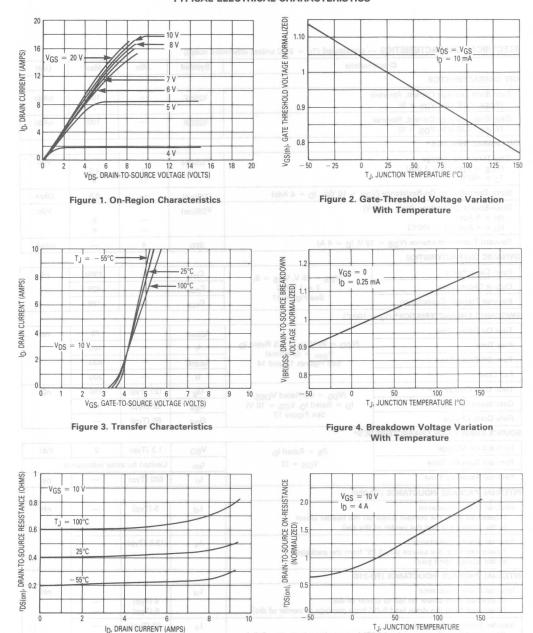


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation
With Temperature

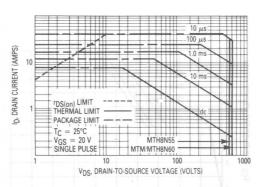


Figure 7. Maximum Rated Forward Biased Safe Operating Area

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

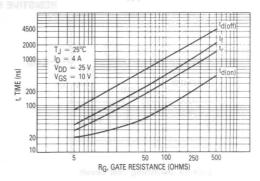


Figure 9. Resistive Switching Time Variation
With Gate Resistance

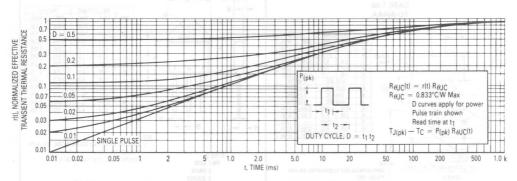


Figure 10. Thermal Response



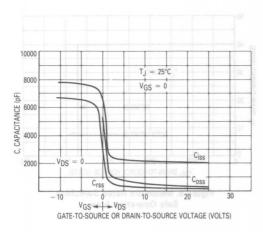


Figure 11. Capacitance Variation

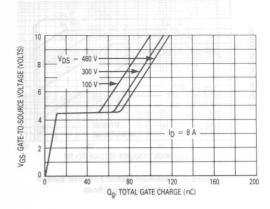


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

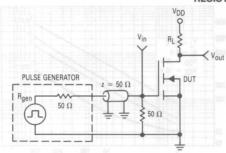


Figure 13. Switching Test Circuit

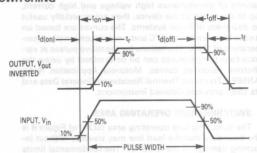
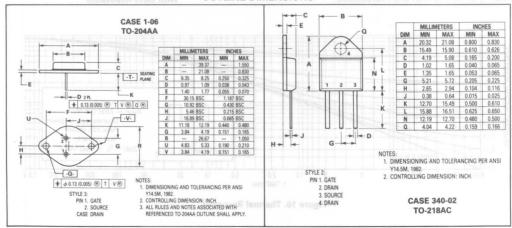


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

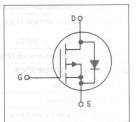
P-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FETS 8 AMPERES rDS(on) = 0.7 OHM 180 and 200 VOLTS



MAXIMUM RATINGS

D-4i	0	MTH o	r MTM	(3°80) =
Rating	Symbol	8P18	8P20	Unit
Drain-Source Voltage	V _{DSS}	180	200	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	180	200	Vdc
	V _{GS} V _{GSM}	±:		Vdc Vpk
Drain Current Continuous Submi ye ta ya belimul Pulsed (qy1) 068 mil	I _D	() neve () 8	3eaV	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	12 1	25 I	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 t	o 150	e t en°C

THERMAL CHARACTERISTICS

Thermal Resistance	2-1		°C/W
Junction to Case Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1 30	ed) movi "d
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C



MTM8P18 MTM8P20 CASE 1-04 TO-204AA



MTH8P18 MTH8P20 CASE 340-02 TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Cha	racteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)		MTH/MTM8P18 MTH/MTM8P20	V _{(BR)DSS}	180 200	s Dat Stall	Vdc
Zero Gate Voltage Drain Current $(V_{DS} = Rated V_{DSS}, V_{GS} = 0)$ $(V_{DS} = Rated V_{DSS}, V_{GS} = 0,$	T _J = 125°	c)	IDSS	comen	10 100	μAdc
Gate-Body Leakage Current, Forwa	ard (VGSF	$=$ 20 Vdc, $V_{DS} = 0$)	IGSSF	_	100	nAdc
Gate-Body Leakage Current, Rever	se (VGSR	= 20 Vdc, V _{DS} = 0)	IGSSR	pang is ab or	100	nAdc
ON CHARACTERISTICS*		ching regu-	such as swib	applications	pnido.iwa	nawad paad
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C		Times	V _{GS(th)}	2 1.5	4.5	on Cate to
Static Drain-Source On-Resistance	Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 4 Adc)			100 SC	0.7	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 8 Adc) (I _D = 4 Adc, T _{.I} = 100°C)			V _{DS(on)}	issipation U racte <u>nz</u> ed fo	7 6	Vdc og
Forward Transconductance (V _{DS}	= 15 V, In	= 4 A)	9FS	2	_	mhos
DYNAMIC CHARACTERISTICS			-10			
Input Capacitance		//pa = 25 V Vaa = 0	Ciss	_	1600	pF
Output Capacitance		- (V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 10		_	400	1
Reverse Transfer Capacitance				_	120	ETAR MUN
SWITCHING CHARACTERISTICS* (T	J = 100°C)	METRS to HERM	C _{rss}			
Turn-On Delay Time	nau	ecos arge loca	t _{d(on)}	_	40	ns
Rise Time	(VDI	$_{\rm D}$ = 25 V, $I_{\rm D}$ = 0.5 Rated $I_{\rm D}$	t _r	_	120	loV scrups Vol
Turn-Off Delay Time	obV	R _{gen} = 50 ohms) See Figures 11 and 12	td(off)	_	100	erioV erso-r
Fall Time			tf	_	80	10M F = 88
SOURCE DRAIN DIODE CHARACTER	ISTICS*	GS ± 20	V	51/01/1	age — Contin	Source Volt
Forward On-Voltage	ada	(IS = Rated ID	V _{SD}	2 (Typ)	4.5	Vdc
Forward Turn-On Time	Adip	VGS = 0)	ton	Limited	by stray ind	uctance
Reverse Recovery Time			t _{rr}	350 (Typ)		ns bea
NTERNAL PACKAGE INDUCTANCE	(TO-204)	g21 Q,		= 25°C	parion (a) Tc	Power Dissi
Internal Drain Inductance (Measured from the contact screeto to the source pin and the center			Ld	5 (Typ)	orage Tampa ACTERISTIC	Hn Shop and S
Internal Source Inductance (Measured from the source pin, to the source bond pad)	0.25" from	the package	L _S	12.5 (Typ)		mal Pegistan nation to Ca
NTERNAL PACKAGE INDUCTANCE	(TO-218)	275		ior Saldering	enute service	T base mure
Internal Drain Inductance (Measured from the contact scre (Measured from the drain lead (L _d	4 (Typ) 5 (Typ)	rom case fo	"8\" nH oq
Internal Source Inductance	0.25" from	n package to source bond pad.	L _S	10 (Typ)	_	

^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

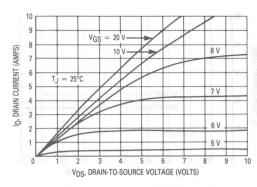


Figure 1. On-Region Characteristics

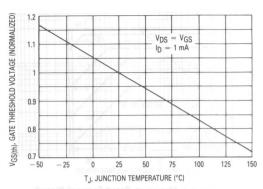


Figure 2. Gate-Threshold Voltage Variation
With Temperature

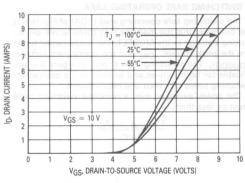


Figure 3. Transfer Characteristics

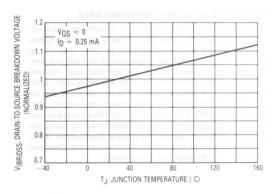


Figure 4. Breakdown Voltage Variation
With Temperature

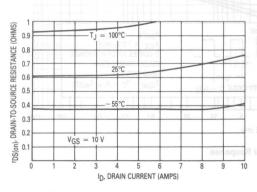


Figure 5. On-Resistance versus Drain Current

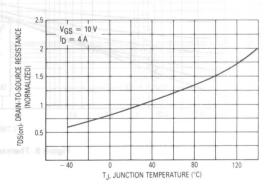


Figure 6. On-Resistance Variation
With Temperature

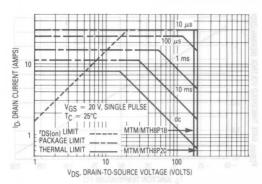


Figure 7. Maximum Rated Forward Biased Safe Operating Area

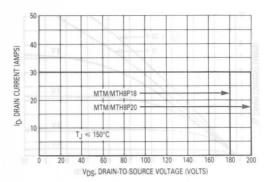


Figure 8. Maximum Rated Switching Safe Operating Area

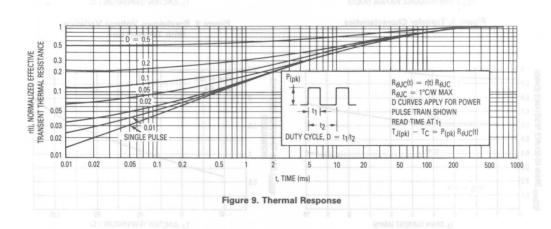
FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$



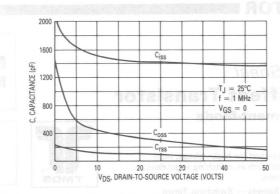
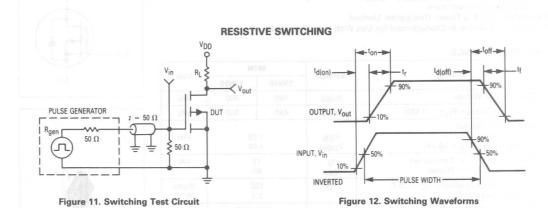
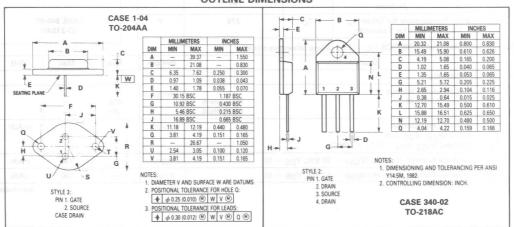


Figure 10. Capacitance Variation



OUTLINE DIMENSIONS



3

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

Rating	0	M	TH	ill Hair
Rating	Symbol	13N45	13N50	Unit
Drain-Source Voltage	V _{DSS}	450	500	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	450	500	Vdc
Gate-Source Voltage Continuous Non-repetitive $(t_p \le 50 \ \mu s)$	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	IDM	13 60		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		50 .2	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	- 65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance	Junction to Case Junction to Ambient	R _θ JC R _θ JA	0.83	°C/W
	perature for Soldering case for 5 seconds	TL ³	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

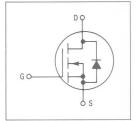
Characteristic		Symbol	Min	Max	Unit		
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)	MTH13N45 MTH13N50	V(BR)DSS	450 500	= -	Vdc		
Zero Gate Voltage Drain Current (Vps = Rated Vpss, Vgs = 0) (Vps = 0.8 Rated Vpss, Vgs = 0, Tj = 125°C)	0800 0800 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			0.2	mAdc		
Gate-Body Leakage Current, Forward (V _{GSF} = 20 Vdc, V _{DS} = 0)	este feró era	IGSSF	-	100	nAdc		
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)		IGSSR		100	nAdc		

(continued)

MTH13N45 MTH13N50



TMOS POWER FETs 13 AMPERES $r_{DS(on)} = 0.4 \text{ OHM}$ 450 and 500 VOLTS





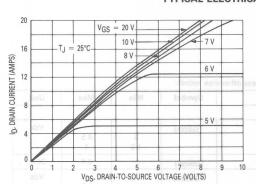
CASE 340-02 TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are give to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS continued (To = 25°C unless otherwise noted

Chara	acteristic	Symbol	Min	Max	Unit
N CHARACTERISTICS*	E.U. 56				
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C	5.0 34	VGS(th)	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	(V _{GS} = 10 Vdc, I _D = 7 Adc)	rDS(on)	-	0.4	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 13 Adc) (I _D = 7 Adc, T _J = 100°C)		V _{DS(on)}	N-TO SOURCE VC	5.2 5	Vdc
Forward Transconductance (VDS =	10 V, I _D = 7 A)	9FS	5	_	mhos
YNAMIC CHARACTERISTICS					
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss	_	3000	pF
Output Capacitance	f = 1 MHz)	Coss	-	500	
Reverse Transfer Capacitance	See Figure 11	C _{rss}	(0.8. — 1.1)	200	
WITCHING CHARACTERISTICS* (TJ	= 100°C)	700°C			
Turn-On Delay Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _{d(on)}	M -	60	ns
Rise Time		t _r	181 T	180	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 13 and 14	td(off)	7//-	450	
Fall Time	9058	tf	//-	180	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Ωg	110 (Typ)	160	nC
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 V)	Qgs	50 (Typ)		
Gate-Drain Charge	See Figure 12	Qgd	60 (Typ)		
OURCE DRAIN DIODE CHARACTERI	STICS*				
Forward On-Voltage	(I _S = Rated I _D	V _{SD}	1.1 (Typ)	1.4	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited by st	ray inductan	се
Reverse Recovery Time		t _{rr}	1200 (Typ)	_	ns
ITERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L _d	4 (Typ) 5 (Typ)	_	nH
Internal Source Inductance (Measured from the source lead	0.25" from package to center of die)	L _S	10 (Typ)	- 1	

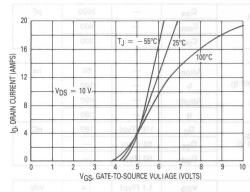
^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



1.1 VDS = VGS ID = 1 mA VDS = VGS ID = VGS ID = 1 mA VDS = VGS ID = VGS ID = 1 mA VDS = VGS ID = VGS ID = 1 mA VDS = VGS ID = VGS I

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



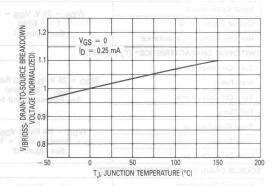
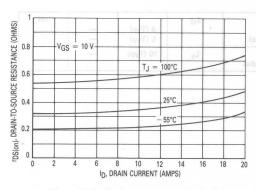


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation With Temperature



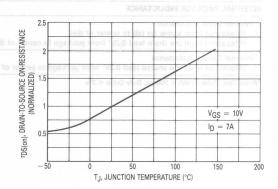


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation
With Temperature

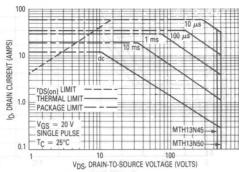


Figure 7. Maximum Rated Forward Biased Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

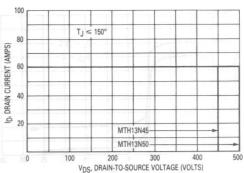


Figure 8. Maximum Rated Switching Safe Operating Area

Figure 9. Resistive Switching Time Variation With Gate Resistance

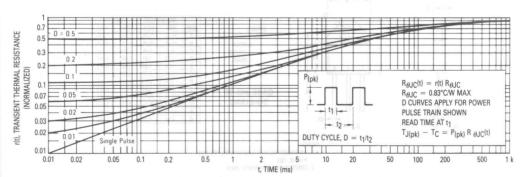


Figure 10. Thermal Response

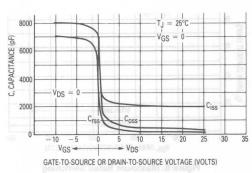


Figure 11. Capacitance Variation

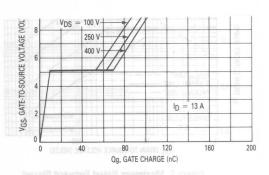


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

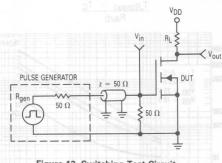


Figure 13. Switching Test Circuit

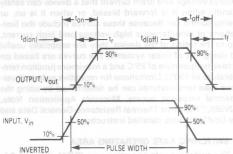
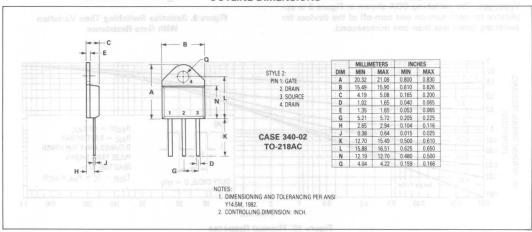


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

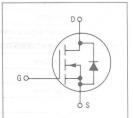
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTH15N20 MTM15N20

TMOS POWER FETS 15 AMPERES rDS(on) = 0.16 OHM 200 VOLTS





MTM15N20 CASE 197A-02 TO-204AE



MTH15N20 CASE 340-02 TO-218AC

MAXIMUM RATINGS

Detion	Combal	MTH or MTM	Haria	
Rating	Symbol	15N20	Unit	
Drain-Source Voltage	V _{DSS}	280 V h 200 8.0 = 23	Vdc	
Drain-Gate Voltage (R _{GS} = 1 M Ω)	VDGR	200	Vdc	
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk	
Drain Current — Continuous — Pulsed	I _D	15 80	Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	150 1.2	Watts W/°C	
Operating and Storage Temperature Range	TJ, T _{stq}	-65 to 150	°C	

THERMAL CHARACTERISTICS

R_{θ} JC R_{θ} JA	0.83 30	°C/W
TL	275	°C
		$R_{\theta}JA$ 30

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				111111111111111111111111111111111111111
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA) MTH15N20, MTM15N20	V(BR)DSS	elb 1200 mag	ož eg ol osq i	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = Rated V_{DSS}, V_{GS} = 0$) ($T_J = 125^{\circ}C$)	IDSS	_	10 100	μAdc
Gate-Body Leakage Current, Forward $(V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0)$	IGSSF	_	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	_	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Ch	naracteristic			Symbol	l Min	Max	Unit
ON CHARACTERISTICS*				1	and2 et	off of	annia
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C		16	nsisto	V _{GS(th)}) 2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 7.5 Adc)		rDS(on)	ncement	0.16	Ohm		
Drain-Source On-Voltage (VGS = (ID = 15 Adc) (ID = 7.5 Adc, TJ = 100°C)	= 10 V)		dpid see	V _{DS} (on) 20	3 2.4	Vdc
Forward Transconductance (VDS	s = 15 V, ID	= 7.5 A)	regulators,	9FS	licati 4ns such s	gge g n dati	mhos
DYNAMIC CHARACTERISTICS					lay drivers.	er bris 1 or	erters, solen
Input Capacitance	18 0 16	8	Sewil	C _{iss}	- ageads barust	2000	pF
Output Capacitance	-	$V_{DS} = 25 \ f - 1$	V , $V_{GS} = 0$, MHz)	Coss	Vostoniady	700	specified at
Reverse Transfer Capacitance			141112/	C _{rss}	_ 90	200	st Elevated
SWITCHING CHARACTERISTICS*	(T _J = 100°C)		ahira Lawiini	niged Jee Wirk Jewi	Ulssipadon Un	A S FOWER	uc — pagg
Turn-On Delay Time				t _d (on)	_	60	ns
Rise Time	(V _{DE}		= 0.5 Rated I _D	tr	_	300	AR MUMO
Turn-Off Delay Time		Rgen = 5 See Figures	ou onms) s 13 and 14	t _d (off)		220	PA MICHID
Fall Time	linU			lodeny2 tf	_	250	
Total Gate Charge	sby ((V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V)		Qg	60 (Typ)	75	nC
Gate-Source Charge	1			Qgs	35 (Typ)		normos-un
Gate-Drain Charge		See Fig	gure 12	Qgd	25 (Typ)	0011110	DV SIEGENO
SOURCE DRAIN DIODE CHARACT	ERISTICS*		±20	8aV			auop lines
Forward On-Voltage	1991	(Is = R	ated In	V _{SD}	1.5 (Typ)	2.1	Vdc
Forward Turn-On Time	DDA.	VGS	200	ton	Limited by s	tray inducta	nce
Reverse Recovery Time	Watte			t _{rr}	450 (Typ)	_	ns
NTERNAL PACKAGE INDUCTANO	E (TO-204)		1.2			25.0	Serate above
Internal Drain Inductance (Measured from the contact so to the source pin and the cent			or 88 – er	an T LT Ld	5 (Typ) 3	Sior ag e Ten RAC TERIS	RMAL CHA
Internal Source Inductance (Measured from the source pi to the source bond pad)	WO	1	e e	ALAR Ls	12.5 (Typ)	nul — sone	ermai Besi.
INTERNAL PACKAGE INDUCTANO	E (TO-218)				for 5 seconds	seen more "	Purposes 18
Internal Drain Inductance (Measured from screw on tab (Measured from the drain lead			center of die)	Symbol	4 (Typ) 5 (Typ)	ARACTER Characteris	() JAnH
Internal Source Inductance (Measured from the source le	ad 0.25" from	package to	center of die)	L _S	10 (Typ)	IE TI <u>S</u> Residown V	CRAPACTE
*Pulse Test: Pulse Width ≤ 300 μs, Du	ty Cycle ≤ 2%.) izo, mtmienzo	Am ds.u = i	J 0 = 50A)

TYPICAL ELECTRICAL CHARACTERISTICS

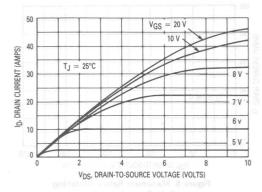


Figure 1. On-Region Characteristics

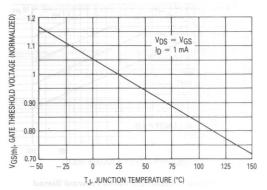


Figure 2. Gate-Threshold Voltage Variation With Temperature

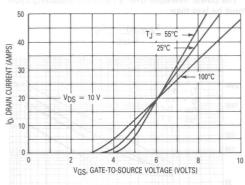


Figure 3. Transfer Characteristics

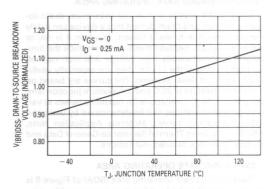


Figure 4. Breakdown Voltage Variation
With Temperature

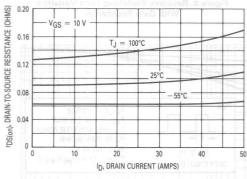


Figure 5. On-Resistance versus Drain Current

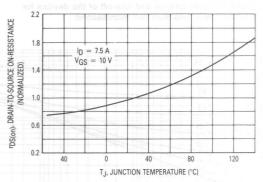


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

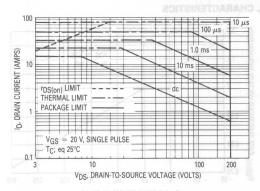


Figure 7. Maximum Rated Forward Biased Safe Operating Area

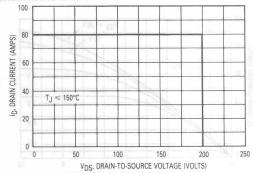


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

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SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

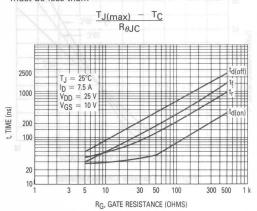


Figure 9. Resistive Switching Time Variation
With Gate Resistance

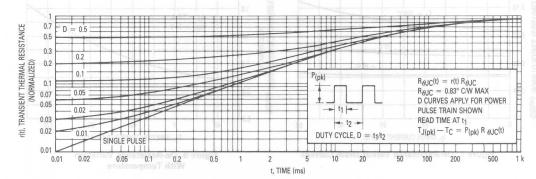
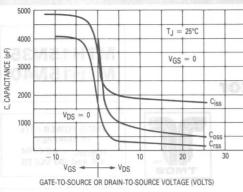


Figure 10. Thermal Response

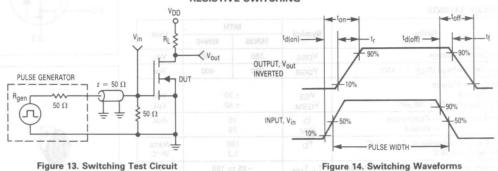


TJ = 25°C ID = 20 A ID = 2

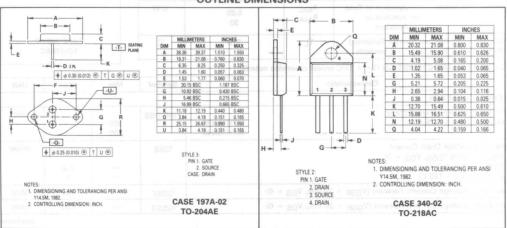
Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage





OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

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- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

P. d.	0	M	Unit	
Rating	Symbol	15N35	15N40	Unit
Drain-Source Voltage	V _{DSS}	350	400	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	350	400	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	IDM	75 15		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		50 .2	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance	Junction to Case Junction to Ambient	R _θ JC R _θ JA	0.83 30	°C/W
Maximum Lead Temp Purposes, 1/8" from		TLT [275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

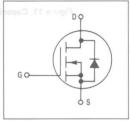
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS	328 2750 328 328 281 538	Ball II			
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)	MTH15N35 MTH15N40	V(BR)DSS	350 400	F	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0$) ($V_{DS} = 0.8\ Rated\ V_{DSS},\ V_{GS} = 0$, $V_{JJ} = 125^{\circ}C$)	. U 2. SATE 2 SAURCE IN COURCE SAURCE SELECTION SELECTIO	91	(% U	0.2	mAdo
Gate-Body Leakage Current, Forward (V _{GSF} = 20 Vdc, V _{DS} = 0)		IGSSF	(81 <u>4-8</u> 19.5)(0)	100	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$)	197A-92 2044E	IGSSR		100	nAdc
UMBELTO)					(contin

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are give to facilitate "worst case" design.

MTH15N35 MTH15N40



TMOS POWER FETS 15 AMPERES rDS(on) = 0.3 OHM 350 and 400 VOLTS





ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
N CHARACTERISTICS*				
Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_{D} = 1$ mA) $I_{J} = 100^{\circ}C$	V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 8 Adc)	rDS(on)		0.3	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 15 Adc) (I _D = 8 Adc, T _J = 100°C)	VDS(on)	TO SC SH CE VO	4.5 3.5	Vdc
Forward Transconductance (V _{DS} = 10 V, I _D = 8 A)	9FS	5	C) r amount?	mhos

Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss	_	3000	pF
Output Capacitance	f = 1 MHz)	Coss	_	500	
Reverse Transfer Capacitance	See Figure 11	C _{rss}	\ -	200	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time	Am Et 8 = gl	td(on)	\\o e	60	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r	/ //-	180	
Turn-Off Delay Time	Rgen = 50 ohms) See Figures 13 and 14	td(off)	\ \ <u>\</u>	450	
Fall Time	\$ 2	tf	1 / #	180	
Total Gate Charge	(VDS = 0.8 Rated VDSS,	Qg	110 (Typ)	160	nC
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 V)	Qgs	50 (Typ)	_	
Gate-Drain Charge	See Figure 12	Q _{gd}	60 (Typ)	_	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	(Is = Rated ID	V _{SD}	1.3 (Typ)	1.6	Vdc
Forward Turn-On Time	$V_{GS} = 0$)	ton	Limited by stray inductance		ce
Reverse Recovery Time		acteristics	1200 (Typ)	E <u>en</u> uge?	ns

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from screw on tab to center of die)	L _d	4 (Typ)	_	nH
(Measured from the drain lead 0.25" from package to center of die)		5 (Typ)		
Internal Source Inductance (Measured from the source lead 0.25" from package to center of die)	L _S	10 (Typ)	- V 07 - 30	

^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



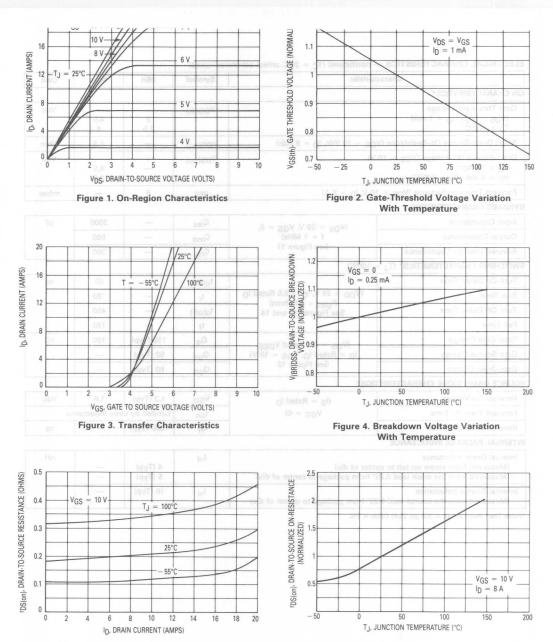


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

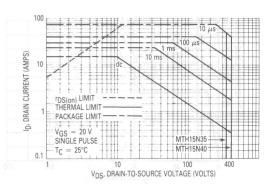


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

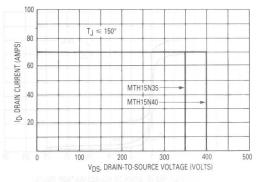


Figure 8. Maximum Rated Switching
Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

$$\frac{T_{J(max)} - T_{C}}{R_{\theta}JC}$$

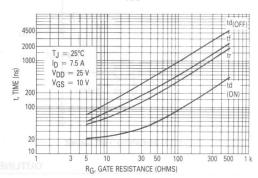


Figure 9. Resistive Switching Time Variation versus Gate Resistance

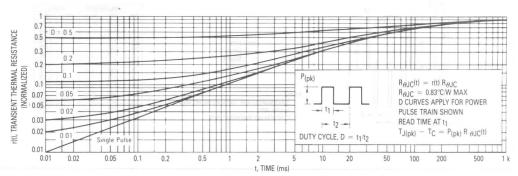
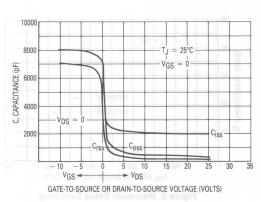


Figure 10. Thermal Response

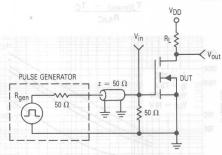


SET 10 VDS = 100 V VDS = 100 V

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING





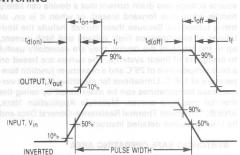
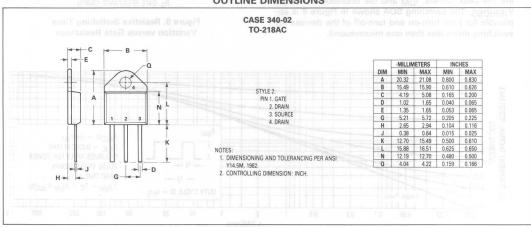


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

Dest.	C	MTH or MTM	2 11-24	
Rating	Symbol	20N15	Unit	
Drain-Source Voltage	VDSS	150	Vdc	
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	(V 01 = 2.150 gl beself =	Vdc	
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk	
Drain Current — Continuous — Pulsed	IDM IDM	(100 N = 20 N)	Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	150 1.2	Watts W/°C	
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C	

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	ed mor °C

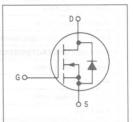
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS		ntar of dis)	sackage to ce	S" from p
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA) MTH20N15, MTM20N15	V(BR)DSS	150 conter of die)	package to d	Vdc mon 32.
Zero Gate Voltage Drain Current (Vps = Rated Vpss, Vgs = 0) (Vps = Rated Vpss, Vgs = 0, Tj = 125° C)	IDSS	_	10 100	μAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	IGSSF	_	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	_	100	nAdc

(continued)

MTH20N15 MTM20N15

TMOS POWER FETs 20 AMPERES rDS(on) = 0.12 OHM 150 VOLTS





MTM20N15 CASE 197A-02



MTH20N15 CASE 340-02 TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

	Characteristic			Symbo	ol Min	Max	Unit
ON CHARACTERISTICS*				1	Shee	r's Data	esigner
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C		10	neist	V _{GS(tl}	h) 2 1.5	4.5 4	Vdc
Static Drain-Source On-Resist	tance (V _{GS} = 10	Vdc, I _D = 1	10 Adc)	rDS(or	n) —	0.12	Ohm
Drain-Source On-Voltage (V _G (I _D = 20 Adc) (I _D = 10 Adc, T _J = 100°C)	S = 10 V)		d power	V _{DS} (o	_	3 2.4	Vdc
Forward Transconductance (\	/DS = 10 V, ID	= 10 A)	erensyn.	9FS	2	26 1002 3100	mhos
DYNAMIC CHARACTERISTICS	1 425 187					Library Control	
Input Capacitance	BOWT	V _{DS} = 25 V,	V00 = 0	Ciss	- service fire	2000	pF _{sec} 3
Output Capacitance	,	f = 1 N	MHz)	Coss	s(o n). Vastu	aV 22 700	Designar's Date
Reverse Transfer Capacitance	9	See Figu	ire 11	C _{rss}		200	at Elevated 7
SWITCHING CHARACTERISTICS	S* (T _J = 100°C)		absoul svitourists		terized for U	Dinda Charac	Source-to-Dustin
Turn-On Delay Time				t _d (on		60	ns
Rise Time	(V _{DD}	(V _{DD} = 25 V, I _D = 0.5 Rated I _D		t _r	_	300	DAR MUMDIA
Turn-Off Delay Time	S	R _{gen} = 50 see Figures 9	0 ohms) 13 and 14	t _d (off	. –	220	
Fall Time	mnG	Brack		tf	_	250	1
Total Gate Charge	Velc	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V)		Q _g	60 (Ty	p) 75	nC nc
Gate-Source Charge	oby ID			Qgs	35 (Ty	oe <u>Ass</u> = 1 (q	Nain-Gara Yelja
Gate-Drain Charge		See Figu	ure 12	Qgd	25 (Ty	p)1)6.1	V earloademe
SOURCE DRAIN DIODE CHARA	CTERISTICS*	0	1.0	OB Y		(au 02 4	Continuos
Forward On-Voltage	sinA	(Is = Ra	ted In	V _{SD}	1.5 (Ty	p) 2.1	Vdc
Forward Turn-On Time		V _{GS} =		ton	Limited	by stray inducta	ance
Reverse Recovery Time	isteW	0		og t _{rr}	450 (Ty		ns
NTERNAL PACKAGE INDUCTA	NCE (TO-204)					5/35	decis assed
Internal Drain Inductance (Measured from the contact to the source pin and the c			9.0	L _d	5 (Typ	ACTERISTICS	Hn Hn CHAR
Internal Source Inductance			06	ALSA LS	12.5 (T	(p) —	
(Measured from the source to the source bond pad)	pin, 0.25" from	the package	27	I	Soldering seconds		Vaximum Lead Purposes, 151
NTERNAL PACKAGE INDUCTA	NCE (TO-218)		Orania police	usakin evision i	Wid	MERCHANICA CA	HO MADESTON
Internal Drain Inductance (Measured from screw on t (Measured from the drain I			enter of die)	Ld Symbol	4 (Typ 5 (Typ		
Internal Source Inductance (Measured from the source	obV		150	Sagram Ls	10 (Ty		Orain-Source fire
Pulse Test: Pulse Width ≤ 300 μs,	Duty Cycle ≤ 2%.				TIMESONIE	MITHZONIE, N	5511

TYPICAL ELECTRICAL CHARACTERISTICS

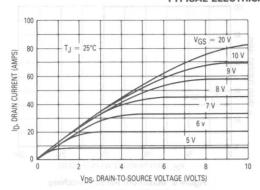


Figure 1. On-Region Characteristics

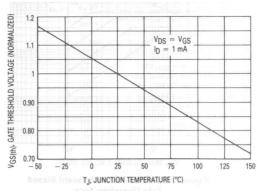


Figure 2. Gate-Threshold Voltage Variation With Temperature

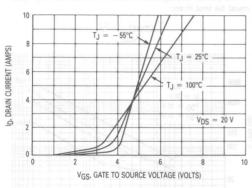


Figure 3. Transfer Characteristics

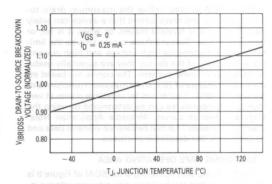


Figure 4. Breakdown Voltage Variation With Temperature

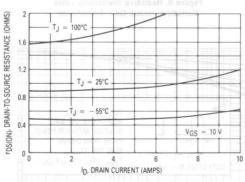


Figure 5. On-Resistance versus Drain Current

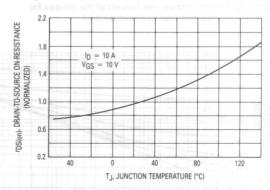


Figure 6. On-Resistance Variation With Temperature

100 μs 10 μ

V_{DS}, DRAIN-TO-SOURCE VOLAGE (VOLTS)

Figure 7. Maximum Rated Forward Biased
Safe Operating Area

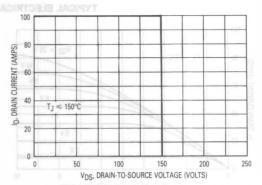


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

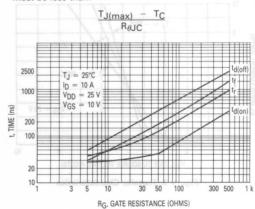


Figure 9. Resistive Switching Time Variation versus Gate Resistance

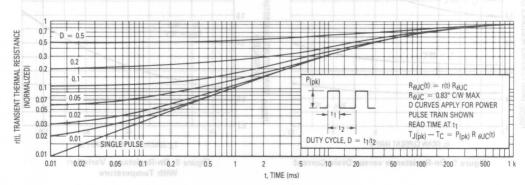


Figure 10. Thermal Response

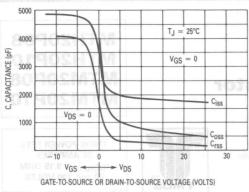


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

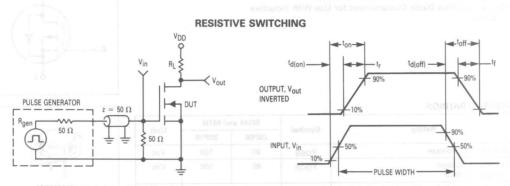
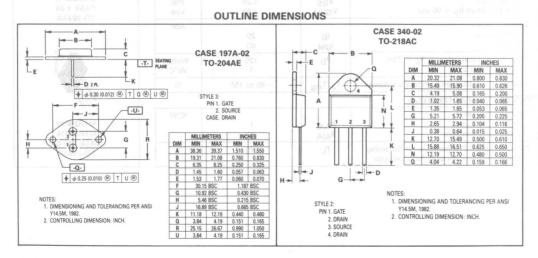


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms



Designer's Data Sheet

Power Field Effect Transistor P-Channel Enhancement-Mode Silicon Gate TMOS

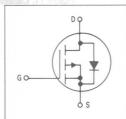
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS 20 AMPERES rDS(on) = 0.15 OHM 80 and 100 VOLTS



MAXIMUM RATINGS

Parking and a second	Combal	MTM a	MTM and MTH		
Rating	Symbol	20P08	20P10	Unit	
Drain-Source Voltage	VDSS	80	100	Vdc	
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	80	100	Vdc	
Gate-Source Voltage μ government μ and μ continuous Non-repetitive ($t_p \le 50~\mu$ s)	V _{GS} V _{GSM}	±20 ±40		Vdc Vpk	
Drain Current Continuous Pulsed Continuous C	I _D	20 80		Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	1	25 1	Watts W/°C	
Operating and Storage Temperature Range	T _J , T _{stg}	-65	to 150	°C	

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	R _O JC R _O JA	1 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C



MTM20P08 MTM20P10 CASE 1-04 TO-204AA



MTH20P08 MTH20P10 CASE 340-02 TO-218AC

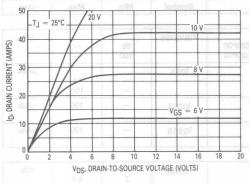
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS				13/7 1-12	
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	MTH20P08, MTM20P08 MTH20P10, MTM20P10	V(BR)DSS	80 100	1	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, T	J = 125°C)	IDSS	=	10 100	μAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	rd	IGSSF	_	100	nAdo
Gate-Body Leakage Current, Revers (VGSR = 20 Vdc, VDS = 0)	e	IGSSR		100	nAdc
ON CHARACTERISTICS*	18 70 5 - 50 - 50 0	81 41 5			
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = 1 \text{ mA})$ $T_J = 100^{\circ}\text{C}$		VGS(th)	2	4.5 4	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, I _D = 10 Adc)		rDS(on)	_	0.15	Ohm
Drain-Source On-Voltage ($V_{GS} = 1$) ($I_D = 20$ Adc) ($I_D = 10$ Adc, $T_J = 100$ °C)	0 V)	V _{DS(on)}	=	3.2	Vdc
Forward Transconductance (V _{DS} = 10 V, I _D = 10 A)	C 5 11 5 mA	9FS	5		mhos
OYNAMIC CHARACTERISTICS					
Input Capacitance		Ciss		2000	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss		950	
Reverse Transfer Capacitance	See Figure 10	C _{rss}		400	
WITCHING CHARACTERISTICS* (TJ	= 100°C)		1/3		
Turn-On Delay Time	100 50	td(on)	14	45	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r	F12	200	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 12 and 13	td(off)	augusta la companya di sa	150	
Fall Time		tf		150	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Qg	52 (Typ)	75	nC
Gate-Source Charge	I_D = Rated I_D , V_{GS} = 10 V)	Qgs	22 (Typ)	_	
Gate-Drain Charge	See Figure 11	Q _{gd}	30 (Typ)	_	
OURCE DRAIN DIODE CHARACTERI	STICS*				
Forward On-Voltage	V 01 = 20V 45	V _{SD}	2.8 (Typ)	4	Vdc
Forward Turn-On Time	(I _S = Rated I _D V _{GS} = 0)	ton	100 (Typ)	<u></u>	ns
Reverse Recovery Time	102 - 01	t _{rr}	350 (Typ)	_	ns

*Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

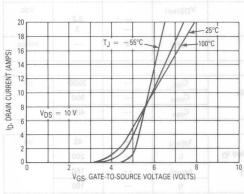
TYPICAL ELECTRICAL CHARACTERISTICS



1.1 VDS = VGS UD = 1 mA VDS = VGS UD = 1 mA VDS = 1 mA

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



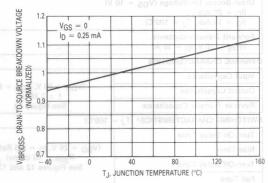
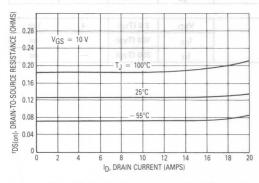


Figure 3. Transfer Characteristics





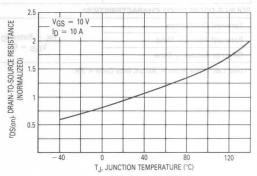


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

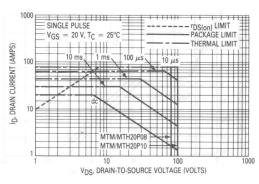


Figure 7. Maximum Rated Forward Biased Safe Operating Area

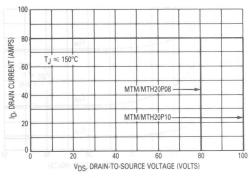


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

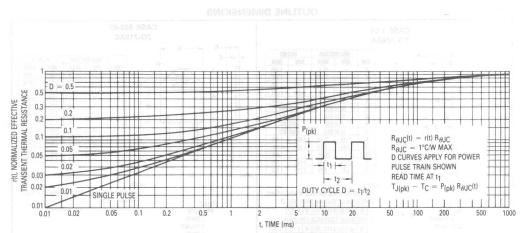


Figure 9. Thermal Response

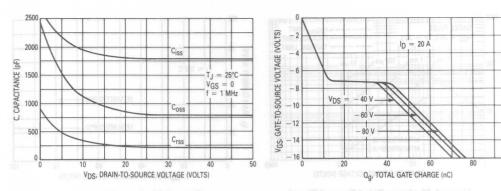


Figure 10. Capacitance Variation

Figure 11. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

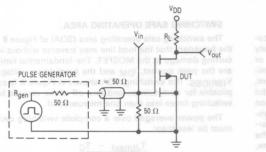


Figure 12. Switching Test Circuit

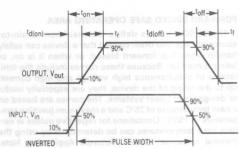
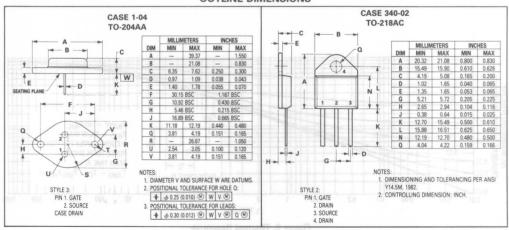


Figure 13. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

Rating	Symbol	MTH25N08	MTH25N10 MTM25N10	Unit
Drain-Source Voltage	VDSS	80	100	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	W 80 28	100	Vdc
Gate-Source Voltage Continuous Non-repetitive $(t_p \le 50 \ \mu s)$	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	ID	25 105		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stq} -65 to 150		to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	or o

ELECTRICAL CHARACTERISTICS — (T_C = 25°C unless otherwise noted)

Characteristic Carlo	Symbol	Min	Max	Unit
FF CHARACTERISTICS		leab for sent	adiage to cer	g most 3
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	V(BR)DSS	(all) to raths	pacinge to t	Vdc
MTH25N08		80	_	
MTH25N10,MTH25N10		100	_	
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0)	IDSS			μAdc
(V _{DS} = Rated V _{DSS} ,		_	10	
$V_{GS} = 0, T_{J} = 125^{\circ}C)$		_	100	
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	IGSSF	_	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	_	100	nAdc

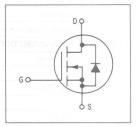
(continued)

TMOS

MTH25N08 MTH25N10 MTM25N10

TMOS POWER FETS
AMPERES

rDS(on) = 0.075 OHM
80 and 100 VOLTS





MTM25N10 CASE 197A-02 TO-204AE



MTH25N08 MTH25N10 CASE 340-02 TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS Cha	aracteristic			Symbol	Min	Max	Unit
ON CHARACTERISTICS*					1.00		
Gate Threshold Voltage		V V		V _{GS(th)}	auc 21	20 C. L	Vdc
$(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$				to the state of	2	4.5	0.03870
T _J = 100°C			A SPECIAL E	200 20	1.5	4	20 119 4
Static Drain-Source On-Resistanc		0 Vdc, ID = 1	2.5 Adc)	rDS(on)	nomnan	0.075	Ohm
Drain-Source On-Voltage (VGS = (ID = 25 Adc) (ID = 12.5 Adc, TJ = 100°C)				V _{DS} (on)	501	2.25 1.8	Vdc
Forward Transconductance (V _{DS}	= 10 V, I _D	= 12.5 A)	atetrevor	9FS	5	T91 Temp1	mhos
DYNAMIC CHARACTERISTICS	100		10000010000	1 1030-5-01	DI BUSINESSE	lav drivers.	on and bloc
Input Capacitance	4 100	05.1/.1	Times	Ciss	tohin a Speed	2000	pF
Output Capacitance	COM	$V_{DS} = 25 \text{ V, V}$ f = 1 MI	/GS = 0, Hz)	Coss	_	1500	Specified o
Reverse Transfer Capacitance		See Figure		C _{rss}	EV (na)eux	400	asignar's D
SWITCHING CHARACTERISTICS* (T ₁ = 100°C)			betimi	Dissipation L	DA la Power	at EHEVERBOO agged — SC
Turn-On Delay Time			detive coads	t _d (on)	eracienzed or	60	ns
Rise Time	(VDD	= 25 V, I _D =	0.5 Rated In	t _r	_	450	
Turn-Off Delay Time		R _{gen} = 50 ohms) See Figures 9, 13 and 14 (V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V)				150	TAS MUND
Fall Time	tletti. S					300	
Total Gate Charge	ShV				29 (Typ)	40	nC
Gate-Source Charge					23 (Typ)	= a - 1 spr	il C
Gate-Drain Charge	U	See Figur		Ωgs	6 (Typ)	- 59-11-981	PICT SCORPTION
SOURCE DRAIN DIODE CHARACTE	DICTICC*	- 05	.2	Q _{gd}	6 (199)	- 5198.0	a v solund-et
Forward On-Voltage	nio i ico	- 01	X-10	Van	1.5 (Tun)	1.8	Vdc
	Aide	(Is = Rat		V _{SD}	1.5 (Typ)	ALMOLINIST D. J.	- Ingeni Lau
Forward Turn-On Time	attistV	V _{GS} =		MGI ton	Limited by s	tray inductar	
Reverse Recovery Time	3 307	0	GI .	og t _{rr}	450 (Typ)	(B) A V TSUE	ns
INTERNAL PACKAGE INDUCTANCE	(10-204)	per o	1 88 -	also a la	ollows as the ol	maT appear	has policie
Internal Drain Inductance (Measured from the contact sort to the source pin and the center				Ld	5 (Typ)	ACTERIST	nH AHO JAME
Internal Source Inductance	74.3	0	6	ALAR LS	12.5 (Typ)	onul -	ermal Resurt
(Measured from the source pin to the source bond pad)		the package	27	TL	e for Soldering	Ter ceratur	es l'eumbe
NTERNAL PACKAGE INDUCTANCE	(TO-218)						
Internal Drain Inductance (Measured from screw on tab t (Measured from the drain lead			nter of die)	Iddaya Ld	4 (Typ) 5 (Typ)	tahas— ada	nH
Internal Source Inductance (Measured from the source lea	d 0.25" from	package to c	enter of die)	aan(A8) Ls	10 (Typ)	V mwo bisan Vi	EIN-Source E
MTHZENOS		-	08			WTH25N	

TYPICAL ELECTRICAL CHARACTERISTICS

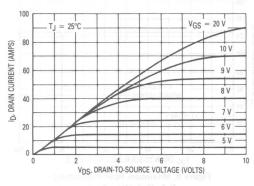


Figure 1. On-Region Characteristics

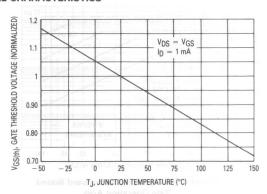


Figure 2. Gate-Threshold Voltage Variation With Temperature

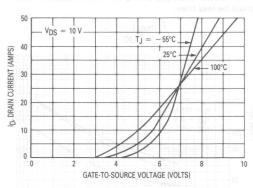


Figure 3. Transfer Characteristics

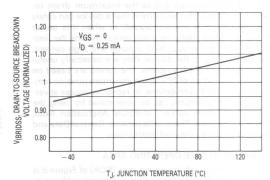


Figure 4. Breakdown Voltage Variation
With Temperature

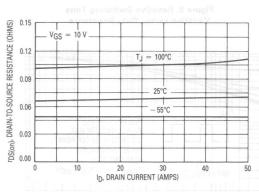


Figure 5. On-Resistance versus Drain Current

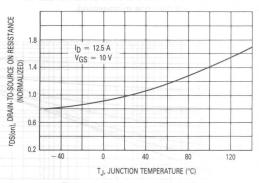


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

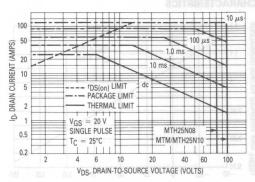


Figure 7. Maximum Rated Forward Biased Safe Operating Area

140 (AMPS) 120 DRAIN CURRENT 100 80 MTH25N08 60 MTM/MTH25N10 ò 40 T_J ≤ 150°C 20 40 60 80 100 20 VDS, DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

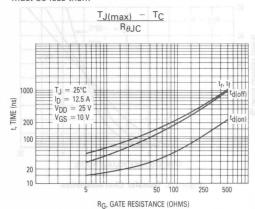


Figure 9. Resistive Switching Time Variation versus Gate Resistance

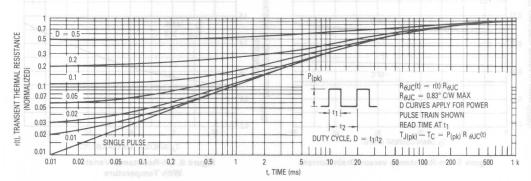
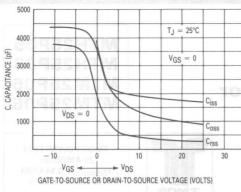


Figure 10. Thermal Response

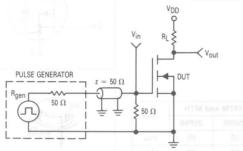


16 T_J = 25°C ON 30 V V_{DS} = 20 V V_{DS} =

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING



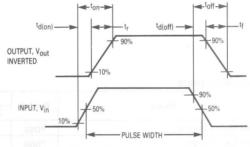
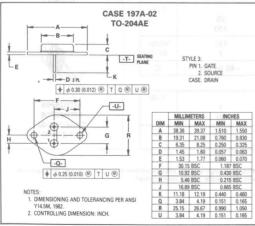
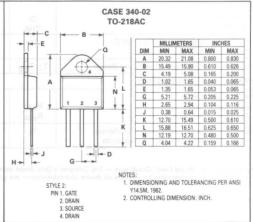


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS





MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

P-Channel Enhancement-Mode Silicon Gate TMOS

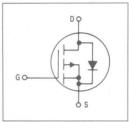
These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive
 Loads





TMOS POWER FETS 25 AMPERES rDS(on) = 0.14 OHM 50 and 60 VOLTS



MAXIMUM RATINGS

7		MTM a	.0.0		
Rating	Symbol	25P05 25P06		Unit	
Drain-Source Voltage	VDSS	50	60	Vdc	
Drain-Gate Voltage (RGS = 1 MΩ) provided guidative AT enugPl	V _{DGR}	50	60	Vdc	
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	±20 ±40		Vdc Vpk	
Drain Current Continuous Pulsed	IDM	25 100		Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	125 1		Watts W/°C	
Operating and Storage Temperature Range	TJ, Tstg	-65 to 150		°C	

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	R _θ JC	1	°C/W
Junction to Ambient	$R_{\theta}JA$	30	BULSE 1944 Non
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C



MTM25P05 MTM25P06 CASE 1-04 TO-204AA



MTH25P05 MTH25P06 CASE 340-02 TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MTH/MTM25P05,06

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

	teristic Mai DANAM JAMA DA	Symbol	Min	Max	Unit
OFF CHARACTERISTICS			T T		
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	MTH25P05, MTM25P05 MTH25P06, MTM25P06	V(BR)DSS	50 60		Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ	= 125°C)	IDSS		10 100	μAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		IGSSF	-	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	-	100	nAdc	
ON CHARACTERISTICS*	80 =				8.0
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$ $T_{J} = 100^{\circ}\text{C}$	0 0 0 00 00	V _{GS(th)}	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 12.5 Adc)	rDS(on)	Region Chan	0.14	Ohm	
Drain-Source On-Voltage ($V_{GS} = 10$ ($I_{D} = 25$ Adc) ($I_{D} = 12.5$ Adc, $T_{J} = 100^{\circ}$ C)	V _{DS(on)}	_	3.5 2.6	Vdc	
Forward Transconductance (V _{DS} = 10 V, I _D = 12.5 A)	g _{FS}	5		mhos	
DYNAMIC CHARACTERISTICS	CRIP 20V	1771		-	
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss		2000	pF
Output Capacitance	f = 1 MHz)	Coss		950	
Reverse Transfer Capacitance	See Figure 10	C _{rss}	-	400	
SWITCHING CHARACTERISTICS* (TJ	= 100°C)				
Turn-On Delay Time	5 9	^t d(on)		50	ns
Rise Time	$(V_{DD} = 25 \text{ V, I}_{D} = 0.5 \text{ Rated I}_{D} $ $R_{gen} = 50 \text{ ohms})$	tr	77	300	
Turn-Off Delay Time	See Figures 12 and 13	td(off)	-43	150	
Fall Time	TB E CT	tf	_	180	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Qg	50 (Typ)	60	nC
Gate-Source Charge	I_D = Rated I_D , V_{GS} = 10 V)	Qgs	25 (Typ)	r entre	
Gate-Drain Charge	See Figure 11	Q _{gd}	33 (Typ)	-	
SOURCE DRAIN DIODE CHARACTERIS	TICS*				
Forward On-Voltage	No. 1 Page 1 In	V _{SD}	3.8 (Typ)	5	Vdc
Forward Turn-On Time	(I _S = Rated I _D V _{GS} = 0)	ton	100 (Typ)	_	ns
Reverse Recovery Time		t _{rr}	275 (Typ)	_	ns
INTERNAL PACKAGE INDUCTANCE (T	0-204)				
Internal Drain Inductance (Measured from the contact screw to the source pin and the center of		L _d	5 (Typ)		nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L _S	12.5 (Typ)	_	
NTERNAL PACKAGE INDUCTANCE (T	0-218)				
Internal Drain Inductance (Measured from screw on tab to c (Measured from the drain lead 0.2		Ld	4 (Typ) 5 (Typ)	=	nH
Internal Source Inductance	L _s	10 (Typ)			

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

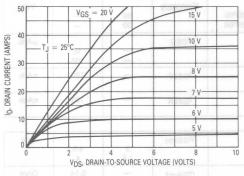


Figure 1. On-Region Characteristics

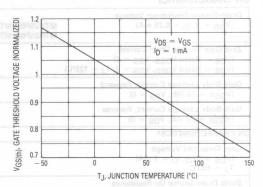


Figure 2. Gate-Threshold Voltage Variation With Temperature

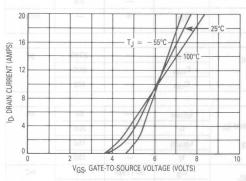


Figure 3. Transfer Characteristics

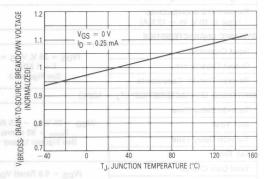


Figure 4. Breakdown Voltage Variation
With Temperature

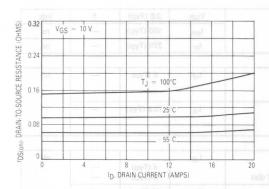


Figure 5. On-Resistance versus Drain Current

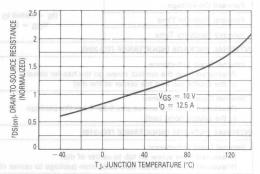


Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

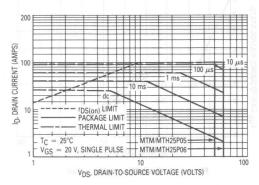


Figure 7. Maximum Rated Forward Biased Safe Operating Area

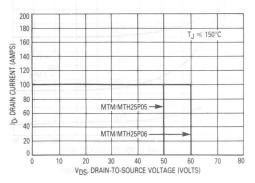


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

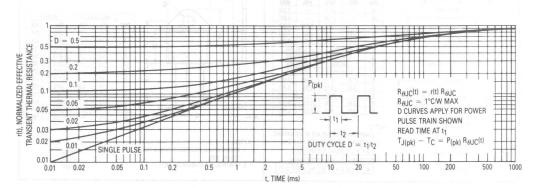


Figure 9. Thermal Response

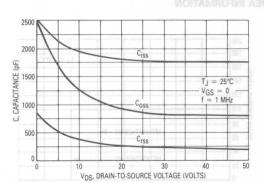


Figure 10. Capacitance Variation

Figure 11. Gate Charge Variation

RESISTIVE SWITCHING

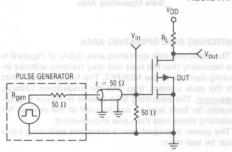


Figure 12. Switching Test Circuit

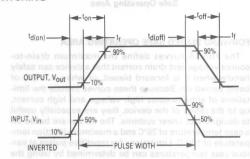
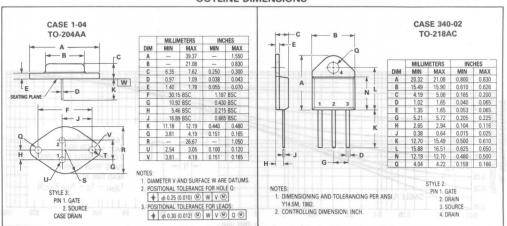


Figure 13. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA ■ SEMICONDUCTOR I **TECHNICAL DATA**

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

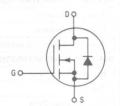
This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

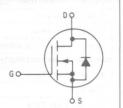
- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FET **30 AMPERES** rDS(on) = 0.08 OHM 200 VOLTS

TMOS





MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	VDSS	200	Vdc
Drain-Gate Voltage (R _{GS} = 1 MΩ)	VDGR	IV 01 = 200 gl betaR	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	ID ID	30 90	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	150 1.2	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta}JC$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)	ITH30N20 V(BR)DSS	200	_	Vdc
Zero Gate Voltage Drain Current (Vps = Rated Vps, Vgs = 0) (Vps = Rated Vps, Vgs = 0, Tj = 125°C)	IDSS	_	10 100	μAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	IGSSF	_	100	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$)	IGSSR	_	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MOTOROLA
SEMICONDUCTOR CONTROL OF THE CONTROL OF TH

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

USI	Uth	Cha	aracteristic		Symbol	Min	Max	Unit	9
N CHARA	ACTERISTICS	*				10-10-00m			
Gate Threshold Voltage (Vps = Vgs, Ip = 1 mA) TJ = 100°C				VGS(th)	2 1.5	4.5 4	Vdc	0. 0-	
Static Dr	ain-Source O	n-Resistanc	e (V _{GS} = 10	Vdc, I _D = 15 Adc)	rDS(on)	-80	0.08	Ohm	Hi
Drain-Source On-Voltage (VGS = 10 V) (I _D = 30 Adc) (I _D = 15 Adc, T _J = 100°C)				V _{DS(on)}	esign <u>e</u> d for n	2.85 1.92	Vdc	eini ber	
Forward	Transconduc	ctance (V _{DS}	= 10 V, I _D =	15 A)	9FS	10	sles bas bi	mhos	1936
YNAMIC	CHARACTER	ISTICS		attent) (Switching -	shapde Auu	DENG SEED OF THE	tol sist no	
Input Ca	pacitance		()/	DS = 25 V, V _{GS} = 0,	Ciss	apy .moiso	5500	gne7q Date	iraG
Output C	Capacitance			f = 1 MHz	Coss		1500	Elevated Te	28
Reverse	Transfer Cap	acitance		See Figure 11		not becaute	500	ged - SUK	Suls Suls
WITCHIN	G CHARACTE	ERISTICS* (T _J = 100°C)						
Turn-On	Delay Time	-00			td(on)	_	50	ns	7
Rise Tim	ie		(V _{DD}	(V _{DD} = 25 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms) See Figures 9, 13 and 14		_	300		
Turn-Off	Delay Time		Se			_	150	INTAR NIUM	DCAL
Fall Time	е		tinit	sulaV	odray@tf	_	150		
Total Ga	te Charge		aby w	(V _{DS} = 0.8 Rated V _{DSS} ,		85 (Typ)	95	nC	lanG.
Gate-Sou	urce Charge					45 (Typ)	= a nd i sp	n Gate Volta	ianG.
Gate-Dra	in Charge			See Figure 12	Q _{qd}	40 (Typ)	- 200	s-Source Volt	Gate
OURCE D	RAIN DIODE	CHARACTE	RISTICS*	20 ±	39V		12 (0.7) · 4V	Supplified	0
Forward	On-Voltage		Ade	60	V _{SD}	1.2 (Typ)	2	Vdc]_
Forward	Turn-On Tim	ne	-0.00	$(I_S = Rated I_D, V_{GS} = 0)$	ton	Limited by stray inductance		nce	36
Reverse	Recovery Tin	ne	emsW	VGS = 0)	an t _{rr}	200 (Typ)	T © au itori	ns	OT
NTERNAL	PACKAGE IN	DUCTANCE	O'NW	\$37			0.9	erste above 2	0
(Measi		e contact sci		center of die)	Ld	4 (Typ) 5 (Typ)	ACTERIST	HAMAL CHAR	Ogo REM
	Source Inducured from the		0.25" from pa	ackage to source bond pad)	ALSA LS	10 (Typ)	breat =	mai Nesim.	901
Pulse Test:	Pulse Width ≤	300 μs, Duty	Cycle ≤ 2%.		1.37	to seconds	from case h	unicase, 1/8"	A NO
			aag!						

TYPICAL ELECTRICAL CHARACTERISTICS

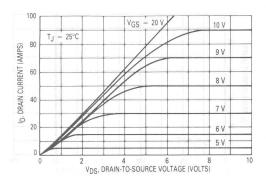


Figure 1. On-Region Characteristics

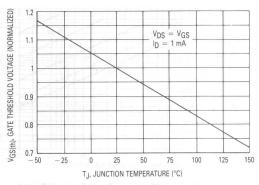


Figure 2. Gate-Threshold Voltage Variation With Temperature

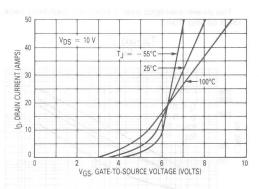


Figure 3. Transfer Characteristics

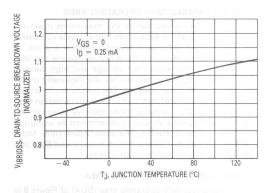


Figure 4. Breakdown Voltage Variation
With Temperature

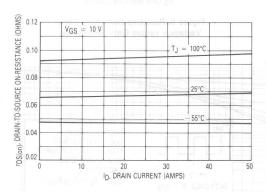


Figure 5. On-Resistance versus Drain Current

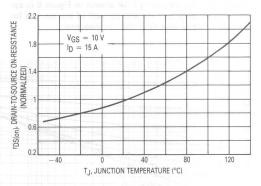


Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

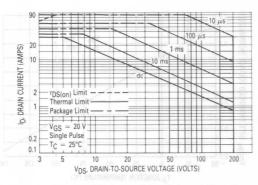


Figure 7. Maximum Rated Forward Biased Safe Operating Area

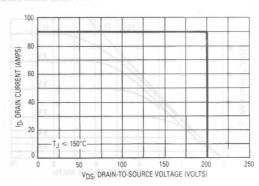


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-tosource voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

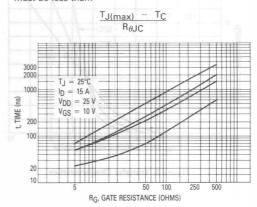


Figure 9. Resistive Switching Time Variation versus Gate Resistance

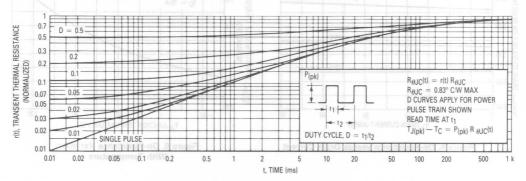
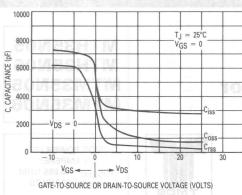


Figure 10. Thermal Response



16, T_J = 25°C
10 = 30 A
100 V
100 V

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

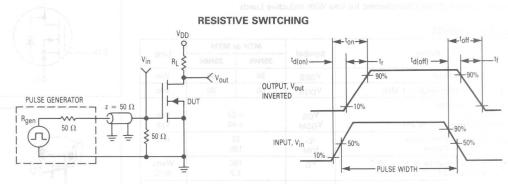
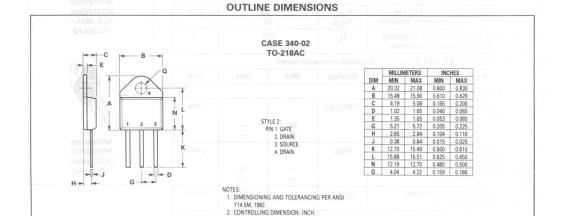


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

Parties Hallengt Hill	0	MTH o	MTH or MTM		
Rating	Symbol	35N05	35N06	Unit	
Drain-Source Voltage	V _{DSS}	50	60	Vdc	
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	50	60	Vdc	
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	±20 ±40		Vdc Vpk	
Drain Current — Continuous — Pulsed	IDM	35 120		Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	150 1.2		Watts W/°C	
Operating and Storage Temperature Range	TJ, T _{sta}	-65 to 150		°C	

THERMAL CHARACTERISTICS

HEIMAE ONAMOTEMOTIO			
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

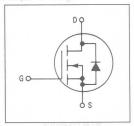
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				1
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA) MTH35N05, MTM35N05 MTH35N06, MTM35N06	V(BR)DSS	50 60	=	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, $T_J = 125^{\circ}C$)	IDSS	32M808 2	10 100	μAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	IGSSF	BAS AND T <u>OL</u> ERANGO	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	SUM POLICE DE	100	nAdc

(continued)

MTH35N05 MTH35N06 MTM35N05 MTM35N06



TMOS POWER FETS 35 AMPERES rDS(on) = 0.055 OHM 50 and 60 VOLTS





MTM35N05 MTM35N06 CASE 197A-02 TO-204AE



MTH35N05 MTH35N06 CASE 340-02 TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

FI FCTRICAL	CHARACTERISTICS	— continued (Tc.)	= 25°C unless	s otherwise noted)

Ch	aracteristic	Symbol	Min	Max	Unit		
ON CHARACTERISTICS*				a N.			
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = 1 \text{ mA})$ $T_J = 100^{\circ}\text{C}$		VGS(th)	2 1.5	4.5 4	Vdc		
Static Drain-Source On-Resistance	ce (V _{GS} = 10 Vdc, I _D = 17.5 Adc)	rDS(on)		0.055	Ohm		
Drain-Source On-Voltage (VGS = (ID = 35 Adc) (ID = 17.5 Adc, TJ = 100°C)		V _{DS(on)}		2.3 1.9	Vdc		
Forward Transconductance (VDS	; = 10 V, I _D = 17.5 A)	gFS	8	-	mhos		
YNAMIC CHARACTERISTICS	os n 🕏						
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss	ur enu ana una d	2000	pF		
Output Capacitance	f = 1 MHz	Coss	_	1500			
Reverse Transfer Capacitance	See Figure 11	Crss	legio <u>n</u> Chara	400			
SWITCHING CHARACTERISTICS* (T _J = 100°C)						
Turn-On Delay Time		td(on)	_	60	ns		
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r		450			
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	\ I	150			
Fall Time	0 - 50V	tf	-	300			
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Ωg	29 (Typ)		nC		
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 V)	Qgs	23 (Typ)				
Gate-Drain Charge	See Figure 12	Q _{gd}	6 (Typ)				
SOURCE DRAIN DIODE CHARACTI	ERISTICS*		70				
Forward On-Voltage	(IS = Rated ID	V _{SD}	1.5 (Typ)	1.8	Vdc		
Forward Turn-On Time	V _{GS} = 0)	ton	Limited by st	y stray inductance			
Reverse Recovery Time	00.0	t _{rr}	450 (Typ)	KS	ns		
NTERNAL PACKAGE INDUCTANC	E (TO-204)	07	8 1	1			
Internal Drain Inductance (Measured from the contact so to the source pin and the cent		L _d (N)	5 (Typ)	01-31 <u>2-1</u> 30 01-31 <u>-1</u> 30 01-31-130	nH		
Internal Source Inductance (Measured from the source pin to the source bond pad)	n, 0.25" from the package	L _S	12.5 (Typ)	_			
NTERNAL PACKAGE INDUCTANC	E (TO-218)			100			
Internal Drain Inductance (Measured from screw on tab (Measured from the drain lead	L _d	4 (Typ) 5 (Typ)		nH			
Internal Source Inductance (Measured from the source lea	L _S	10 (Typ)	T				
Pulse Test: Pulse Width ≤ 300 μs, Dut	y Cycle ≤ 2%.						

TYPICAL ELECTRICAL CHARACTERISTICS

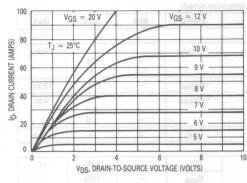


Figure 1. On-Region Characteristics

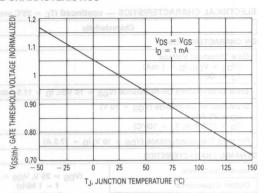


Figure 2. Gate-Threshold Voltage Variation
With Temperature

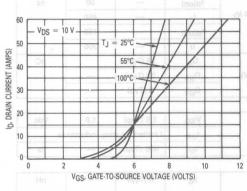


Figure 3. Transfer Characteristics

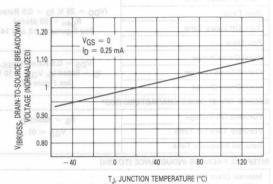


Figure 4. Breakdown Voltage Variation
With Temperature

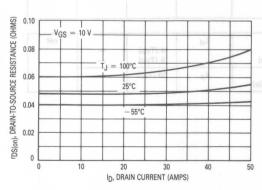


Figure 5. On-Resistance versus Drain Current

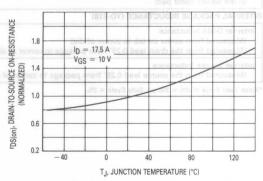


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

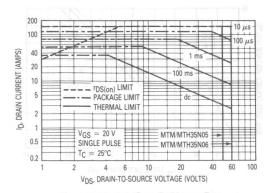


Figure 7. Maximum Rated Forward Biased Safe Operating Area

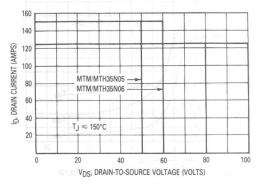


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V(\mbox{\footnotesize BR})\mbox{\footnotesize DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{\mathsf{T}\mathsf{J}(\mathsf{max}) - \mathsf{T}\mathsf{C}}{\mathsf{R}_{\theta}\mathsf{J}\mathsf{C}}$$

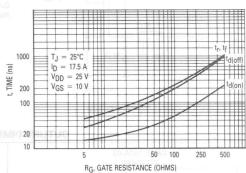


Figure 9. Resistive Switching Time Variation versus Gate Resistance

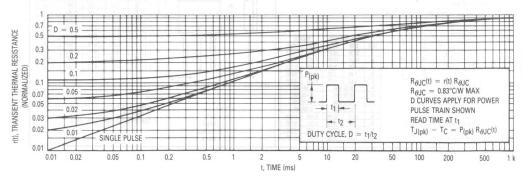


Figure 10. Thermal Response

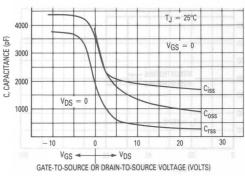


Figure 11. Capacitance Variation

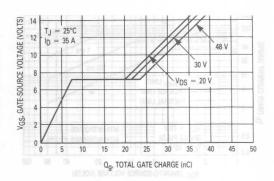


Figure 12. Gate Charge versus

Gate-to-Source Voltage

RESISTIVE SWITCHING

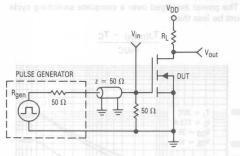


Figure 13. Switching Test Circuit

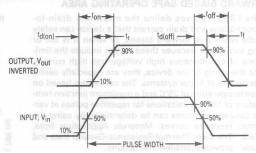
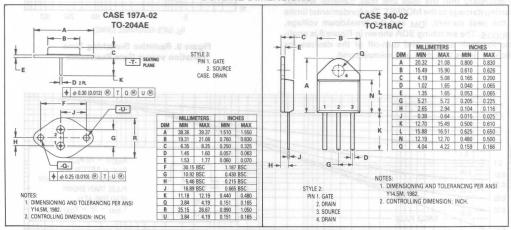


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Designer's Data Sheet

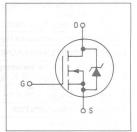
TMOS IV Power Field Effect Transistors N-Channel Enhancement-Mode Silicon Gate

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

MTH35N06E MTM35N06E

TMOS POWER FETS
35 AMPERES
rDS(on) = 0.055 OHM
60 VOLTS





MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	VDSS	60 882	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous (T _C = 25°C) — Pulsed	I _D	35 120	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	150 1.2	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	R_{θ} JC R_{θ} JA	0.83	°C/W sed out no (sile out)
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C



MTM35N06E CASE 197A-02 TO-204AE



MTH35N06E CASE 340-02 TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Cha		Symbol	Min	Max	Unit		
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)					60	_	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, 7	T _J = 125°C)			IDSS	eta_5h _	10 100	μΑ
Gate-Body Leakage Current, Forwa		20 Vdc, V _{DS} = 0)		IGSSF		100	nAdc
Gate-Body Leakage Current, Rever	se (V _{GSR} =	20 Vdc, V _{DS} = 0)	2015	IGSSR	772 1	100	nAdc
ON CHARACTERISTICS*		staD no:	AHP a	hold-to	amanna	al Enha	hamadi
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) T.I = 100°C	ETs is designed to withstand high				2 1.5	4.5	Vdc sansvas s
Static Drain-Source On-Resistance	(VGS = 10 \	/dc, ID = 17.5 Adc	on semil	rDS(on)	dtive s shoil	0.055	Ohm
Drain-Source On-Voltage ($V_{GS} = \frac{1}{2}$) ($I_D = 35 \text{ Adc}$) ($I_D = 17.5 \text{ Adc}$, $T_J = 100^{\circ}\text{C}$)		ters and PWM mo cuits where diods onal safety marg	s, convert ridge circ fler additi	V _{DS(on)}	cations in p ticularly we g area are o	1008 pmins 80 2.3 850 116 1.9 81	spisoby swith the second secon
Forward Transconductance (VDS =	= 15 V, I _D =	17.5 A)		g _{FS}	14 210	age <u>transie</u>	mhos
DRAIN-TO-SOURCE AVALANCHE CH	ARACTERIST	rics	90	ned to Repla	Diode Dasig	re-to-Drain	emal Soun
Unclamped Inductive Switching Er (I _D = 120 A, V _{DD} = 25 V, T _C = (I _D = 35 A, V _{DD} = 25 V, T _C = 2 (I _D = 14 A, V _{DD} = 25 V, T _C = 1	25°C, Single 25°C, P.W. ≤	Pulse, Non-repetiti 200 μs, Duty Cycle	≤ 1%)	WDSR	ne Mode — IS) E <u>nergy</u>	200 500 180	nergy in t nductive S if 100°C.
DYNAMIC CHARACTERISTICS			101 661	Dade (AOS)	ating Area t	Sare Uper	ninukaring
Input Capacitance	BONA	_{DS} = 25 V, V _{GS} =	0 8 01 9	C _{iss}	niT v rs voce	3000	rG-opF _{151U}
Output Capacitance	- ()	f = 1 MHz	0,	Coss	Diode	1500	Discrete Fa
Reverse Transfer Capacitance	See Figure 16			C _{rss}	18 NI 98U 1	500	de is Chai
SWITCHING CHARACTERISTICS* (T	1 = 100°C)	7.					
Turn-On Delay Time			Dis.	td(on)	esplant Trac	60	ns
Rise Time	(V _{DD}	$= 25 \text{ V, I}_D = 0.5 \text{ R}$ R _{gen} = 50 ohms)	ated ID	t _r	_	450	7,111,141,000,00
Turn-Off Delay Time	SHV	See Figure 9		td(off)	_	150	V 600002-0
Fall Time	869	//00		tf	7000	300	Poly Mail
Total Gate Charge	(V	DS = 0.8 Rated VD	000	Q_g	60 (Typ)	90	nC
Gate-Source Charge	ID =	Rated ID, VGS =	10 V)	Qgs	33 (Typ)	— Nor	7 Y 9311000-1
Gate-Drain Charge	20A	See Figures 17 and	18	Qgd	35 (Typ)	- Confinuous	n-Current -
OURCE DRAIN DIODE CHARACTER	ISTICS*	(20	MO			bantu ⁻¹ -	
Forward On-Voltage	SHEAA	(I _S = 35 A		V _{SD}	1.7 (Typ)	2.5	Vdc
Forward Turn-On Time	J. WY	$V_{GS} = 0$		ton	Limited	by stray ind	uctance
Reverse Recovery Time	- J	$dI_S/dt = 100 A/\mu s$	gfz - iJ-	t _{rr}	200 (Typ)	HINT BESTON	ns
NTERNAL PACKAGE INDUCTANCE	(TO-204)				108	ACTERIST	MAL CHAI
Internal Drain Inductance (Measured from the contact scre to the source pin and the center		ader closer		Ld	5 (Typ)	ase mbient	maHnesisti inction to C inction to A
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)				L _S	12.5 (Typ)	Temperatur from case	Imum Lead Imposes, 1/8
NTERNAL PACKAGE INDUCTANCE	TO-218)	m to replace and animal	ata Sheet pe	Tra Designer's D	Conditions	"Worst Case"	er's Jata for
Internal Drain Inductance (Measured frrom the contact scr (Measured from the drain lead 0			die)	L _d	4 (Typ) 5 (Typ)	_	nH
Internal Source Inductance (Measured from the source lead	0.25" from n	ackage to source b	ond nad)	L _S	10 (Typ)	_	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

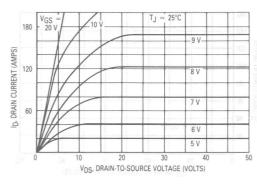


Figure 1. On-Region Characteristics

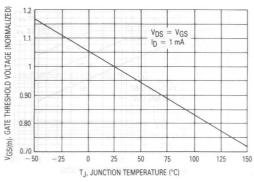


Figure 2. Gate-Threshold Voltage Variation
With Temperature

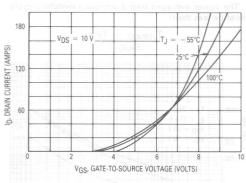


Figure 3. Transfer Characteristics

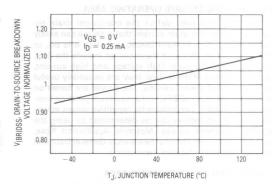


Figure 4. Breakdown Voltage Variation With Temperature

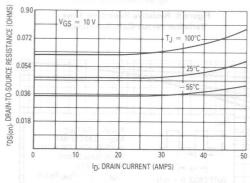


Figure 5. On-Resistance versus Drain Current

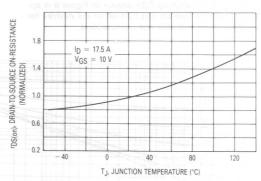


Figure 6. On-Resistance Variation
With Temperature

3

SAFE OPERATING AREA INFORMATION

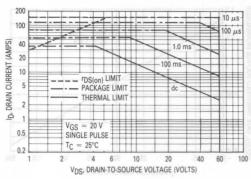


Figure 7. Maximum Rated Forward Biased Safe Operating Area

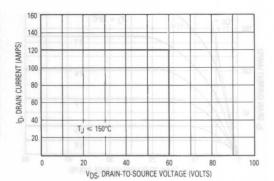


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

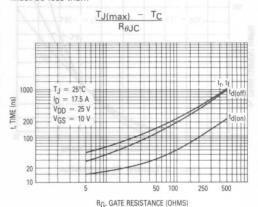


Figure 9. Resistive Switching Time Variation versus Gate Resistance

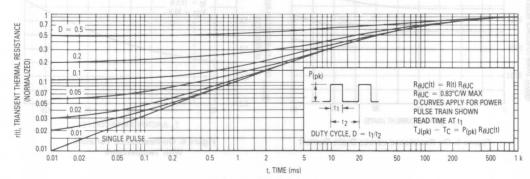


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so $dl_{\rm S}/dt$ is specified with a maximum value. Higher values of $dl_{\rm S}/dt$ require an appropriate derating of $l_{\rm FM}$, peak $V_{\rm DS}$ or both. Ultimately $dl_{\rm S}/dt$ is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during $t_{\rm TT}$ as the diode goes from conduction to reverse blocking.

 $V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; IFM is the maximum forward source-drain diode current just prior to the onset of commutation.

 V_R is specified at 80% of $V_{\left(BR\right)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

RGS should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_{S}/dt of 400 A/ μ s.

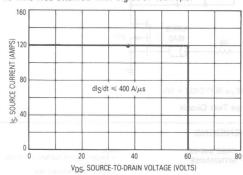


Figure 12. Commutating Safe Operating Area (CSOA)

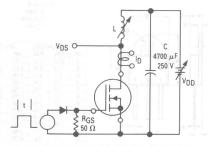


Figure 14. Unclamped Inductive Switching Test Circuit

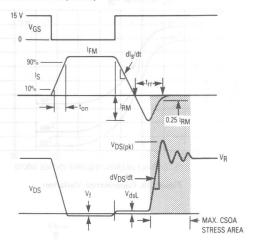


Figure 11. Commutating Waveforms

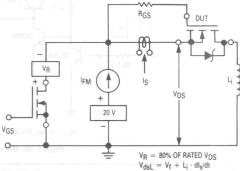


Figure 13. Commutating Safe Operating Area Test Circuit

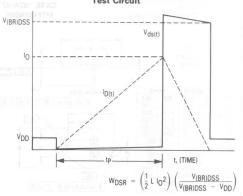


Figure 15. Unclamped Inductive Switching Waveforms

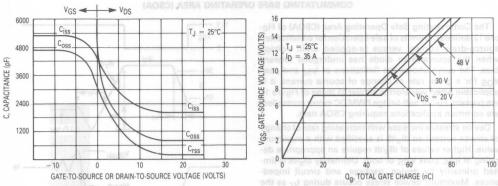
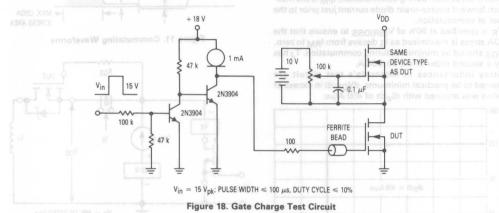
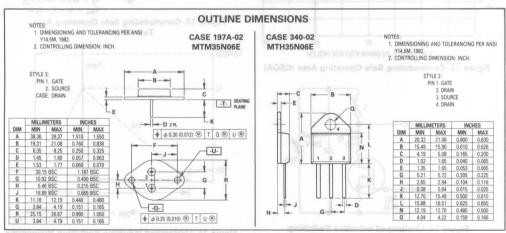


Figure 16. Capacitance Variation

Figure 17. Gate Charge versus





MOTOROLA SEMICONDUCTOR

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

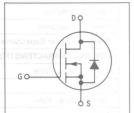
This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FET 35 AMPERES rDS(on) = 0.06 OHM 150 VOLTS

TMOS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	asaV b150 8.0 = sa	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	150	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	IDM	(100 saV	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	150 1.2	Watts W/°C
Operating and Storage Temperature Range	TJ, Tsta	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	R _θ JC R _θ JA	0.83 a brood source bond a	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	.vs °C, _{lov0}



CASE 340-02 TO-218AC

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS				
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA) MTH35N15	V _{(BR)DSS}	150	-	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, T_J = 125°C)	IDSS	=	10 100	μAdo
Gate-Body Leakage Current, Forward (V _{GSF} = 20 Vdc, V _{DS} = 0)	IGSSF	_	100	nAdd
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	_	100	nAdd

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ATA

Cha	racteristic	Symbol	Min	Max	Unit	
N CHARACTERISTICS*			195	BIG BIS	11 8 J.	signe.
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C		V _{GS(th)}	2 1.5	4.5 4	Vdc	
Static Drain-Source On-Resistance	(VGS = 10) Vdc, I _D = 17.5 Adc)	rDS(on)	201	0.06	Ohm
Drain-Source On-Voltage (VGS = (ID = 35 Adc) (ID = 17.5 Adc, TJ = 100°C)	10 V)	ltage, high	V _{DS(on)}	designed for	2.52 2.10	Vdc
Forward Transconductance (V _{DS}	= 10 V, I _D =	9FS	10	n bne bion	mhos	
YNAMIC CHARACTERISTICS		ng Times	ts — Switchi	Itching Speed	OT Fast Sw	on Gare
Input Capacitance	0	$V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss		5500	pF
Output Capacitance	,	f = 1 MHz)	Coss	1 - (uo) SG / -	1500	igner's Or Elevated ged — SC
Reverse Transfer Capacitance		See Figure 11	C _{rss}	Diss ip ation	500	
WITCHING CHARACTERISTICS* (1	Г _Ј = 100°С)	aductive Loads	or Use With I	naractarized for	10 eboid ni	erid-ot-sor
Turn-On Delay Time			td(on)	_	50	ns
Rise Time	(VDE	$R_{gen} = 25 \text{ V}, I_D = 0.5 \text{ Rated ID}$ $R_{gen} = 50 \text{ ohms}$	t _r	_	300	- ASI SVILIS
Turn-Off Delay Time	S	See Figures 9, 13 and 14	td(off)	_	150	
Fall Time	Hart I		tf	_	150	
Total Gate Charge	and C	V _{DS} = 0.8 Rated V _{DSS} ,	Qg	85 (Typ)	95	nC
Gate-Source Charge		= Rated ID, VGS = 10 V)	Qgs	45 (Typ)	= 0081.000	Land Street
Gate-Drain Charge		See Figure 12	Qgd	40 (Typ)	- CD - CO	W on work
OURCE DRAIN DIODE CHARACTE	RISTICS*	e20	VGS		V (20)	ntinuous
Forward On-Voltage	Урк	04年	V _{SD}	1.2 (Typ)	a 08 2 all a	Vdc
Forward Turn-On Time	obA	(I _S = Rated I _D , V _{GS} = 0)	ton	Limited by stray inductance		nce
Reverse Recovery Time	etes(A)	03 004	t _{rr}	200 (Typ)	i St. on its oin	ns
NTERNAL PACKAGE INDUCTANCE	OTW .	1.2	0	_ sasa D.	25°C	cate above
Internal Drain Inductance (Measured from the contact scr (Measured from the drain lead			T Ltd	4 (Typ) 5 (Typ)	Sterage Ten	tins nHm
Internal Source Inductance	*C/W	package to source bond pad)	MAR Ls	10 (Typ)	nut <u> </u>	nal Resist

	-									
*Pulse Test:	Pulse	Width	<	300	μS,	Duty	C	vcle	1	2%.

		Gate-Body Leakage Current, Forward (Viggr = 20 Vdc, Vpg = 0)

3

TYPICAL ELECTRICAL CHARACTERISTICS

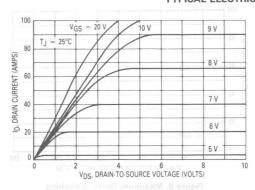


Figure 1. On-Region Characteristics

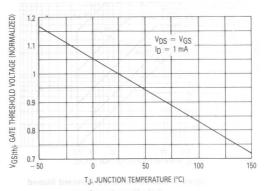


Figure 2. Gate-Threshold Voltage Variation With Temperature

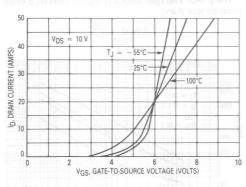


Figure 3. Transfer Characteristics

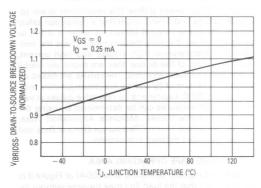


Figure 4. Breakdown Voltage Variation
With Temperature

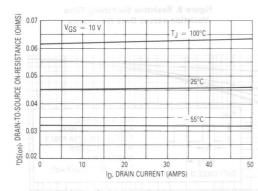


Figure 5. On-Resistance versus Drain Current

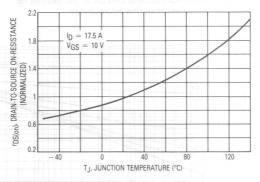


Figure 6. On-Resistance Variation With Temperature

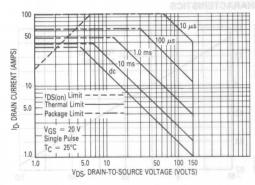


Figure 7. Maximum Rated Forward Biased Safe Operating Area

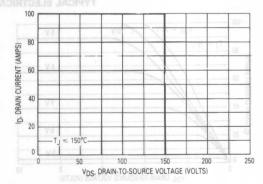


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-tosource voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

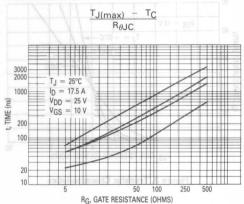


Figure 9. Resistive Switching Time Variation versus Gate Resistance

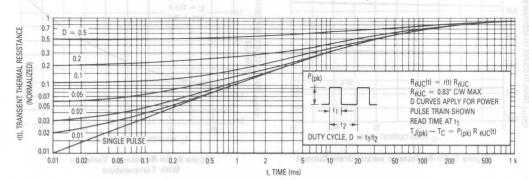


Figure 10. Thermal Response

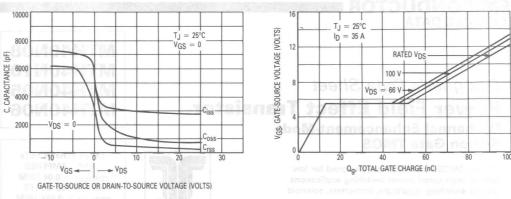


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus

Gate-to-Source Voltage

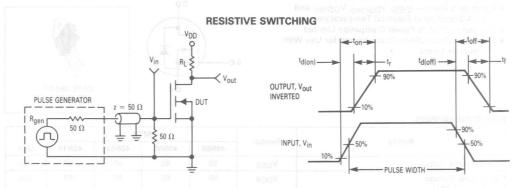
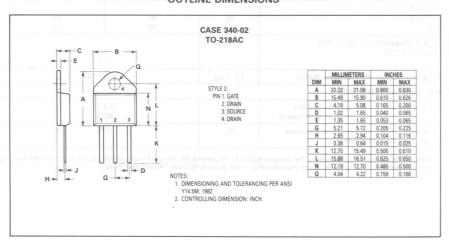


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

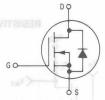
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTH40N08 MTH40N10 MTH40N05 MTH40N06

TMOS POWER FETS and AMPERES rDS(on) = 0.04 OHM 80 and 100 VOLTS rDS(on) = 0.028 OHM 50 and 60 VOLTS





CASE 340-02 TO-217AC

MAXIMUM RATINGS

Daties .	Cb-I		n a sM	TH		0
Rating my	Symbol	40N05	40N06	40N08	40N10	Unit
Drain-Source Voltage	V _{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	V _{DGR}	50	60	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive (t _p ≤ 50 μs)	V _{GS} V _{GSM}	0.573370	± 20 ± 40			Vdc Vpk
Drain Current Continuous Pulsed	I _D		40 40 140 120			Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	150 1.2			Watts W/°C	
Operating and Storage Temperature Range	T _J , T _{stg}		- 65	to 150		°C

THERMAL CHARACTERISTICS

1 (0.01) 1000 (0.00)	PLANTAGE TO THE REST OF THE PARTY OF THE PAR			
	Junction to Case Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.833 62.5	°C/W
Maximum Lead Temp. for 1/8" from case for 5 seco		TL	275	°C

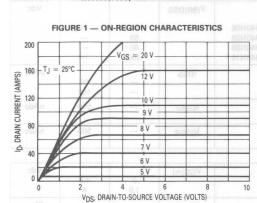
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

$\textbf{ELECTRICAL CHARACTERISTICS} \ \ - \ \ \textbf{continued} \ \ (T_{\text{C}} \ = \ 25^{\circ}\text{C unless otherwise noted})$

Charac	teristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	TM	801/10	akus, witha	ANTI	
Drain- Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)	MTH40N05 MTH40N06 MTH40N08 MTH40N10	V(BR)DSS	50 60 80 100	(1 - ± 5000)	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ	= 125°C)	IDSS	1	10 100	μAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		IGSSF	V 0	500	nAdc
Gate Body Leakage Current, Reverse (V _{GSR} = 20 Vdc, V _{DS} = 0)		IGSSR	V.S	500	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$ $T_{J} = 100^{\circ}\text{C}$	01	V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance $(V_{GS} = 10 \text{ Vdc}, I_D = 20 \text{ Adc})$	MTH40N05/06 MTH40N08/10	rDS(on)	_	0.028 0.04	Ohm
$ \begin{array}{lll} \mbox{Drain-Source On-Voltage } (V_{\mbox{GS}} = 10 \\ (I_{\mbox{D}} = 40 \mbox{ Adc}) \\ (I_{\mbox{D}} = 20 \mbox{ Adc}, T_{\mbox{J}} = 100^{\circ}\mbox{C}) \\ (I_{\mbox{D}} = 40 \mbox{ Adc}) \\ (I_{\mbox{D}} = 20 \mbox{ Adc}, T_{\mbox{C}} \mbox{100}^{\circ}\mbox{C}) \end{array} $	V) MTH40N05/06 MTH40N05/06 MTH40N08/10 MTH40N08/10	V _{DS(on)}	12 AS 180 AN	1.4 1.12 2 1.6	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 20 A)		9FS	10	_	mhos
YNAMIC CHARACTERISTICS	- arv + = =	100			
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	C _{iss}		5000	pF
Output Capacitance	f = 1 MHz)	Coss		2500	
Reverse Transfer Capacitance	See Figure 8	C _{rss}	<u>_</u>	1000	
WITCHING CHARACTERISTICS (TJ =	100°C)				
Turn-On Delay Time	1 D	td(on)		100	ns
Rise Time	$(V_{DD} = 25 \text{ V}, I_{D} = 0.5 \text{ Rated } I_{D})$	t _r	V 30161 <u>-</u> 1-01-11	330	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figure 16	td(off)	_	330	
Fall Time	C a ERUDR	tf	DRAW PURS	360	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Qg	105 (Typ)	120	nC
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 Vdc)	Qgs	74 (Typ)	_	
Gate-Drain Charge	See Figure 15	Q _{gd}	31 (Typ)	27	
SOURCE DRAIN DIODE CHARACTERIS	TICS	7:00			
Forward On-Voltage	(I _S = Rated I _D ,	V _{SD}	2.2 (Typ)	3	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	luctance
Reverse Recovery Time	100 2	t _{rr}	75 (Typ)		ns
NTERNAL PACKAGE INDUCTANCE	0	100000000000000000000000000000000000000			
Internal Drain Inductance (Measured from the contact screw (Measured from the drain lead 0.2		L _d	4 (Typ) 5 (Typ)	_	nH
Internal Source Inductance (Measured from the source lead 0.2)	5" from package to source bond pad)	L _s	10 (Typ)	<u>U.</u>	







MTH40N08, MTH40N10

FIGURE 2 — ON-REGION CHARACTERISTICS

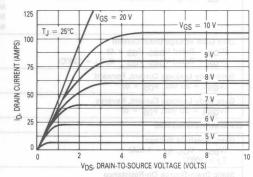


FIGURE 3 — TRANSFER CHARACTERISTICS

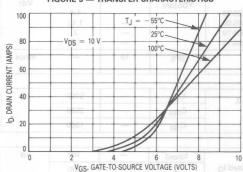


FIGURE 4 — TRANSFER CHARACTERISTICS

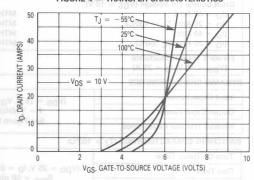


FIGURE 5 — ON-RESISTANCE versus DRAIN CURRENT

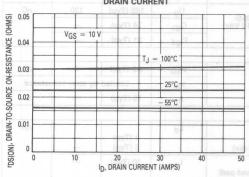
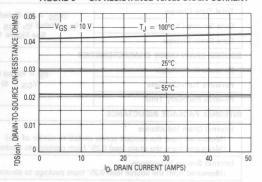


FIGURE 6 — ON-RESISTANCE versus DRAIN CURRENT



3

TYPICAL CHARACTERISTICS

FIGURE 7 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

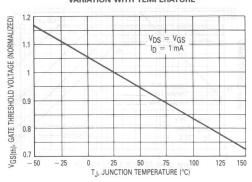


FIGURE 8 — CAPACITANCE VARIATION

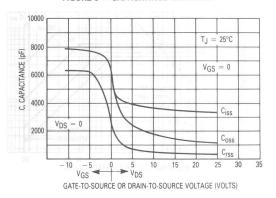


FIGURE 9 — BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE

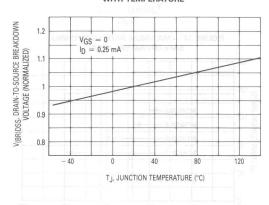


FIGURE 10 — ON-RESISTANCE VARIATION
WITH TEMPERATURE

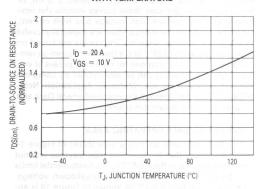
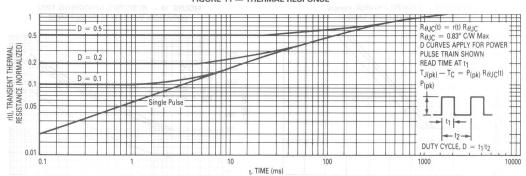


FIGURE 11 — THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

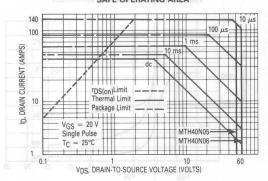
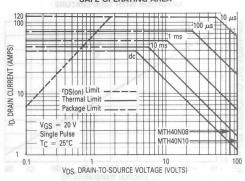


FIGURE 13 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:



FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

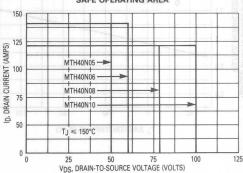


FIGURE 15 — STORED CHARGE versus

GATE-TO-SOURCE VOLTAGE

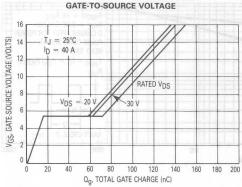
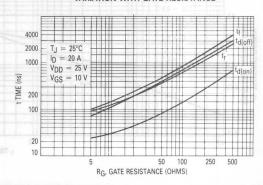


FIGURE 16 — RESISTIVE SWITCHING TIME VARIATION WITH GATE RESISTANCE



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

TMOS IV Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- DC Equivalent to IRFZ40



Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	8 mun 50 e 8	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	V _{DGR}	50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous (T _C = 25°C)	IDM	50 160	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	125 20V.A1d = 20	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stq}	-65 to 150	°C

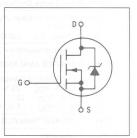
THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	R_{θ} JC R_{θ} JA	1 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL(alb l	275	q man°C i

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MTH50N05E

TMOS POWER FET 50 AMPERES rDS(on) = 0.028 OHM 50 VOLTS





MTH50N05E CASE 340-02 TO-218AC

Ch	aracteristic		Symbol	Min A	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)			V(BR)DSS	50	To'ra	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0 (VDS = Rated VDSS, VGS = 0		C)	IDSS	_	10 80	μΑ
Gate-Body Leakage Current, Forv	vard (VGSF	= 20 Vdc, V _{DS} = 0)	IGSSF	42-bl	100	nAdc
Gate-Body Leakage Current, Revi	erse (VGSR	= 20 Vdc, V _{DS} = 0)	IGSSR		100	nAdc
ON CHARACTERISTICS*		SAND HOURIE DIS	ONE ATTOR	SERVICE OF STREET	SHEET TON	231025143
Gate Threshold Voltage (VDS = VGS, ID = 250 μ A) T _J = 100°C		FETs is designed to withstan . These new energy efficient	VGS(th)	2	4 3.5	ob Vdc
Static Drain-Source On-Resistance	e (VGS = 1	0 Vdc, I _D = 25 Adc)	rDS(on)	ei ae o stesile	0.028	Ohm
Drain-Source On-Voltage (V _{GS} = (I _D = 50 Adc) (I _D = 25 Adc, T _J = 100°C)		bridge circuits where diode offer additional safety margi	V _{DS(on)}	articularly ving area and	1.4 as 1.3	b s Vdc gritatum
Forward Transconductance (VDS	= 15 V. In	= 25 A)	g _{FS}	17		mhos
RAIN-TO-SOURCE AVALANCHE C			seor — Abso	DO DOMEST	lica-to-prai lener Trans	Sternetz
Unclamped Inductive Switching II (ID = 160 A, VDD = 25 V, TC = (ID = 50 A, VDD = 25 V, TC = (ID = 20	25°C, Sing 25°C, P.W.	le Pulse, Non-repetitive) ≤ 45 μs, Duty Cycle ≤ 1%)	WDSR	UIS) Energy reting Area Bridge Circu	60 135 50	Lm ¹ Vm ¹ Inductive at 100°C.
OYNAMIC CHARACTERISTICS	850	MT s or olds	твато Сетран	ji yasvoosh	eborO nior	ji vi sen
Input Capacitance		$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss	ev Diode	3000	ete PE
Output Capacitance		f = 1 MHz) See Figure 16	Coss	tor (Js a in s	1200	de is Cha
Reverse Transfer Capacitance			C _{rss}		400	Equival:
SWITCHING CHARACTERISTICS* (T _J = 100°C)		1		
Turn-On Delay Time	(Vr	DD = 25 V, ID = 0.5 Rated ID	td(on)	= 25 to unie	25	ns
Rise Time	1 mU	$R_{gen} = 4.7 \text{ ohms}$	t _r	90	60	
Turn-Off Delay Time	5 EsV	See Figure 9	td(off)	_	70 nov	in-Source
Fall Time	167	Voca 50	tf	= 1 M(U)	25	V arsiD-nis
		(VDS = 0.8 Rated VDSS,	Qg	55 (Typ)	60	nC
Total Gate Charge	307		Qqs	30 (Typ)	И — —	
Gate-Source Charge		= Rated ID, VGS = 10 V)	ags			
Gate-Source Charge Gate-Drain Charge	agV I _E		Q _{gd}	25 (Typ)	— C os tinuc	in Curren
Gate-Source Charge Gate-Drain Charge COURCE DRAIN DIODE CHARACTE	agV I _E	= Rated ID, VGS = 10 V)	-	25 (Typ)	— C os tinue — Pulsed	
Gate-Source Charge Gate-Drain Charge COURCE DRAIN DIODE CHARACTE Forward On-Voltage	agV I _E	= Rated ID, VGS = 10 V)	-	25 (Typ)	2.5	Vdc
Gate-Source Charge Gate-Drain Charge COURCE DRAIN DIODE CHARACTE Forward On-Voltage Forward Turn-On Time	agV I _E	See Figures 17 and 18	Q _{gd}	1.9 (Typ) Limited	by stray ind	Vdc
Gate-Source Charge Gate-Drain Charge GOURCE DRAIN DIODE CHARACTE Forward On-Voltage Forward Turn-On Time Reverse Recovery Time	ERISTICS*	D = Rated ID, V _{GS} = 10 V) See Figures 17 and 18 (I _S = 51 A, V _{GS} = 0,	Q _{gd}	1.9 (Typ)	7 30 01	Vdc
Gate-Source Charge Gate-Drain Charge OURCE DRAIN DIODE CHARACTE Forward On-Voltage Forward Turn-On Time Reverse Recovery Time	ERISTICS*	D = Rated ID, V _{GS} = 10 V) See Figures 17 and 18 (I _S = 51 A, V _{GS} = 0,	O _{gd}	1.9 (Typ) Limited	by stray ind	Vdc
Gate-Source Charge Gate-Drain Charge OURCE DRAIN DIODE CHARACTE Forward On-Voltage Forward Turn-On Time	ERISTICS* E (TO-218) crew on tab	See Figures 17 and 18 $(I_S = 51 \text{ A, V}_{GS} = 0, \\ dI_{S}/dt = 100 \text{ A/}\mu\text{s})$ to center of die)	O _{gd}	1.9 (Typ) Limited	by stray ind	Vdc

^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

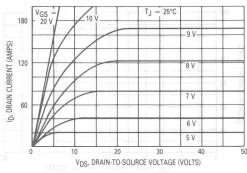


Figure 1. On-Region Characteristics

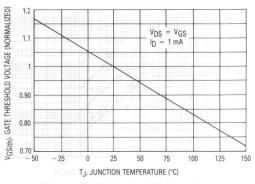


Figure 2. Gate-Threshold Voltage Variation

With Temperature

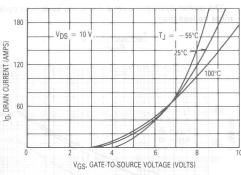


Figure 3. Transfer Characteristics

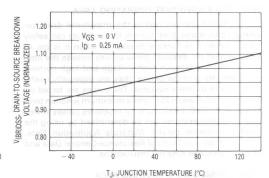


Figure 4. Breakdown Voltage Variation

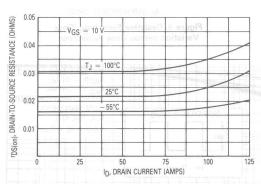


Figure 5. On-Resistance versus Drain Current

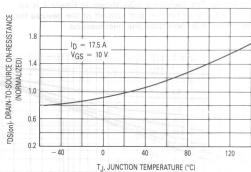


Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

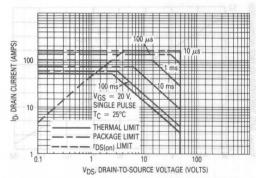


Figure 7. Maximum Rated Forward Biased Safe Operating Area

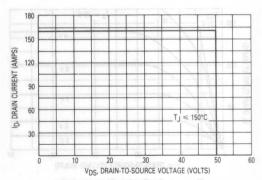


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

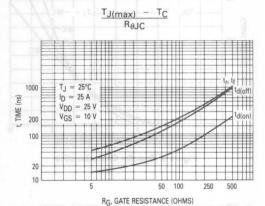


Figure 9. Resistive Switching Time Variation versus Gate Resistance

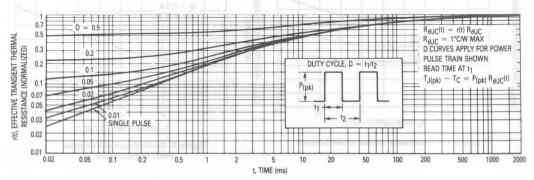


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dl_s/dt is specified with a maximum value. Higher values of dl_s/dt require an appropriate derating of l_{FM} , peak V_{DS} or both. Ultimately dl_s/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

V_{DS(pk)} is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

 $V_{\mbox{\scriptsize R}}$ is specified at 80% of V(BR)DSS to ensure that the CSOA stress is maximized as IS decays from IRM to zero.

RGS should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dVpg/dt in excess of 10 V/ns was attained with dle/dt of 400 A/us.

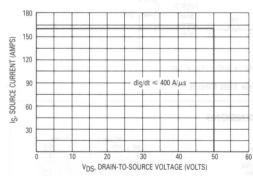


Figure 12. Commutating Safe Operating Area (CSOA)

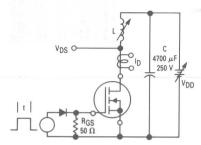


Figure 14. Unclamped Inductive Switching Test Circuit

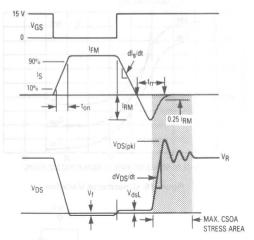


Figure 11. Commutating Waveforms

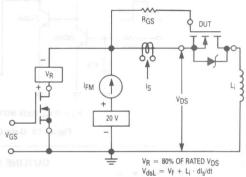


Figure 13. Commutating Safe Operating Area
Test Circuit

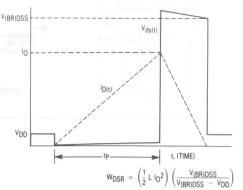
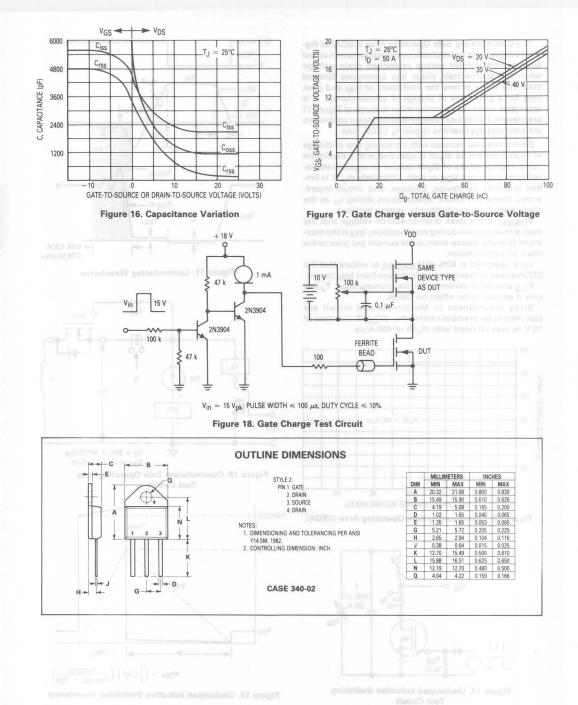


Figure 15. Unclamped Inductive Switching Waveforms



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

Rating	Symbol	MTM1N95	MTM1N100	Unit
riating	10/6/11/20	MTP1N95	### MTP1N100	
Drain-Source Voltage	V _{DSS}	950	1000	Vdc
Drain-Gate Voltage (R _{GS} = 1 M Ω)	V _{DGR}	950	8 1000 ad	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS}			Vdc Vpk
Drain Current — Continuous — Pulsed	IDM	201.0	1 6	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		75 20 ^V 0.6	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{sta}	- 65	to 150	°C (

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	TO-204 TO-220	R_{θ} JC	1.67 30 62.5	°C/W
Maximum Lead Temperatur Purposes, 1/8" from case t		TL	275	O°220)

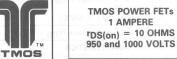
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

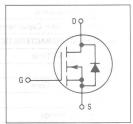
Characteristic (AVT) 8.44	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	لع			
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA) MTM1N95/MTP1N95 MTM1N100/MTP1N100	V(BR)DSS	950 1000	packaga to s 	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0, $T_J = 125^{\circ}C$)	IDSS	=	0.2 1	mAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	IGSSF	<u>—</u>	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	_	100	nAdc

continued)

MTM1N100 MTP1N95 MTP1N100

MTM1N95







MTM1N95 MTM1N100 CASE 1-06 TO-204AA



MTP1N95 MTP1N100 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are give to facilitate "worst case" design.



Characteristic			Symbol	Min	Max	Unit	
ON CHARACTERISTICS*				10	pure pr	BM 6 1	andle.
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C				V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistanc	Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 0.5 Adc)			rDS(on)	-20	10	Ohms
Drain-Source On-Voltage (VGS = (ID = 0.5 Adc) (ID = 0.5 Adc, TJ = 100°C)	10 V)	9	tage, high	V _{DS(on)}	are designed	5 10	Vdc
Forward Transconductance (VDS	= 15 V, ID =	= 0.5 A)	- Samunigati	9FS	0.5	en br o bion	mhos
DYNAMIC CHARACTERISTICS	u		a Times	-	ching Speeds	o Fast Swif	icon Gate fi
Input Capacitance		/ 25.1/		Ciss	I	1200	pF
Output Capacitance		f = 25 V, $f = 1 N$	$V_{GS} = 0,$ (Hz)	Coss	DS(Upp) Val	300	signer's Da
Reverse Transfer Capacitance		See Figu		C _{rss}	Dissignation L	80	iged — 80
SWITCHING CHARACTERISTICS* (Γ ₁ = 100°C)		avisoubs	I MANA REO TO	eracterizad to	ID DIDCE UK	57U-07-991L
Turn-On Delay Time				td(on)	T -	50	ns
Rise Time	(V _{DS}	= 125 V, I _D	= 0.5 Rated ID	tr		150	IMUM PAT
Turn-Off Delay Time	start t	$R_{gen} = 50$	ohms)	t _d (off)	—	200	-
Fall Time	50	ee Figures 9,	, 13 and 14	t _f		100	
Total Gate Charge	Vete	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V)		Qg	33 (Typ)	37	nC
Gate-Source Charge				Qgs	20 (Typ)	- 2010-004	in-Cate Vall
Gate-Drain Charge	יטי		See Figure 12	Q _{gs}	13 (Typ)	Haga	e Source Vi
SOURCE DRAIN DIODE CHARACTE	RISTICS*	- 3	AZ AZ	- aga	13 (190)	814 06 2 g/l 8	onundous lon-repetitive
Forward On-Voltage	abA .			V _{SD}	1 (Typ)	1.3	Vdc
Forward Turn-On Time		(IS = Rated ID,		ton		tray inductar	1.55
Reverse Recovery Time	Watts	V _{GS} =	= (0)	t _{rr}	725 (Typ)	-490	ns
NTERNAL PACKAGE INDUCTANCE	(TO-204)		et 28	-T /T	control customs	meT ensut	
Internal Drain Inductance (Measured from the contact scr to the source pin and the cente	rew on the h	eader closer		Ld	5 (Typ)	RACTERIST	AHONHAAR
Internal Source Inductance (Measured from the source pin to the source bond pad)		the package	7.6 30 30 62.1	L _S	12.5 (Typ)	meldent	nH nH
NTERNAL PACKAGE INDUCTANCE	(TO-220)		100	-17	of Seconds	restance quantity	Daed niumis
Internal Drain Inductance (Measured from the contact sci (Measured from the drain lead				o asella ora	3.5 (Typ) 4.5 (Typ)	ARACTERII Churuzierishi	nH _M
Internal Source Inductance (Measured from the source lead				L _S	7.5 (Typ)	STICS.	HETOARAK
*Pulse Test: Pulse Width ≤ 300 μs, Duty	200.0			- Lander	7167		VGS = 0, 10
		yole ≈ 276.					

TYPICAL ELECTRICAL CHARACTERISTICS

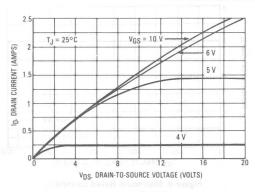


Figure 1. On-Region Characteristics

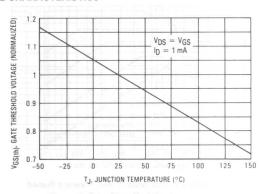


Figure 2. Gate-Threshold Voltage Variation With Temperature

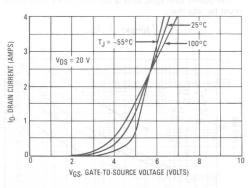


Figure 3. Transfer Characteristics

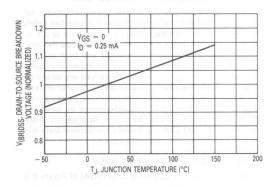


Figure 4. Breakdown Voltage Variation With Temperature

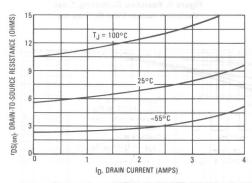


Figure 5. On-Resistance versus Drain Current

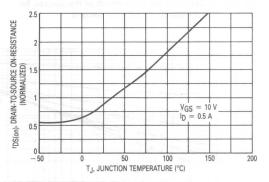


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

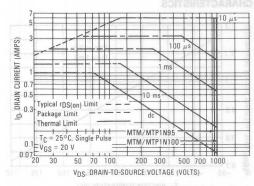


Figure 7. Maximum Rated Forward Biased Safe Operating Area

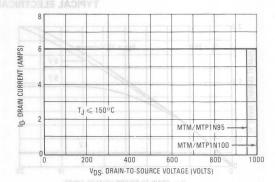


Figure 8. Maximum Rated Switching
Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

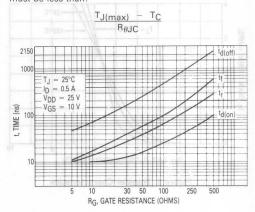


Figure 9. Resistive Switching Time
Variation versus Gate Resistance

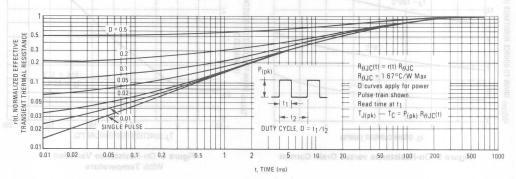
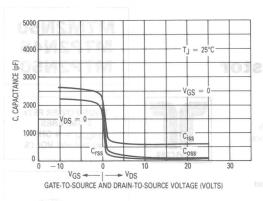


Figure 10. Thermal Response



16 VDS = 330 V 800 V 800 V 500 V 7 J = 25°C VDS = 1 A VDS = 1 A VDS = 1 A VDS = 20 A VDS

Figure 11. Capacitance Variation

 $z = 50 \Omega$

₹ 50 Ω

Figure 12. Gate Charge versus
Gate-to-Source Voltage

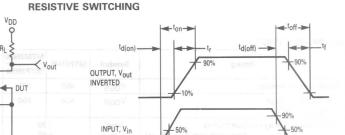


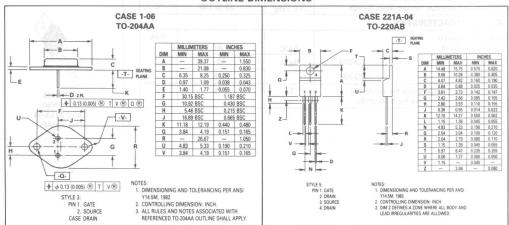
Figure 13. Switching Test Circuit

PULSE GENERATOR

50 Ω

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



Designer's Data Sheet

SEMICONDUCTOR

MOTOROLA

TECHNICAL DATA

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

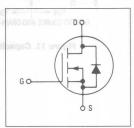
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MTM2N50 MTP2N45 MTP2N50

TMOS POWER FETS
2 AMPERES
rDS(on) = 4 OHMS
450 and 500 VOLTS

TMOS



MAXIMUM RATINGS

3

Rating Ass	Comphal	MTP2N45	MTM2N50	Unit
Rating	Symbol	WITP2N45	MTP2N50	Unit
Drain-Source Voltage	VDSS	450	500	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	450	500	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}		20 40	Vdc Vpk
Drain Current Continuous Pulsed	I _D		2	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		75 .6	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	- 65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204	R_{θ} JA	30	生甘甜
	TO-220		62.5	
Maximum Lead Temperature f Purposes, 1/8" from case for		TL	275	°C



MTM2N50 CASE 1-06 TO-204AA



MTP2N45 MTP2N50 CASE 221A-04 TO-220AB

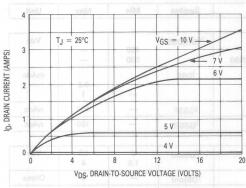
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Char	acteristic	G	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				1		
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)		ΓΡ2N45 ΓΜ/MTP2N50	V(BR)DSS	450 500	=	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = Rated V_{DSS}, V_{GS} = 0$) ($V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0.8 Rated V_{DSS}$)	0, T _J = 125°C)	100 At 1	IDSS		0.2 1	mAdd
Gate-Body Leakage Current, Forwa	rd (VGSF = 20 Vdc, VD	S = 0)	IGSSF	_	100	nAdd
Gate-Body Leakage Current, Rever	se (VGSR = 20 Vdc, VD	S = 0)	IGSSR	_	100	nAdd
ON CHARACTERISTICS*		6				
Gate Threshold Voltage ($V_{DS} = V_0$ $T_J = 100^{\circ}C$	GS, ID = 1 mA)		VGS(th)	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	$(V_{GS} = 10 \text{ Vdc}, I_D = 1)$	Adc)	rDS(on)	WA HOMPONEOUS	4	Ohm
Drain-Source On-Voltage (VGS = 1 (ID = 2 Adc) (ID = 1 Adc, TJ = 100°C)			V _{DS} (on)	d3 noigail-i	10 8	Vdc
Forward Transconductance (VDS =	= 15 V, I _D = 1 A)		9FS	1		mhos
DYNAMIC CHARACTERISTICS		ē				
Input Capacitance	(V _{DS} = 25 V,	Voc = 0	C _{iss}	78 <u>-</u> U	500	pF
Output Capacitance	$\int_{0}^{\infty} \int_{0}^{\infty} \int_{0$	Coss	-789-	100		
Reverse Transfer Capacitance	See Figur	re 11	C _{rss}	_	50	1
SWITCHING CHARACTERISTICS* (T	j = 100°C)	E 8		1		1
Turn-On Delay Time		td(on)	\ -	40	ns	
Rise Time	(V _{DD} = 25 V, I _D =		tr	4 -	60	
Turn-Off Delay Time	R _{gen} = 50 See Figures 9,		td(off)	1,-	60	1
Fall Time			tf	1 <u>V</u>	30	
Total Gate Charge	(V _{DS} = 0.8 Ra	ted Voce	Ωg	17 (Typ)	25	nC
Gate-Source Charge	I _D = Rated I _D , V	GS = 10 V	Qgs	9 (Typ)	_	1
Gate-Drain Charge	See Figur	re 12	Q _{gd}	8 (Typ)	r The way	
SOURCE DRAIN DIODE CHARACTER	ISTICS*		estralvetos	anster Clara	T. Green	
Forward On-Voltage	(I _S = Rat	ed In	V _{SD}	1 (Typ)	1.5	Vdc
Forward Turn-On Time	V _{GS} =		ton	Limited	by stray ind	luctance
Reverse Recovery Time			t _{rr}	200 (Typ)	_	ns
NTERNAL PACKAGE INDUCTANCE	TO-204)					
Internal Drain Inductance (Measured from the contact scre to the source pin and the center			Ld	5 (Typ)	-	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L _S	12.5 (Typ)	<u> </u>		
NTERNAL PACKAGE INDUCTANCE (TO-220)	1			The state of the s	1
Internal Drain Inductance (Measured from the contact scre (Measured from the drain lead 0			L _d	3.5 (Typ) 4.5 (Typ)		nH
Internal Source Inductance (Measured from the source lead			L _S	7.5 (Typ)		

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS SOURCESTOASIANO MADISTORIA



1.1 VDS = VGS ID = 1 mA

VDS = VGS
ID = 1 mA

VDS = VGS
ID = 1 mA

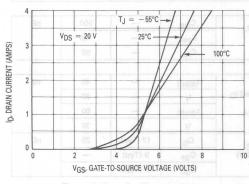
VDS = VGS
ID = 1 mA

VDS = VGS
ID = 1 mA

VDS = VGS
ID = 1 mA

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



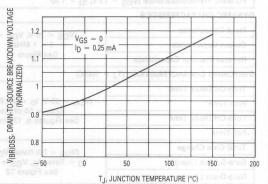
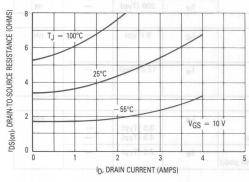


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation With Temperature



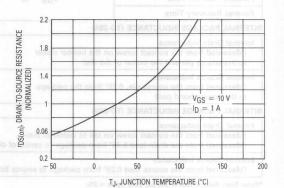


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

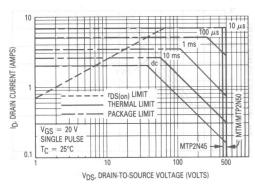


Figure 7. Maximum Rated Forward Biased Safe Operating Area

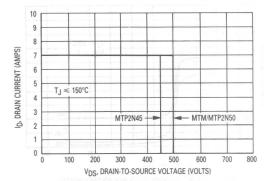


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

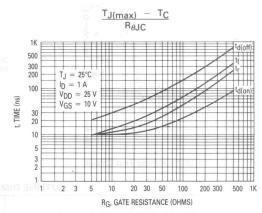


Figure 9. Resistive Switching Time Variation versus Gate Resistance

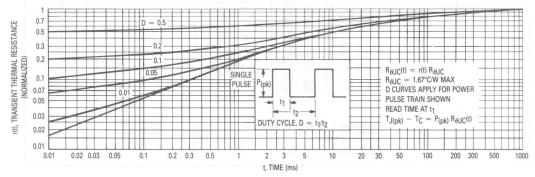
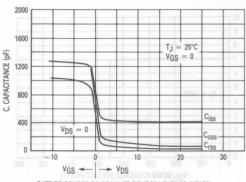


Figure 10. Thermal Response



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 11. Capacitance Variation

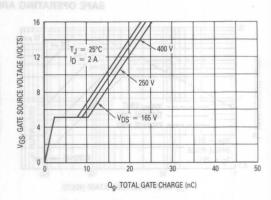


Figure 12. Gate Charge versus Gate-to-Source Voltage

A SERVICE

RESISTIVE SWITCHING

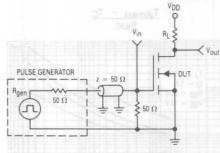


Figure 13. Switching Test Circuit

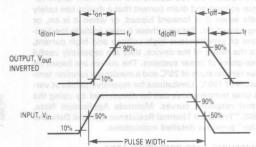
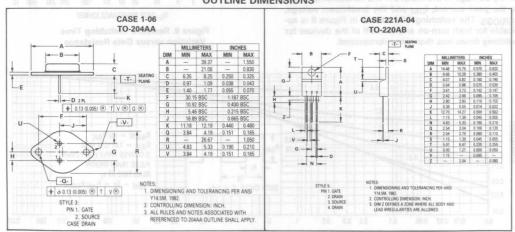


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

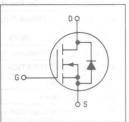
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS 2 AMPERES rDS(on) = 8 OHMS 850 and 900 VOLTS



MAXIMUM RATINGS

an at salb	Cumbal	MTM2N85	MTM2N90	Unit	
Rating	Symbol	MTP2N85	MTP2N90	Unit	
Drain-Source Voltage	V _{DSS}	850	900	Vdc	
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	850	900	Vdc	
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	DESTRUCTION OF THE PROPERTY OF	20 40	Vdc Vpk	
Drain Current — Continuous — Pulsed	I _D	jure 12	2 se3 7	Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		.6	Watts W/°C	
Operating and Storage Temperature Range	T _J , T _{stg}	-65	to 150	°C	

THERMAL CHARACTERISTICS

Thermal Resistance				°C/W
Junction to Case	foyTia Lg	$R_{\theta JC}$	1.67	
Junction to Ambient	TO-204	$R_{\theta JA}$	30	er adt no
	TO-220		62.5	- 10 4/12
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C



MTM2N85 MTM2N90 CASE 1-06 TO-204AA



MTP2N85 MTP2N90 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

ELECTRICAL CHARACTERIS	1109 (1C = 59	C unless otherwise no	tea)		1	ALALL	
	Characteristic			Symbol	Min	Max	Unit
OFF CHARACTERISTICS							
Drain-Source Breakdown Vol (VGS = 0, ID = 0.25 mA)	ltage	MTM/MTP2 MTM/MTP2		V(BR)DSS	850 900	's Da	Vdc
Zero Gate Voltage Drain Cur (VDS = Rated VDSS, VGS (VDS = 0.8 Rated VDSS, V	= 0)	125°C)	5010	I _{DSS}	ieu <u>l</u> eau	0.2 1	mAdc
Gate-Body Leakage Current,	Forward (VGSF	$=$ 20 Vdc, $V_{DS} = 0$)		IGSSF	_00	100	nAdc
Gate-Body Leakage Current,	Reverse (VGSR	$=$ 20 Vdc, $V_{DS} = 0$)	id .apst	IGSSR	are designe	100	nAdc
ON CHARACTERISTICS*		ators,	g regula	h as switchin	cations auc	ching appli	power swit
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C				V _{GS(th)}	2 1.5	4.5	on Gate for pecified at 1
Static Drain-Source On-Resis	stance (VGS = 1	0 Vdc, I _D = 1 Adc)	A Speci	rDS(on)	DS(se). VG	888	Ohms
Drain-Source On-Voltage (V _C (I _D = 2 Adc) (I _D = 1 Adc, T _J = 100°C)	GS = 10 V)	e Loads	Inductiv	V _{DS(on)}	Dissipation Practerized	20 16	Nos Vdc
Forward Transconductance (V _{DS} = 15 V, I _D	= 1 A)		9FS	0.5	_	mhos
DYNAMIC CHARACTERISTICS							
Input Capacitance		(V _{DS} = 25 V, V _{GS} = 0	1	Ciss		1200	pF
Output Capacitance		f = 1 MHz	,	Coss	_	300	1
Reverse Transfer Capacitanc	e	See Figure 11		C _{rss}	_	80	
SWITCHING CHARACTERISTIC)				108	MUM RATIF
Turn-On Delay Time		MTM2N86 WTM2N80		td(on)	_	50	ns
Rise Time	(V _{DE}	$_{\rm D} = 125 \text{V}, \text{I}_{\rm D} = 0.5 \text{Ra}$	ted ID	tr	_	150	
Turn-Off Delay Time	Vde	$R_{gen} = 50 \text{ ohms}$) See Figures 9, 13 and 1	4 220	td(off)	_	200	n-Source Vott
Fall Time	Vdc	000 088		tf	-(010)	100	n-Gate Voltro
Total Gate Charge	vbV	(V _{DS} = 0.8 Rated V _{DS}	, aav	Qg	33 (Typ)	40	ON a nC
Gate-Source Charge		= Rated ID, VGS = 10	5'	Qgs	20 (Typ)	-noVI <u>-</u>	
Gate-Drain Charge	strA	See Figure 12		Q _{qd}	13 (Typ)	enonuluo.	n Current (
SOURCE DRAIN DIODE CHARA	ACTERISTICS*		MG		2000	Dealer III	
Forward On-Voltage	D*W	(I _S = Rated I _D	-01	V _{SD}	1 (Typ)	1.4	Vdc
Forward Turn-On Time)°	V _{GS} = 0)		ton	Limited	by stray in	ductance
Reverse Recovery Time				t _{rr}	420 (Typ)	CTENSTN	ns
NTERNAL PACKAGE INDUCTA	ANCE (TO-204)					90	mail Resisten
Internal Drain Inductance (Measured from the contact to the source pin and the contact			OLR ² ALR ²	L _d	5 (Typ)	e s	netion to Cas netion to Am
Internal Source Inductance (Measured from the source to the source bond pad)	e pin, 0.25" from	the package	jī	L _S	12.5 (Typ)	emperatura rom casa fo	imum Load F Irposes, 1/8 1
NTERNAL PACKAGE INDUCTA	ANCE (TO-220)						
Internal Drain Inductance (Measured from the contac (Measured from the drain			e)	L _d	3.5 (Typ) 4.5 (Typ)	_	nH
Internal Source Inductance (Measured from the source	a lead 0.25" from			L _S	7.5 (Typ)	_	

^{*}Pulse Test: Pulse Width \leq 300 μs , Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

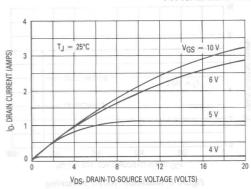


Figure 1. On-Region Characteristics

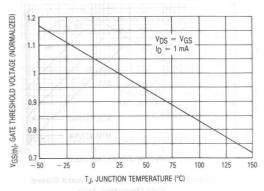


Figure 2. Gate-Threshold Voltage Variation
With Temperature

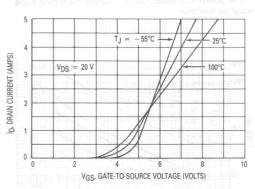


Figure 3. Transfer Characteristics

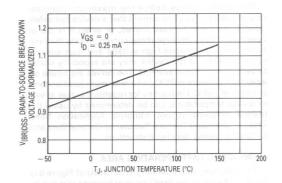


Figure 4. Breakdown Voltage Variation
With Temperature

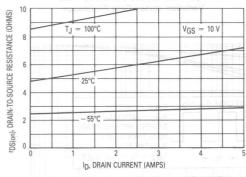


Figure 5. On-Resistance versus Drain Current

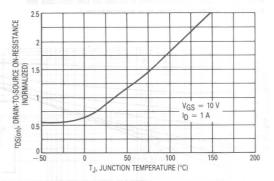


Figure 6. On-Resistance Variation
With Temperature

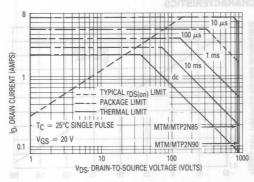


Figure 7. Maximum Rated Forward Biased Safe Operating Area

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

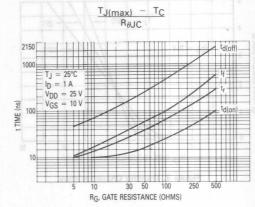


Figure 9. Resistive Switching Time Variation versus Gate Resistance

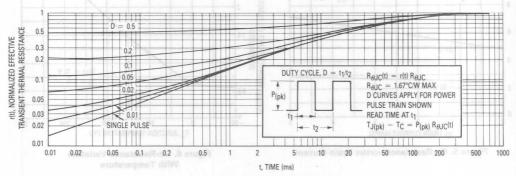
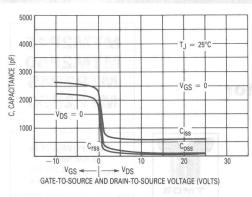


Figure 10. Thermal Response



12 V_{DS} = 330 V 800 V 500 V T_J = 25°C V_D = 2 A V_D

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

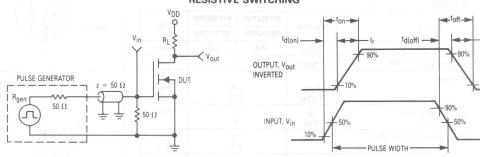
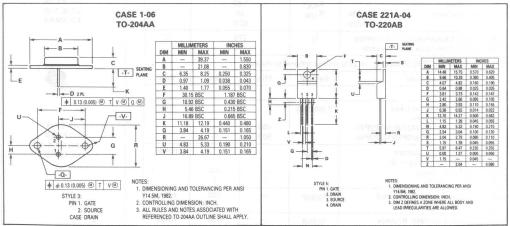


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

P-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

-45-110 ¹ -50-1	Comphal	MTM2P45	MTM2P50	Unit
Rating	Symbol	MTP2P45	MTP2P50	Omit
Drain-Sourve Voltage	V _{DSS}	450	500	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	450	500	Vdc
Gate-Source Voltage Continuous Non-repetitive (t _p ≤ 50 μs)	V _{GS} V _{GSM}		20 40	Vdc Vpk
Drain Current Continuous Pulsed	I _D		2	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		'5 .6	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient Junction to Ambient TO-220	R _θ JC R _θ JA	1.67 30 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

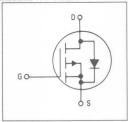
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	Librilia		1.000 111	00.7 Z Nt.bs 3
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA) MTM2P45/MTP2P45 MTM2P50/MTP2P50	V(BR)DSS	450 500	1215 0 238 1215 0 238 1010 0 238 1010 0 215 1110 0 1124 1110 0 1135	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0$) ($V_{DS} = 0.8\ Rated\ V_{DSS},\ V_{GS} = 0,\ T_J = 125^{\circ}\text{C}$)	IDSS		0.2	mAdo
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	IGSSF		100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	4 %	100	nAdc

(continued)

MTM2P45 MTM2P50 MTP2P45 MTP2P50



TMOS POWER FETS 2 AMPERES rDS(on) = 6 OHMS 450 and 500 VOLTS





MTM2P45 MTM2P50 CASE 1-06 TO-204AA

RRED



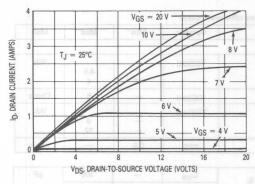
MTP2P45 MTP2P50 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Charac	teristic	Symbol	Min	Max	Unit	
ON CHARACTERISTICS*	\$ -v3					
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$ $T_{J} = 100^{\circ}\text{C}$	V _{GS(th)}	2 1.5	4.5 4	Vdc		
Static Drain-Source On-Resistance (V	'GS = 10 Vdc, I _D = 1 Adc)	rDS(on)		6	Ohm	
Drain-Source On-Voltage (V _{GS} = 10 (I _D = 1 Adc) (I _D = 1 Adc, T _J = 100°C)	V)	V _{DS(on)}	la +	6 12	Vdc	
Forward Transconductance (V _{DS} =	9FS	0.5		mhos		
DYNAMIC CHARACTERISTICS	20 5 -50 0	81	8 12	N		
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	C _{iss}	DA GROVE STOPPSALE	100	pF	
Output Capacitance	(sHM t = frigure 2. Gar	Coss	n-Rey lo n Cha	200		
Reverse Transfer Capacitance	See Figure 11	C _{rss}	_	80		
SWITCHING CHARACTERISTICS* (TJ	= 100°C)					
Turn-On Delay Time		^t d(on)		50	ns	
Rise Time	(V _{DS} = 125 V, I _D = 0.5 Rated I _D	tr	// - /	100		
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	^t d(off)	1 /0*85	150		
Fall Time Am	0 = 0.21	gas t _f T		50		
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Qg	20 (Typ)	25	nC	
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 V)	Qgs	10 (Typ)			
Gate-Drain Charge	See Figure 12	Qgd	10 (Typ)			
SOURCE DRAIN DIODE CHARACTERIS	TICS*		1			
Forward On-Voltage	- E	V _{SD}	1.8 (Typ)	2.5	Vdc	
Forward Turn-On Time	$(I_S = Rated I_D V_{GS} = 0)$	ton	Limited by st	ray inducta	nce	
Reverse Recovery Time	0 00	t _{rr}	120 (Typ)		ns	
NTERNAL PACKAGE INDUCTANCE (T	0-204)	121 JDV 12	ATTOV TO A TOT OT	TTAGY ON U		
Internal Drain Inductance (Measured from the contact screw and the center of the die)	on the header closer to the source pin	L _d ctenstics	5 (Typ)	T E engel	nH	
Internal Source Inductance (Measured from the source pin 0.25 pad)	" from the package to the source bond	L _S	12.5 (Typ)	_		
NTERNAL PACKAGE INDUCTANCE (T	O-220)			VVI = 2.90		
Internal Drain Inductance (Measured from contact screw on (Measured from the drain lead 0.2		Ld	3.5 (Typ) 4.5 (Typ)	-	nH	
Internal Source Inductance	The Bridge	Ls	7.5 (Typ)	- 1		

3

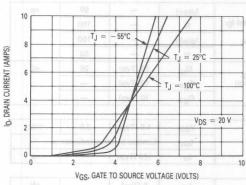
TYPICAL ELECTRICAL CHARACTERISTICS



1.1 VDS = VGS | VDS = VDS | VDS | VDS = VD

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



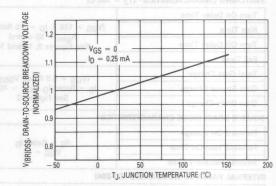
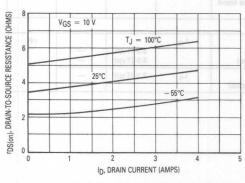


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation With Temperature



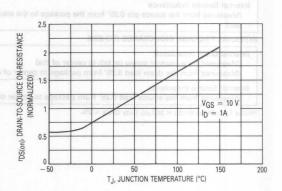


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

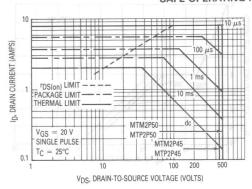


Figure 7. Maximum Rated Forward Biased Safe Operating Area

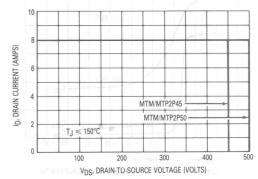


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

Figure 9. Resistive Switching Time Variation versus Gate Resistance

RG, GATE RESISTANCE (OHMS)

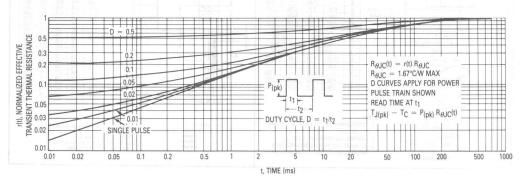
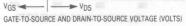


Figure 10. Thermal Response

2000

1600



- 10 - 15 - 20 - 25 - 30

T₁ = 25°C

Ciss

Coss Crss

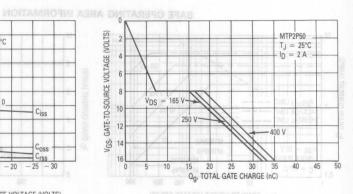


Figure 12. Gate Charge versus Gate-to-Source Voltage

Figure 11. Capacitance Variation

elovo gaudotive atelamos a revo begareva riRESISTIVE SWITCHING

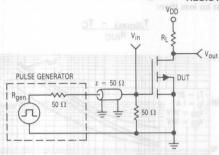


Figure 13. Switching Test Circuit

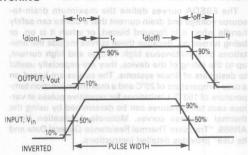
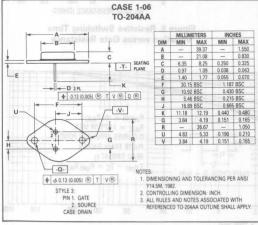
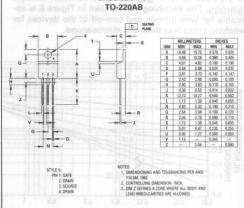


Figure 14. Switching Waveforms

CASE 221A-04

OUTLINE DIMENSIONS





MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

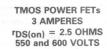
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

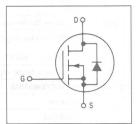
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS



MAXIMUM RATINGS

	Rating	instal	Symbol	MTP3N55	MTM3N60 MTP3N60	Unit
Drain-Source Voltage		-1	VDSS	550	600	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	-	(Ho)b [‡]	V _{DGR}	550	600	Vdc
Gate-Source Voltage –	- Continuous - Non-repetitive (t _p ≤	50 μs)	V _{GS} V _{GSM}		20 40	Vdc Vpk
Drain Current Continuous Pulsed	(ay1) 8 (ay1) 8	ogC Ogc	I _D	St aug 3 aug 10		Adc
Total Power Dissipatio Derate above 25°C	n @ T _C = 25°C	asy	PD		75 .6	Watts W/°C
Operating and Storage Temperature Range		nes	TJ, T _{stg}	- 65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance				°C/W
Junction to Case		$R_{\theta JC}$	1.67	
Junction to Ambient	TO-204	$R_{\theta JA}$	30 0 190891	on the
	TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C



MTM3N60 CASE 1-06 TO-204AA



MTP3N55 MTP3N60 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) Min Characteristic Symbol Max OFF CHARACTERISTICS Drain-Source Breakdown Voltage Vdc V(BR)DSS $(V_{GS} = 0, I_{D} = 0.25 \text{ mA})$ MTP3N55 550 MTM/MTP3N60 600 Zero Gate Voltage Drain Current IDSS mAdc (VDS = Rated VDSS, VGS = 0) 0.2 $(V_{DS} = 0.8 \text{ Rated } V_{DSS}, V_{GS} = 0, T_{J} = 125^{\circ}C)$ Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0) IGSSF 100 nAdc Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0) IGSSR 100 nAdc **ON CHARACTERISTICS*** Gate Threshold Voltage 2 VGS(th) 4.5 Vdc $(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$ 1.5 4 T_J = 100°C Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 1.5 Adc) Ohms rDS(on) 25 Drain-Source On-Voltage (VGS = 10 V) V_{DS}(on) Vdc 9 $(I_D = 3 Adc)$ $(I_D = 1.5 \text{ Adc}, T_J = 100^{\circ}\text{C})$ 7.5 Forward Transconductance (V_{DS} = 15 V, I_D = 1.5 A) 1.5 mhos **g**FS DYNAMIC CHARACTERISTICS Input Capacitance Ciss 1000 $(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz})$ **Output Capacitance** 300 Coss See Figure 11 Reverse Transfer Capacitance Crss 80 SWITCHING CHARACTERISTICS* (TJ = 100°C) Turn-On Delay Time td(on) ns $(V_{DD} = 25 \text{ V}, I_{D} = 0.5 \text{ Rated } I_{D}$ Rise Time 100 tr $R_{gen} = 50 \text{ ohms}$ See Figures 9, 13 and 14 Turn-Off Delay Time td(off) 180 Fall Time tf 80 16 (Typ) **Total Gate Charge** Q_{g} 18 nC (VDS = 0.8 Rated VDSS, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12 Gate-Source Charge Qgs 8 (Typ) Gate-Drain Charge Q_{gd} 8 (Typ)

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	(Is = Rated Ip	VSD	1.1 (Typ)	25°C	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited by stray inductance		
Reverse Recovery Time		t _{rr}	165 (Typ)	219 77 14.9	ns

Internal Drain Inductance	Raic	Ld	5 (Typ)	- 938	of mHonal
(Measured from the contact screw on the header closer to the source pin and the center of the die)	AUR		DT .	makimu	Janetian to
Internal Source Inductance		L _S	12.5 (Typ)		
(Measured from the source pin, 0.25" from the package to the source bond pad)			or 5 seconds	l'i from case	раводий цезі Ригрозия, 17

INTERNAL PACKAGE INDUCTANCE (TO-220)

Internal Drain Inductance	Ld			nH
(Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		3.5 (Typ) 4.5 (Typ)	_	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L _S	7.5 (Typ)	_	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

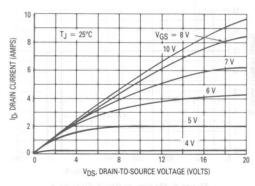


Figure 1. On-Region Characteristics

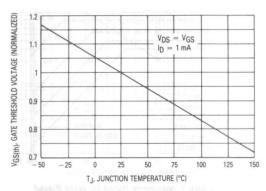


Figure 2. Gate-Threshold Voltage Variation With Temperature

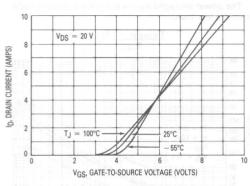


Figure 3. Transfer Characteristics

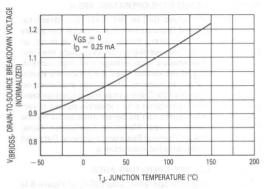


Figure 4. Breakdown Voltage Variation

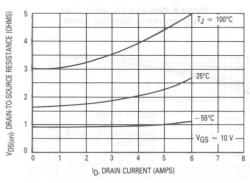


Figure 5. On-Resistance versus Drain Current

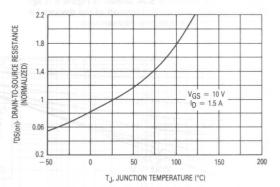


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

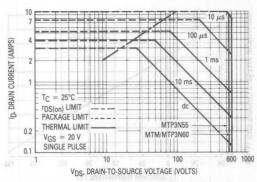


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

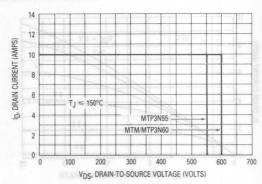


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

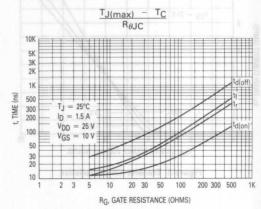


Figure 9. Resistive Switching Time Variation versus Gate Resistance

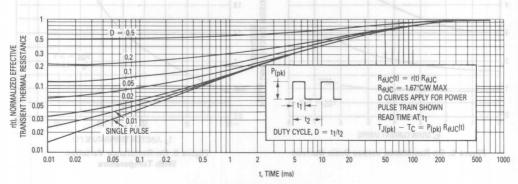


Figure 10. Thermal Response

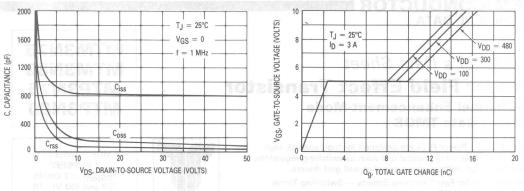


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

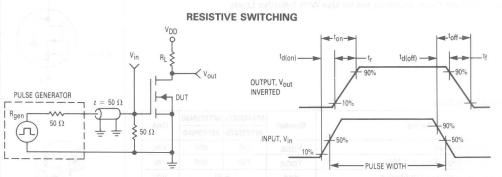
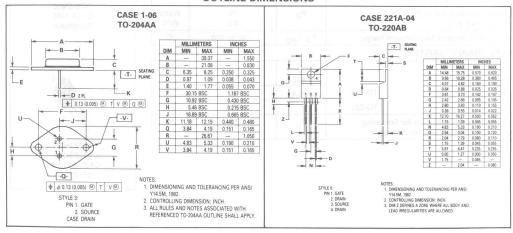


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



3

MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate TMOS

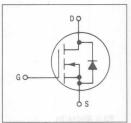
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, high voltage power supplies and grid drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS
3 AMPERES
rDS(on) = 7 OHMS
750 and 800 VOLTS



MAXIMUM RATINGS

Rating	Symbol	MTM3N75 MTP3N75	MTM3N80 MTP3N80	Unit
Drain-Source Voltage	VDSS	750	800	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	750	800	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	3 8 7 0 0		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	- 65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		R_{θ} JC	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta JA}$	30	89 6 2 8
	TO-220		62.5	
Maximum Lead Temperature 1 Purposes, 1/8" from case for		TL	275	°C



MTM3N75 MTM3N80 CASE 1-06 TO-204AA



MTP3N75 MTP3N80 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

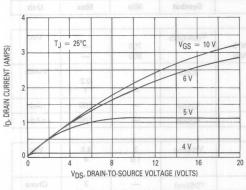
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Chara	cteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)		MTM/MTP3N75 MTM/MTP3N80	V(BR)DSS	750 800	=	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0$) ($V_{DS} = 0.8\ Rated\ V_{DSS},\ V_{GS} = 0$)	0, T _J = 12	5°C)	IDSS		0.2	mAdc
Gate-Body Leakage Current, Forwa	rd (VGSF =	20 Vdc, V _{DS} = 0)	IGSSF	-	100	nAdc
Gate-Body Leakage Current, Revers	e (VGSR =	20 Vdc, V _{DS} = 0)	IGSSR		100	nAdc
ON CHARACTERISTICS*						124
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$ $T_{J} = 100^{\circ}\text{C}$			V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	$V_{GS} = 10$	Vdc, I _D = 1.5 Adc)	rDS(on)		7	Ohms
Drain-Source On-Voltage ($V_{GS} = 1$ ($I_D = 3$ Adc) ($I_D = 1.5$ Adc, $T_J = 100^{\circ}$ C)	0 V)	and a	VDS(on)	Feddon Cho	21 21	Vdc
Forward Transconductance (V _{DS} =	15 V, I _D =	1.5 A)	9FS	0.5	·	mhos
OYNAMIC CHARACTERISTICS			17171			
Input Capacitance	(Vi	ne = 25 V. Vce = 0.	Ciss		1200	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)		Coss	- 1	300	
Reverse Transfer Capacitance		See Figure 11	C _{rss}	\ -	80	
WITCHING CHARACTERISTICS* (TJ	= 100°C)	養養				
Turn-On Delay Time			td(on)	- //	50	ns
Rise Time	(V _{DD} = 125 V, I _D = 0.5 Rated I _D	t _r	_	150		
Turn-Off Delay Time		R _{gen} = 50 ohms) e Figures 9, 13 and 14	td(off)	_	200	1
Fall Time			tf		100	
Total Gate Charge	(V	DS = 0.8 Rated VDSS,	Ωg	35 (Typ)	50	nC
Gate-Source Charge		Rated ID, VGS = 10 V)	Qgs	20 (Typ)	_]
Gate-Drain Charge		See Figure 12	Ωgd	15 (Typ)	CONTES	
OURCE DRAIN DIODE CHARACTERI	STICS*					
Forward On-Voltage	21 07	(I _S = Rated I _D	V _{SD}	1 (Typ)	1.6	Vdc
Forward Turn-On Time		$V_{GS} = 0$	ton	Limited	by stray ind	uctance
Reverse Recovery Time		11	t _{rr}	420 (Typ)		ns
NTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact scree to the source pin and the center		ader closer	Ld	5 (Typ)		nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)			L _S	12.5 (Typ)		
NTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact scree (Measured from the drain lead 0.			L _d	3.5 (Typ) 4.5 (Typ)		nH
Internal Source Inductance (Measured from the source lead	0.25" from _I	package to source bond pad	L _S	7.5 (Typ)	<u> </u>	

^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.







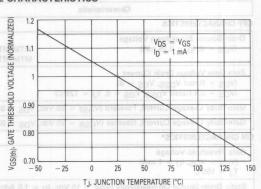
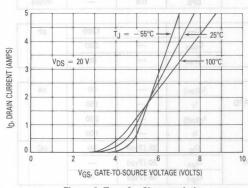


Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



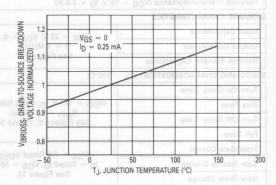
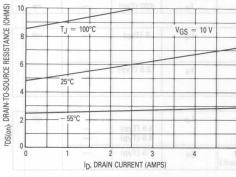


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation With Temperature



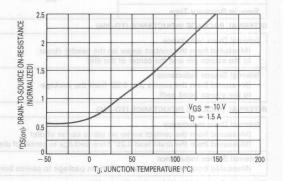


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

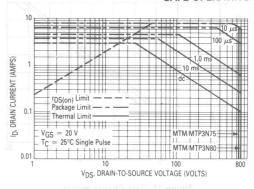


Figure 7. Maximum Rated Forward Biased Safe Operating Area

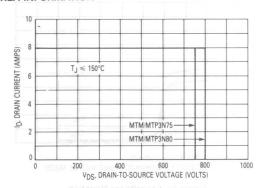


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

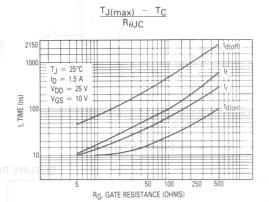


Figure 9. Resistive Switching Time Variation versus Gate Resistance

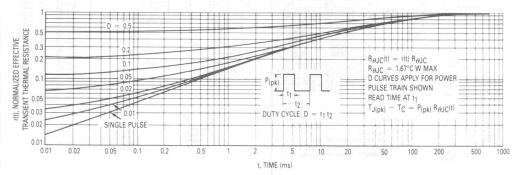


Figure 10. Thermal Response

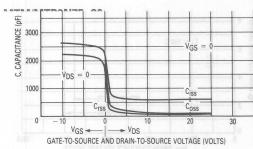


Figure 11. Capacitance Variation

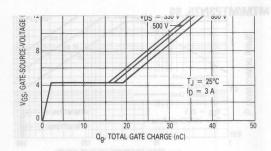


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

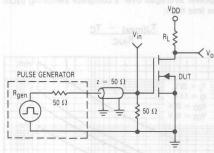


Figure 13. Switching Test Circuit

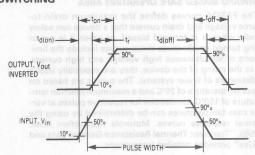
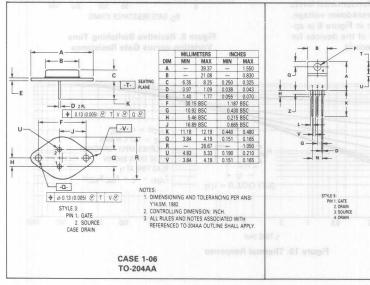
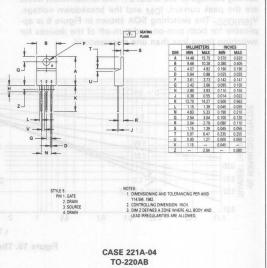


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS





MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement Mode Silicon Gate TMOS

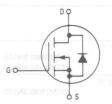
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS 3 and 4 AMPERES rDS(on) = 4 OHMS 850, 900, 950 and 1000 VOLTS





TO-204AA

MAXIMUM RATINGS

Detica	C			11-14		
Rating	Symbol	4N85	4N90	3N95	3N100	Unit
Drain-Source Voltage	V _{DSS}	850	900	950	1000	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	850	900	950	1000 A	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	0 = g _E V V dx = g±20 fartM 1 = 1 ±40			95561	Vdc Vpk
Drain Current Continuous Pulsed	I _D		4	3 16		Adc
Gate Current — Pulsed	IGM	1.5			n	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	gl betse 8 d = gl V 8s 125 gy			Watts W/°C	
Operating and Storage Temperature Range	TJ, Tstg	8 bm	- 65	to 150	nin icu	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	R_{θ} JC	gggV bataR a D = ggV	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	boD to	01 bris 8 arg 1 as 275	°C

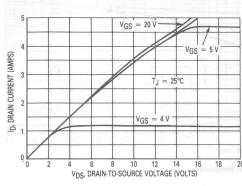
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ELECTRICAL	CHARACTERISTICS	$(T_C = 25^{\circ}C \text{ unless})$	otherwise noted)

Char	acteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS			Sheet	staCl 2	Designer
Drain-Source Breakdown Volta (VGS = 0, I _D = 0.25 mA)	MTM4N85 MTM4N80 MTM3N95 MTM3N100	V(BR)DSS	850 900 950 1000	Field I	Vdc
Zero Gate Voltage Drain Curre (VDS = Rated VDSS, VGS = (VDS = 0.8 Rated VDSS, VG	= 0)	IDSS	designed for h	0.25	mAdc
Gate-Body Leakage Current, F (VGSF = 20 Vdc, VDS = 0)	orward	IGSSF	and relay drive	500	nAdc
Gate Body Leakage Current, R (VGSR = 20 Vdc, VDS = 0)	everse	IGSSR	o - Uncoult	500	nAdc
ON CHARACTERISTICS			erature	Jevated Temp	Specified at 6
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) (T _J = 100°C)	90	VGS(th)	2 1.5	a Power Dis 4 ab	Vdc speu Source-to-Drant Inductive Loa
Static Drain-Source On-Resista (VGS = 10 Vdc, I _D = 1.5 Ad (VGS = 10 Vdc, I _D = 2 Add	dc) MTM3N95/3N100	rDS(on)	=	4 4	Ohm
Drain-Source On-Voltage (VGS = 10 V) (ID = 3 Adc) (ID = 1.5 Adc, TJ = 100°C) (ID = 4 Adc) (ID = 2 Adc, TC = 100°C) MTM3N95/3N100 MTM4N85/4N90		VDS(on)	=	12 10 16 82 14	Vdc MITAR MUMBIA
Forward Transconductance (V _{DS} = 10 V, I _D = 1.5 A) (V _{DS} = 10 V, I _D = 2 A)	MTM3N95/3N100 MTM4N85/4N90	9fs	2 2	Raying	mhos
DYNAMIC CHARACTERISTICS	950 950	sanV			Drain-Grife Voltage
Input Capacitance		C _{iss}		1500	PGS Pq M(I)
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss		150	Gate-Source Volta
Reverse Transfer Capacitance	- WITE	C _{rss}	_9	60	
SWITCHING CHARACTERISTICS	(T _J = 100°C)	MO ₁			Continuous Pulsed
Turn-On Delay Time	6.1	td(on)	_	40	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	tr	_ 50	40	Total Power Dissis Berete sloove 25
Turn-Off Delay Time	$R_{gen} = 50 \text{ ohms}$) See Figs. 8 and 9.	td(off)	ro Range	250	Orersting and Sto
Fall Time		tf	_	75	AGAMA TAMBER
Total Gate Charge	(VDS = 0.8 Rated VDSS,	Qg	55 (typ)	85	nC
Gate-Source Charge	ID = Rated ID, VGS = 10 Vdc)	Qgs	30 (typ)	and to Contain	T beat or invited A
Gate-Drain Charge	See Figs. 6 and 10.	Q _{gd}	25 (typ)	sbriuses 3 n	if éaso mon '8\
SOURCE DRAIN DIODE CHARAC	CTERISTICS				
Forward On-Voltage		V _{SD}	1.1 (typ)	1.5	Vdc
Forward Turn-On Time	(I _S = Rated I _D , V _{GS} = 0) See Figs. 15 and 16.	ton	200 (typ)	_	ns
Reverse Recovery Time		t _{rr}	1000 (typ)		ns

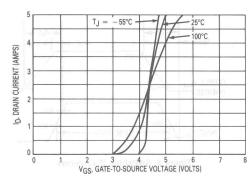
TYPICAL CHARACTERISTICS



1.1 VDS = VGS | ID = 1 mA | ID

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation with Temperature



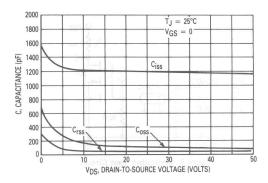
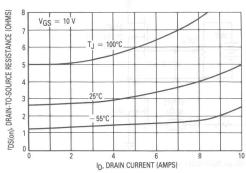


Figure 3. Transfer Characteristics

Figure 4. Capacitance Variation



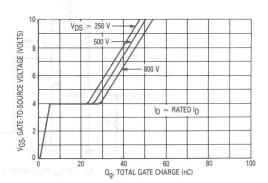


Figure 5. On-Resistance versus 1997 agreed and and of each Drain Current

Figure 6. Gate Charge Variation

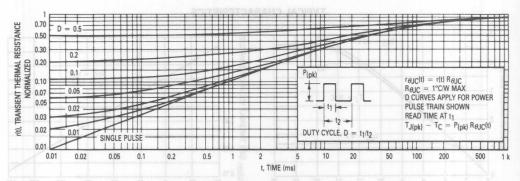


Figure 7. Thermal Response

RESISTIVE SWITCHING

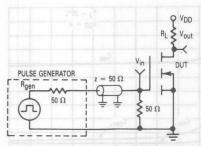


Figure 8. Switching Test Circuit

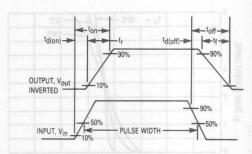
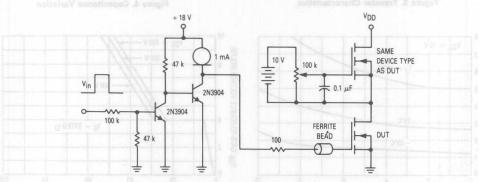


Figure 9. Switching Waveforms



 $V_{in} = 15 V_{pk}$; PULSE WIDTH $\leq 100 \mu s$, DUTY CYCLE $\leq 10\%$

Figure 10. Gate Charge Test Circuit

SAFE OPERATING AREA INFORMATION

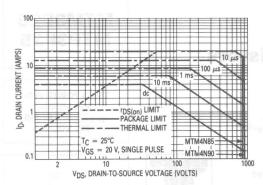


Figure 11. Maximum Rated Forward Biased Safe Operating Area

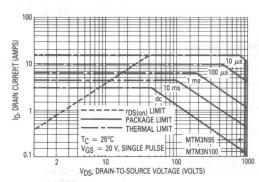


Figure 12. Maximum Rated Forward Biased Safe Operating Area

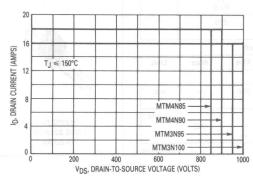


Figure 13. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 11 and 12 are based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D}(25^{\circ}C) \left[\frac{T_{J(max)} - T_{C}}{P_{D} \cdot R_{\theta JC} \cdot r(t)} \right]$$

where

I_D(25°C) = the dc drain current at T_C = 25°C from Figures 11 and 12

T_{J(max)} = rated maximum junction temperature

T_C = device case temperature

PD = rated power dissipation at T_C = 25°C

 $R_{\theta JC}$ = rated steady state thermal resistance

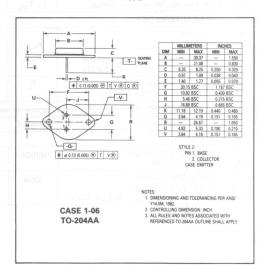
r(t) = normalized thermal response from Figure 7

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 13 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 13 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{\mathsf{T}_{\mathsf{J}(\mathsf{max})} - \mathsf{T}_{\mathsf{C}}}{\mathsf{R}_{\theta}\mathsf{J}\mathsf{C}}$$



Designer's Data Sheet

Power Field Effect Transistors

P-Channel Enhancement-Mode **Silicon Gate TMOS**

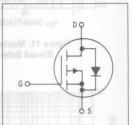
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designers Data IDSS, VDS(on), VGS(th), and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Rayc = rated steady state thermal resistan absol

MTM3P25 MTP3P25

TMOS POWER FETS 3 AMPERES rDS(on) = 4 OHMS 250 VOLTS





MAXIMUM RATINGS

funditive easevery Rating beel ent tant years	Symbol	MTM3P25	MTP3P25	Unit
Drain-Source Voltage MI A SHOOM BOY OF SHORE	VDSS	25	50	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	25	50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	1844-57	20 40	Vdc Vpk
Drain Current — Continuous Pulsed	I _D	i	0	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	7 0		Watts W/°C
Operating and Storage Temperature Range	TJ, T _{sta}	-65 1	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	1 - 2	$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204 TO-220	R_{θ} JA	30 62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Min	Max	Unit
7,		111000	0
V(BR)DSS	250		Vdc
IDSS		0.2	mAdd
	1	V(BR)DSS 250	V(BR)DSS 250 —



CASE 1-04 TO-204AA



MTP3P25 **CASE 221A-04** TO-220AB

3

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristi	С	Symbol	Min	Max	Unit
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	\$1 B V8	IGSSF	V Spv	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	V8 V8	IGSSR		100	nAdc
N CHARACTERISTICS*	D VE		1997		
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C	8H075 VOC	V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 1.5 Adc)		rDS(on)	_	4	Ohms
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 3 \text{ Adc}$) ($I_D = 1.5 \text{ Adc}$, $T_J = 100^{\circ}\text{C}$)	1 10 g	V _{DS(on)}	_	12 10	Vdc
Forward Transconductance (V _{DS} = 10 V, I _D = 1.5 A)		9FS	1	60 L	mhos
YNAMIC CHARACTERISTICS					
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss	_	750	pF
Output Capacitance	f = 1 MHz)	Coss	_	150	
Reverse Transfer Capacitance	See Figure 11	C _{rrs}	- 1	30	
SWITCHING CHARACTERISTICS* (TJ = 100°	C)	125 P/ 0.29-	LT-+		
Turn-On Delay Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms) See Figures 9, 12 and 13	td(on)		30	ns
Rise Time (V		tr		50	
Turn-Off Delay Time		td(off)	_	60	
Fall Time		tf	_	50	
Total Gate Charge	(VDS = 0.8 Rated VDSS,	Qg	10 (Typ)	25	nC
Gate-Source Charge	ID = Rated ID, VGS = 10 V)	Qgs	4 (Typ)		
Gate-Drain Charge	See Figure 12	Q _{gd}	6 (Typ)		
SOURCE DRAIN DIODE CHARACTERISTICS*	65		11/11		
Forward On-Voltage	(I _S = Rated I _D	V _{SD}	4 (Typ)	5	Vdc
Forward Turn-On Time	$V_{GS} = 0$	ton	Limited	by stray inc	luctance
Reverse Recovery Time		t _{rr}	150 (Typ)	1 -5 6 10)	ns
NTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the to the source pin and the center of the d		L _d	5 (Typ)	_	nH
Internal Source Inductance (Measured from the source pin, 0.25" fro to the source bond pad)	0.25" from the package		12.5 (Typ)		
NTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		Ld	3.5 (Typ) 4.5 (Typ)	1=-	nH
Internal Source Inductance (Measured from the source lead 0.25" from	om package to source bond pad.)	L _S	7.5 (Typ)	_	
Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2	0/				

TYPICAL ELECTRICAL CHARACTERISTICS

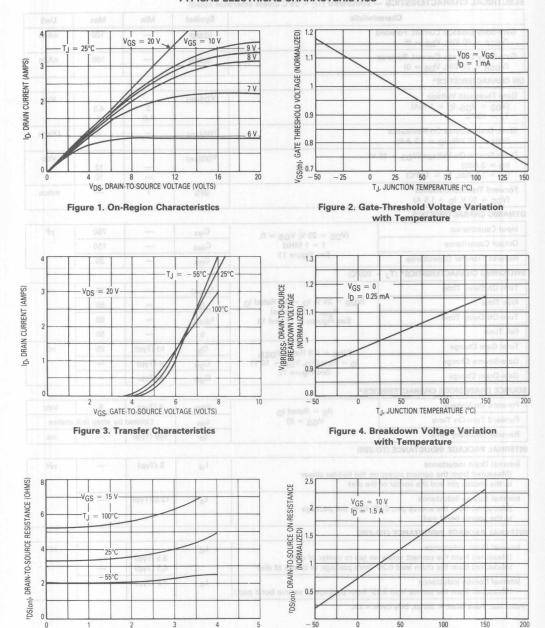


Figure 5. On-Resistance versus Drain Current

ID, DRAIN CURRENT (AMPS)

Figure 6. On-Resistance Variation with Temperature

TJ, JUNCTION TEMPERATURE (°C)

3

SAFE OPERATING AREA INFORMATION

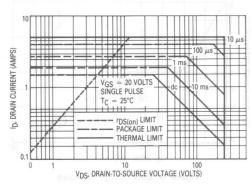


Figure 7. Maximum Rated Forward Bias Safe Operating Area

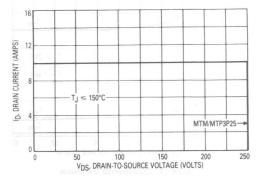


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

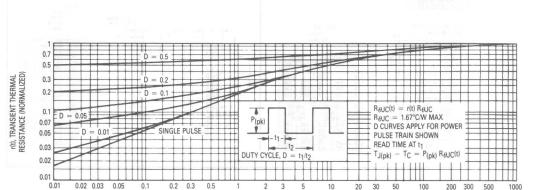
R_G, GATE RESISTANCE (OHMS)

Figure 9. Resistive Switching Time Variation

= 1.5 A

 $V_{DD} = 125 V$

 $V_{GS} = 10 \text{ V}$



t, TIME

t, TIME (ms)

Figure 10. Thermal Response

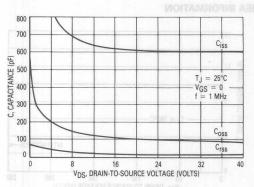


Figure 11. Capacitance Variation

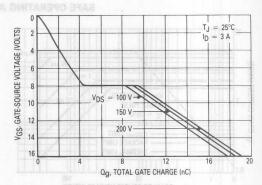


Figure 12. Gate Charge Variation

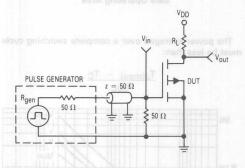


Figure 13. Switching Test Circuit

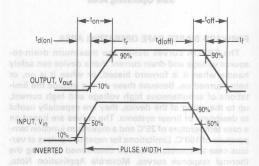
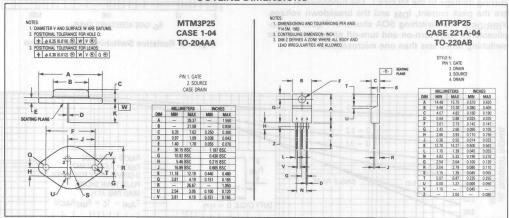


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate TMOS

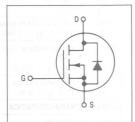
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times
 Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS 4 AMPERES rDS(on) = 1.5 OHMS 450 and 500 VOLTS



MAXIMUM RATINGS

Datin		6804	Comphal	MTM4N45	MTM4N50	Unit	
Rating		Cras	Symbol	MTP4N45	MTP4N50	Unit	
Drain-Source Voltage		VDSS	450	500	Vdc		
Drain-Gate Voltage $(R_{GS} = 1 M\Omega)$		14(00)	V _{DGR}	450	500	Vdc	
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)		V _{GS} V _{GSM}	### ##################################		Vdc Vpk		
Drain Current Continuous Pulsed	27 (Typ) 17 (Typ)	O Sel	I _D	8 Rared VOS	4 = 8aV)	Adc	
Total Power Dissipation @ Derate above 25°C	$T_C = 25^{\circ}C$	hyD	PD		75 .6	Watts W/°C	
Operating and Storage Ten	nperature Rang	ge	T _J , T _{stg}	- 65	to 150	°C	

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204	R _θ JA	30	Naz-01
	TO-220		62.5	d adr no v
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C



MTM4N45 MTM4N50 CASE 1-06 TO-204AA



MTP4N45 MTP4N50 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

	Characteristic	Symbol	Min	Max	Unit	
FF CHARACTERISTICS						
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA) MTM/MTP4N45 MTM/MTP4N50		V(BR)DSS	450 500	er's D	Vdc	
Zero Gate Voltage Drain Curre		IDSS	11 10 10	1011	mAdc	
(VDS = Rated VDSS, VGS = (VDS = 0.8 Rated VDSS, VG	= 0)	bolii-ta	eui e oui	0.2	anad	
Gate-Body Leakage Current, F (VGSF = 20 Vdc, VDS = 0)	orward	IGSSF	2000	100	nAdc	
Gate-Body Leakage Current, R (VGSR = 20 Vdc, VDS = 0)	deverse and a second to get	IGSSR	s are designed	100	nAdc	
N CHARACTERISTICS*			Lesevists yeld	in bine bibit	lios met	
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C	TMOS TMOS	V _{GS(th)}	2 1.5	4.5	Vdc	
Static Drain-Source On-Resista (V _{GS} = 10 Vdc, I _D = 2 Add		rDS(on)	Dissipation haracterized	ewo 1.5	Ohms	
Drain-Source On-Voltage (VGS (ID = 4 Adc) (ID = 2 Adc, TJ = 100°C)	S = 10 V)	V _{DS(on)}	=	7.5 6	Vdc	
Forward Transconductance (V _{DS} = 15 V, I _D = 2 A)		9FS	1.5	- 1	mhos	
YNAMIC CHARACTERISTICS						
Input Capacitance		Ciss	_	1200	pF	
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss		300	OT BUCK	
Reverse Transfer Capacitance		C _{rss}	- 0	80		
WITCHING CHARACTERISTICS	* (T _J = 100°C)					
Turn-On Delay Time	90 000 000 800	td(on)		50	ns	
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	tr	_	100	ov sisum	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	awo unin	200	Source V	
Fall Time	Voew ±40 V/k	tf	n-rep <u>eti</u> tive (i	100		
Total Gate Charge	(Vp 0.9 Poted Vp	Qq	27 (Typ)	32	nC	
Gate-Source Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V)	Qgs	17 (Typ)		lsed	
Gate-Drain Charge	See Figure 12	Q _{qd}	10 (Typ)	5) notrocisa	Power D	
OURCE DRAIN DIODE CHARAC	CTERISTICS*			3 25°C	vode state	
Forward On-Voltage	Us - Peted Is	V _{SD}	1.1 (Typ)	1.4	Vdc	
Forward Turn-On Time	$V_{GS} = Rated I_{D}$	ton	Limited by stra		v inductance	
Reverse Recovery Time	WO	t _{rr}	210 (Typ)	_ L_eons	ns	
NTERNAL PACKAGE INDUCTAN	NCE (TO-204)			0000	01 110 121	
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L _d oss	5 (Typ)	utsragmeT t	nH	
Internal Source Inductance (Measured from the source to the source bond pad)		L _S	12.5 (Typ)	esao moni '8	rposes, 1	
NTERNAL PACKAGE INDUCTAN	NCE (TO-220)			1196		
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L _d	3.5 (Typ) 4.5 (Typ)	_	nH	
			, , , , , , ,			

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

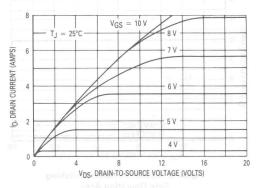


Figure 1. On-Region Characteristics

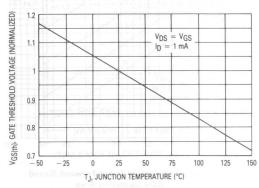


Figure 2. Gate-Threshold Voltage Variation With Temperature

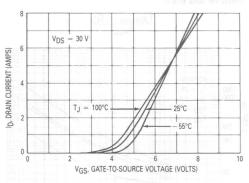


Figure 3. Transfer Characteristics

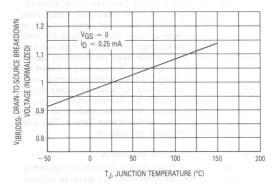


Figure 4. Breakdown Voltage Variation
With Temperature

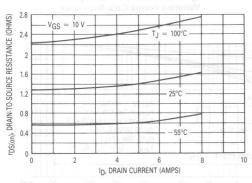


Figure 5. On-Resistance versus Drain Current

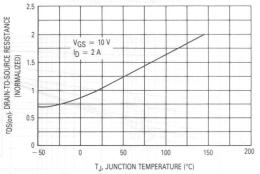


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

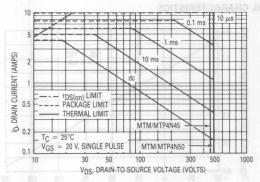


Figure 7. Maximum Rated Forward Biased Safe Operating Area

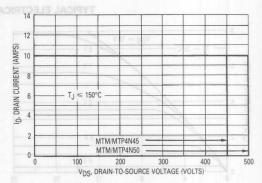


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

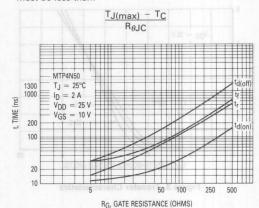


Figure 9. Resistive Switching Time Variation versus Gate Resistance

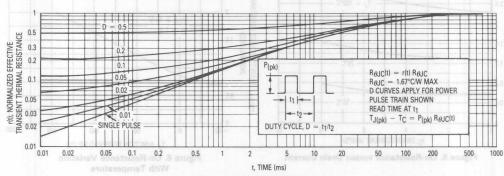
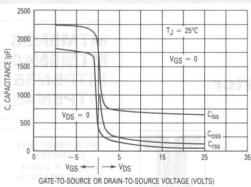


Figure 10. Thermal Response



16 /OLTAGE (VOLTS) 14 360 V T_J = 25°C 12 ID = 4 A 10 225 V GATE SOURCE \ = 150 V VGS, 10 30 Q_q, TOTAL GATE CHARGE (nC)

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING VDD tofftd(off) OUTPUT, V_{out} INVERTED INPUT, Vin

Figure 13. Switching Test Circuit

 $z = 50 \Omega$

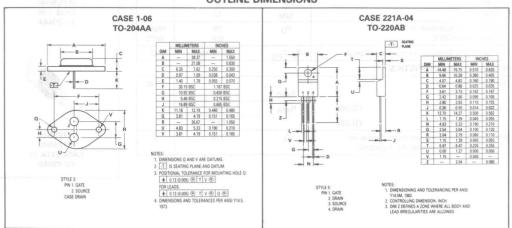
€ 50 Ω

PULSE GENERATOR

50 Ω

PULSE WIDTH Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

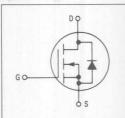
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS
5 AMPERES
rDS(on) = 1 OHM
350 and 400 VOLTS



MAXIMUM RATINGS

Rating	Symbol	MTM5N35 MTP5N35	MTM5N40 MTP5N40	Unit
Drain-Source Voltage	VDSS	350	400	Vdc
Drain-Gate Voltage (RGS = 1 MΩ)	VDGR	350	400	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}		20 40	Vdc Vpk
Drain Current Continuous Pulsed	I _D	1 a 3 WILT	5 2	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		.6	Watts W/°C
Operating and Storage Temperature Range	TJ, Tstg	- 65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta JA}$	30	
	TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C



MTM5N35 MTM5N40 CASE 1-06 TO-204AA



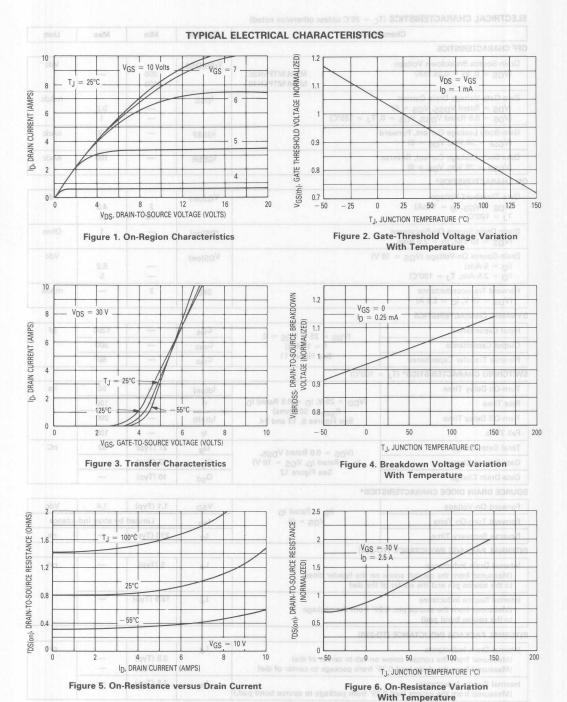
MTP5N35 MTP5N40 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Charac	teristic - DAHAHO MADIN DEL	Symbol	Min	Max	Unit
FF CHARACTERISTICS		-			
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	MTM/MTP5N35 MTM/MTP5N40	V(BR)DSS	350 400	Ξ	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0$) ($V_{DS} = 0.8\ Rated\ V_{DSS},\ V_{GS} = 0$,	T _J = 125°C)	IDSS		0.2	mAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	an ŝ	IGSSF	_	100	nAdc
Gate-Body Leakage Current, Reverse $(V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0)$	0.8	IGSSR	_	100	nAdc
N CHARACTERISTICS*					
Gate Threshold Voltage $(V_DS = V_GS, I_D = 1 \text{ mA})$ $T_J = 100^{\circ}C$		VGS(th)	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 2.5 Adc)	Figure 2. C	rDS(on)	and gelland	I J entipid	Ohm
	V)	V _{DS(on)}	_	6.2 5	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 2.5 A)	1,2	9FS	2	_	mhos
YNAMIC CHARACTERISTICS	0 = 01	W			
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz})$	Ciss	-	1200	pF
Output Capacitance		Coss	\ - \	300	
Reverse Transfer Capacitance	See Figure 11	C _{rss}	\(-	80	
SWITCHING CHARACTERISTICS* (TJ =	100°C)		1		
Turn-On Delay Time		td(on)		50	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	tr	1/2	100	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	-75	200	
Fall Time	0 68 - 00	8 t _f	_	100	
Total Gate Charge	$(V_{DS} = 0.8 \text{ Rated } V_{DSS},$	Q_g	27 (Typ)	32	nC
Gate-Source Charge	I_D = Rated I_D , V_{GS} = 10 V)	Q_{gs}	17 (Typ)	\$ 8 10 96	
Gate-Drain Charge	See Figure 12	Q _{gd}	10 (Typ)	_	
OURCE DRAIN DIODE CHARACTERIS	TICS*				
Forward On-Voltage	(I _S = Rated I _D	V _{SD}	1.1 (Typ)	1.4	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	uctance
Reverse Recovery Time	2	t _{rr}	210 (Typ)	_	ns
NTERNAL PACKAGE INDUCTANCE (TO)-204)				
Internal Drain Inductance (Measured from the contact screw to the source pin and the center of		Ld	5 (Typ)	-	nH
Internal Source Inductance (Measured from the source pin, 0.2 to the source bond pad)	5" from the package	L _S	12.5 (Typ)	_	
NTERNAL PACKAGE INDUCTANCE (TO)-220)				
(Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L _d	3.5 (Typ) 4.5 (Typ)	_	nH
Internal Source Inductance (Measured from the source lead 0.3	urent Rours D	Ls	7.5 (Typ)	nO Trans	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.



3

SAFE OPERATING AREA INFORMATION

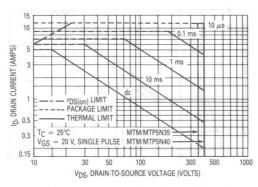


Figure 7. Maximum Rated Forward Biased Safe Operating Area

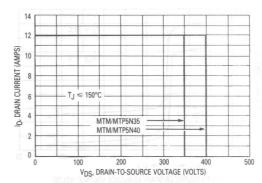


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

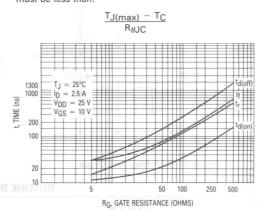


Figure 9. Resistive Switching Time Variation versus Gate Resistance

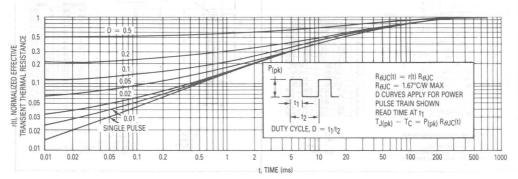


Figure 10. Thermal Response

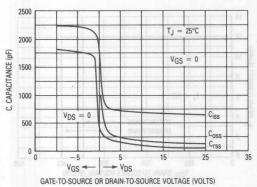
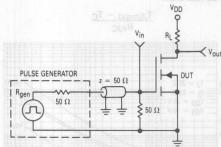


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus
Gate-to-Source Voltage

RESISTIVE SWITCHING



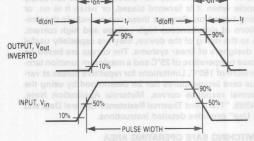
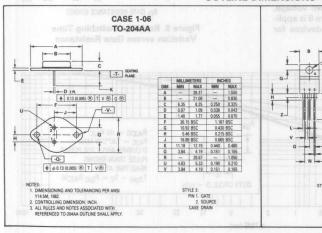
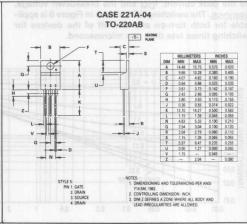


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS





MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

P-Channel Enhancement-Mode Silicon Gate TMOS

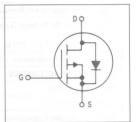
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MTM5P18 MTM5P20 MTP5P18 MTP5P20



TMOS POWER FETS
5 AMPERES
rDS(on) = 1 OHM
180 and 200 VOLTS



MAXIMUM RATINGS

Pating	Complete	MTM	I I - ia	
Rating	Symbol	5P18	5P20	Unit
Drain-Source Voltage	V _{DSS}	180	200	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	V _{DGR}	180	200	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}		20 40	Vdc Vpk
Drain Current Continuous Pulsed	I _D	5 20		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta JA}$	30	(O-220)
	TO-220		62.5	
Maximum Lead Temperature f Purposes, 1/8" from case for		TL (sib	275	°C



MTM5P18 MTM5P20 CASE 1-04 TO-204AA



MTP5P18 MTP5P20 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Char	acteristic			Symbol	Min	Max	Unit
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA)		MTM/MTF		V(BR)DSS	180 200	r's Da Fhalu	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = Rated\ V_{DSS}, V_{GS} = 0$) ($V_{DS} = Rated\ V_{DSS}, V_{GS} = 0$,	TJ = 125°0	c)	-	IDSS	nceme OS-	10 100	μAdc
Gate-Body Leakage Current, Forwa	rd (VGSF	$= 20 \text{ Vdc, V}_{DS} = 0)$		IGSSF	_	100	nAdc
Gate-Body Leakage Current, Rever	se (VGSR	$=$ 20 Vdc, $V_{DS} = 0$)	m voltag	IGSSR	are <u>de</u> sign	100	nAdc
ON CHARACTERISTICS*					to valer bas		
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) T.j = 100°C					2 1.5	4.5	Vdc
Static Drain-Source On-Resistance	(VGS = 10	Vdc, I _D = 2.5 Adc)		rDS(on)	9	Temperatu	Ohm
Drain-Source On-Voltage (VGS = 10 V) (ID = 5 Adc) (ID = 2.5 Adc, TJ = 100°C)				V _{DS(on)}	Dissipation aractorized	Pewo9 al Al O eb 5 Cl ni 4	Vdc
Forward Transconductance (VDS =	15 V, I _D	= 2.5 A)		9FS	2	_	mhos
DYNAMIC CHARACTERISTICS					. 12 - 1		
Input Capacitance	(V====25 V V====0			Ciss	-	1000	pF
Output Capacitance	'	$V_{DS} = 25 \text{ V, } V_{GS} = 0,$ f = 1 MHz)			_	250	
Reverse Transfer Capacitance		See Figure 10		C _{oss}	_	75	
SWITCHING CHARACTERISTICS* (T.	= 100°C)					SEMI	An WU
Turn-On Delay Time	dinU -	Inti STM to NITM		td(on)	-	40	ns
Rise Time	(VDD	= 25 V, ID = 0.5 Ra	ted ID	tr		50	V sasue8
Turn-Off Delay Time	ibV	R _{gen} = 50 ohms) See Figures 11 and 1	2 880	td(off)	_	90	
Fall Time	lbV		ABOA	tf	_	60	Gata Volt
SOURCE DRAIN DIODE CHARACTER	ISTICS*	DC +	Voe		emouni	Hann Cont	oV amună
Forward On-Voltage	IgV	(Is = Rated ID	Мару	V _{SD}	2 (Typ)	поИ -4	Vdc
Forward Turn-On Time	abA	$V_{GS} = 0$		ton	Limited	by stray ind	uctance
Reverse Recovery Time		20	l D	t _{rr}	(Typ)		ns
NTERNAL PACKAGE INDUCTANCE	TO-204)	35	23		c = 28°C	singtion (6) T	Power Dis
Internal Drain Inductance (Measured from the contact scre to the source pin and the center		eader closer	gtaT st.	L _d	5 (Typ)	25°C— Storage Tem	He beet
Internal Source Inductance (Measured from the source pin, to the source bond pad)	0.25" from	the package	Raje	L _S	12.5 (Typ)	DACTERIST DOC 200	IAL CHA rel Resist ction to C
NTERNAL PACKAGE INDUCTANCE	TO-220)	30	ALIA	80%	OT	meidm	A of noise
Internal Drain Inductance (Measured from the contact scre (Measured from the drain lead 0				L _d oss	3.5 (Typ) 4.5 (Typ)	Temperatuo	nH um Leac
Internal Source Inductance (Measured from the source lead	0.25" from	package to source be	ond pad.)	L _S	7.5 (Typ)	- Hann mov	Doses, 1/2

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

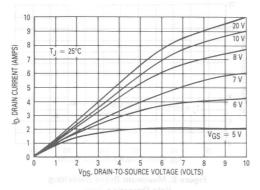


Figure 1. On-Region Characteristics

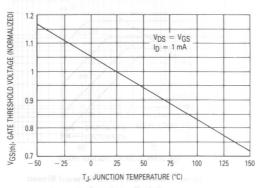


Figure 2. Gate-Threshold Voltage Variation With Temperature

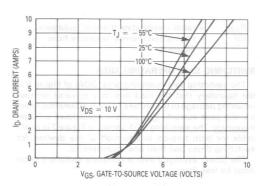


Figure 3. Transfer Characteristics

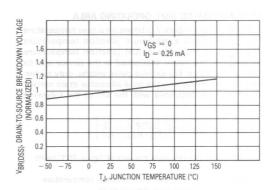


Figure 4. Normalized Breakdown Voltage versus Temperature

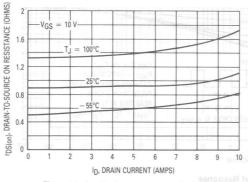


Figure 5. On-Resistance versus Drain Current

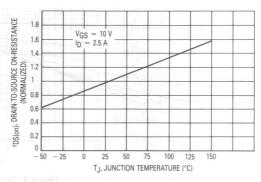


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

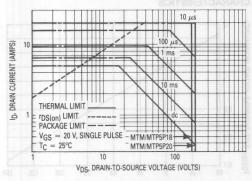


Figure 7. Maximum Rated Forward Biased Safe Operating Area

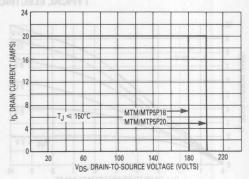


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 7 is based on a case temperature (T_C) of 25°C and a maximum junction temperature ($T_{J(max)}$) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D}(25^{\circ}C) \left[\frac{T_{J}(max) - T_{C}}{P_{D} \cdot R_{\theta J}C \cdot r(t)} \right]$$

where

 $I_D(25^{\circ}C)$ = the dc drain current at T_C = 25°C from

Figure 6.

TJ(max) = rated maximum junction temperature.

T_C = device case temperature. P_D = rated power dissipation at T_C = 25°C. $\begin{array}{ll} R_{\mbox{\it BJC}} & = \mbox{rated steady state thermal resistance.} \\ r(t) & = \mbox{normalized thermal response from} \\ & Figure 9. \end{array}$

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 7 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

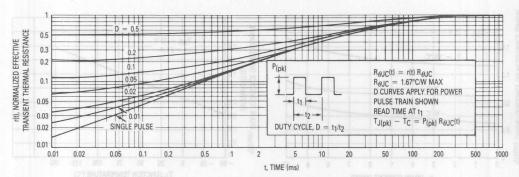


Figure 9. Thermal Response

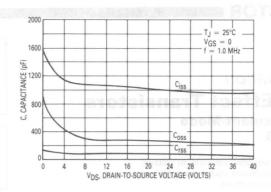


Figure 10. Capacitance Variation

RESISTIVE SWITCHING

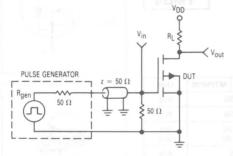


Figure 11. Switching Test Circuit

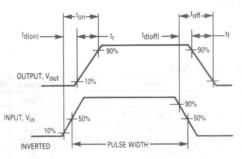
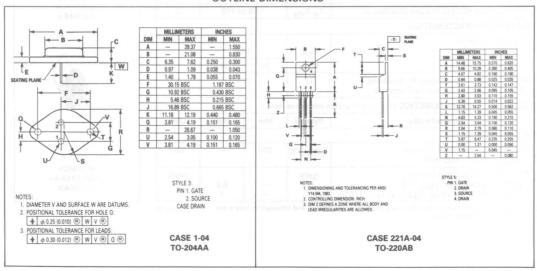


Figure 12. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Advance Information

Power Field Effect Transistors

P-Channel Enhancement-Mode Silicon Gate TMOS

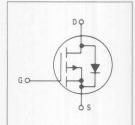
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and motor drives.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designers Data I_{DSS}, V_{DS(on)}, V_{GS(th)}, and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive
 Loads



MTM5P25 MTP5P25

TMOS POWER FETS
5 AMPERES
rDS(on) = 3 OHMS
250 VOLTS



MAXIMUM RATINGS

Rating	Symbol	MTM5P25	MTP5P25	Unit
Drain-Source Voltage	V _{DSS}	250		Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	250		Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	I _D		5	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD BNOISE		5 .6)TUO	Watts W/°C
Operating and Storage Temperature Range	TJ, Tsta	-65 1	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{ heta}$ JC	1	1.67	
Junction to Ambient	$R_{\theta}JA$	30	62.5	651 (83
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	der land		0010 0010	254 1.05
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA)	V _{(BR)DSS}	250	80.0. 1 10.0	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0, TJ = 125°C)	IDSS	=	0.2	mAdc

This document contains information on a new product. Specifications and information herein are subject to change without notice. (continued)



MTM5P25 CASE 1-04 TO-204AA



MTP5P25 CASE 221A-04 TO-220AB

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)			Symbol	Min	Max	Unit	
			IGS		IGSSF —		nAdc
Gate-Body Leakage Current, Reve (VGSR = 20 Vdc, VDS = 0)	erse	11 2	VE	IGSSR	v M	100	nAdc
N CHARACTERISTICS*		/ L. §			X.		-
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = 1 \text{ mA})$ $T_J = 100^{\circ}\text{C}$		10 A C A C A C A C A C A C A C A C A C A	_V.8 -	V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 2.5 Adc)	е	- 181 Q		rDS(on)		3	Ohms
Drain-Source On-Voltage ($V_{GS} = (I_D = 5 \text{ Adc})$ ($I_D = 2.5 \text{ Adc}$, $T_J = 100^{\circ}\text{C}$)	10 V)		VET	V _{DS(on)}		16 15	Vdc
Forward Transconductance (V _{DS} = 10 V, I _D = 2.5 A)		or o e		9FS	1		mhos
YNAMIC CHARACTERISTICS	TOWN 1		- V	ZIJŠV. BRA	SION CHINE IT	. 140>	
Input Capacitance	ure 2 Gate-TI	Figure 2 Sator		Ciss	mad Taninas	1600	pF
Output Capacitance	(V _{DS}	$= 25 \text{ V, V}_{GS} = 0,$ f = 1 MHz)		Coss	_	400	
Reverse Transfer Capacitance	S	ee Figure 14		C _{rss}	-	250	
WITCHING CHARACTERISTICS* (7	Γ _J = 100°C)	1 1 3					
Turn-On Delay Time	Art 20 0 m	3		td(on)		40	ns
Rise Time		25 V, ID = 0.5 Rated	D 00	tr	-	70	
Turn-Off Delay Time		gures 11, 12 and 13		td(off)	_	90	
Fall Time				tf	_	60	1
Total Gate Charge	(Vpc	= 0.8 Rated V _{DSS} ,		Qg	15 (Typ)	30	nC
Gate-Source Charge	$I_D = Ra$	ated ID, VGS = 10 V		Qgs	5 (Typ)	_	
Gate-Drain Charge		See Figure 10		Q_{gd}	10 (Typ)		
OURCE DRAIN DIODE CHARACTE	RISTICS*				-		
Forward On-Voltage		Is = Rated In		V _{SD}	3 (Typ)	5	Vdc
		$(I_S = Rated I_D V_{GS} = 0)$					

^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

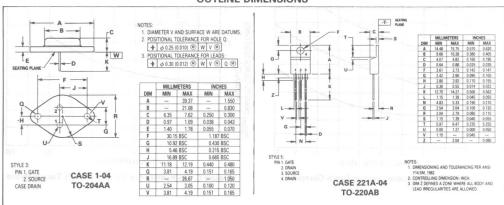
Reverse Recovery Time

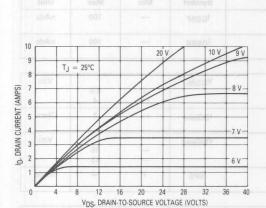
OUTLINE DIMENSIONS

trr

200 (Typ)

ns





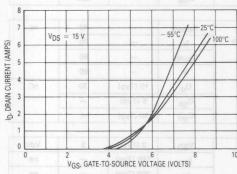
GATE THRESHOLD VOLTAGE (NORMALIZED) $V_{DS} = V_{GS}$ $I_{D} = 1 \text{ mA}$ 0.90 0.80 VGS(th) 0.70

Figure 1. On-Region Characteristics

T.J. JUNCTION TEMPERATURE (°C) Figure 2. Gate-Threshold Voltage Variation With Temperature

50

25



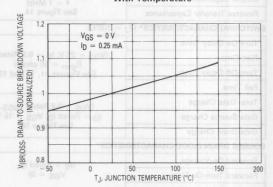
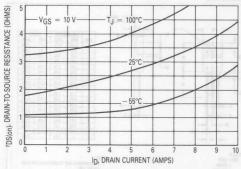


Figure 3. Transfer Characteristics

Figure 4. Drain-To-Source Breakdown Voltage Variation With Temperature



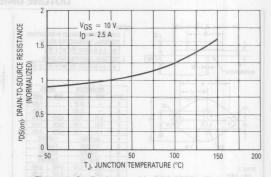


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

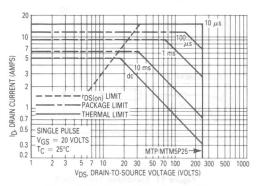


Figure 7. Maximum Rated Forward Bias Safe Operating Area

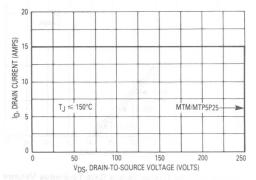


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

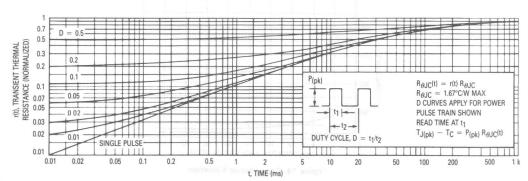


Figure 9. Thermal Response

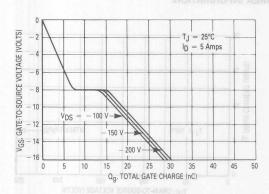


Figure 10. Gate Charge versus Gate-To-Source Voltage

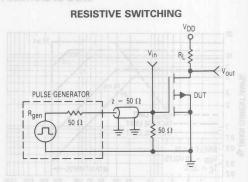


Figure 11. Switching Test Circuit

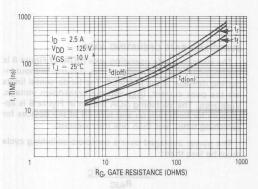


Figure 12. Resistive Switching versus Gate Resistance

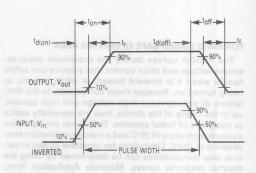


Figure 13. Switching Waveforms

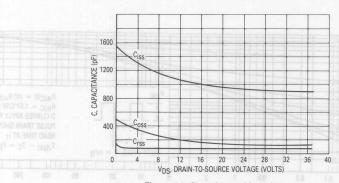


Figure 14. Capacitance Variation

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

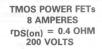
Power Field Effect Transistor

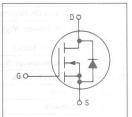
N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads







MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	VDSS	200	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	(emido 200	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu$	VGS	± 40 ± 13 and 1 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	8 gagV bars 25t.0 = agV	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance	palloury tio			°C/W
Junction to Case	(ey) 325 (yg)	$R_{\theta}JC$	1.67	
Junction to Ambient	TO-204	$R_{\theta JA}$	30	-204}
	TO-220		62.5	
Maximum Lead Temperatur Purposes, 1/8" from case		TL	275	°C



MTM8N20 CASE 1-04 TO-204AA



MTP8N20 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Characteristic			Min	Max	Unit
OFF CHARACTERISTICS					THE THE
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA) MTM/MTP8N20			200	's Da	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0,	Г _Ј = 125°C)	IDSS	et <u>l</u> a	10 100	μAdc
Gate-Body Leakage Current, Forwa	rd (VGSF = 20 Vdc, VDS = 0)	IGSSF	- 200	100	nAdc
Gate-Body Leakage Current, Revers	se (VGSR = 20 Vdc, VDS = 0)	IGSSR	_	100	nAdc
ON CHARACTERISTICS*	voltage, January	for medium	are designed	ower FETs	ia TMOS Ri
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C	SOMT Pear Being	V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	(V _{GS} = 10 Vdc, I _D = 4 Adc)	rDS(on)	and a second	0.4	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 8 Adc) (I _D = 4 Adc, T _J = 100°C)			Dissipation I	4 3.6	be Vdc
Forward Transconductance (VDS =	9FS	3	_	mhos	
DYNAMIC CHARACTERISTICS					
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss		800	pF
Output Capacitance	f = 1 MHz)	Coss	_	300	
Reverse Transfer Capacitance	See Figure 11	C _{rss}		100	TAS MUN
SWITCHING CHARACTERISTICS* (T.	= 100°C)	a l		neltes	
Turn-On Delay Time	Vince 200 Vdc	td(on)	_	40	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r	(Oto	150	utloV etsD-n
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	apoun	200	loV equipo2-rol
Fall Time	SSM ±40 Vok	(t _f 08 =	gt) s <u>wi</u> ftegar	100	
Total Gate Charge	lo 8 Ado	Q_g	15 (Typ)	30	nC
Gate-Source Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V)	Qgs	8 (Typ)	District	
Gate-Drain Charge	The state of the s	Q _{gd}	7 (Typ)	Distriction on 10	Power Bist
SOURCE DRAIN DIODE CHARACTER	ISTICS*	a	sona9 muters	omeT some	ation and St
Forward On-Voltage	(IS = Rated ID	V _{SD}	1 (Typ)	2.5	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	luctance
Reverse Recovery Time	8JC 1.87	t _{rr}	325 (Typ)	- 52	ns
NTERNAL PACKAGE INDUCTANCE	TO-204) 08 Atm	8 40	10-2	Trieidi	nction to An
Internal Drain Inductance (Measured from the contact scre to the source pin and the center		L _d 653	5 (Typ)	emperature	nH baaJ mumi
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)			12.5 (Typ)		
NTERNAL PACKAGE INDUCTANCE	TO-220)	ATTACK TO			
Internal Drain Inductance (Measured from the contact scre (Measured from the drain lead 0	w on tab to center of die) .25" from package to center of die)	Ld	3.5 (Typ) 4.5 (Typ)	-	nH
Internal Source Inductance	0.25" from package to source bond pad.)	L _S	7.5 (Typ)	_	

*Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

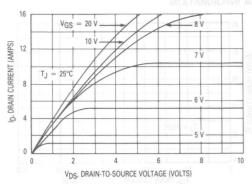


Figure 1. On-Region Characteristics

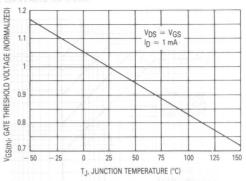


Figure 2. Gate-Threshold Voltage Variation
With Temperature

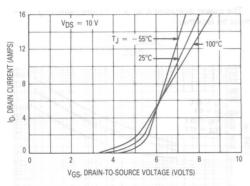


Figure 3. Transfer Characteristics

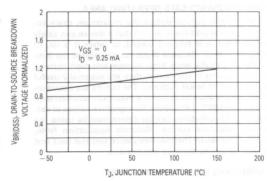


Figure 4. Breakdown Voltage Variation With Temperature

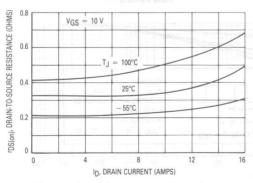


Figure 5. On-Resistance versus Drain Current

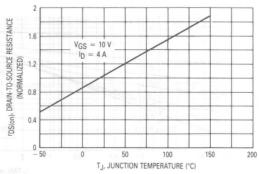


Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

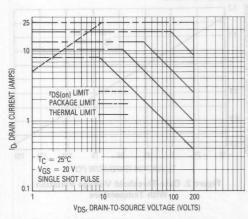


Figure 7. Maximum Rated Forward Biased Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

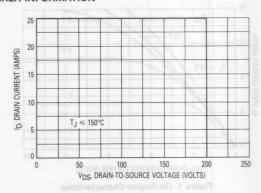


Figure 8. Maximum Rated Switching Safe Operating Area

The power averaged over a complete switching cycle must be less than:

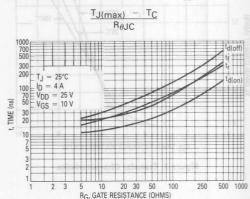


Figure 9. Resistive Switching Time versus Gate Resistance

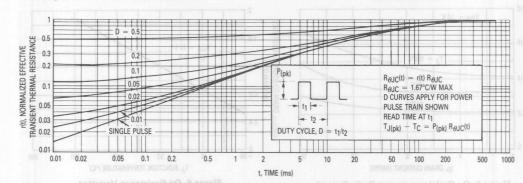


Figure 10. Thermal Response

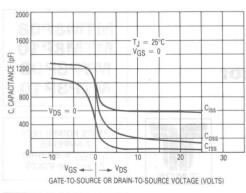


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

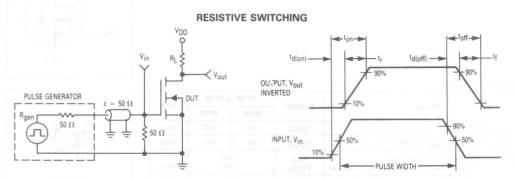
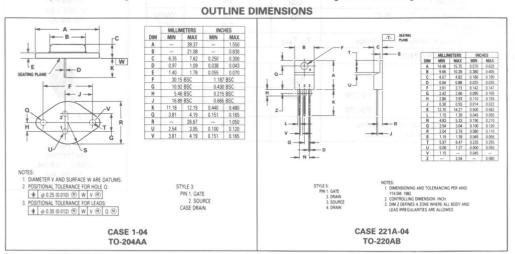


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms



Power Field Effect Transistor

P-Channel Enhancement-Mode Silicon Gate TMOS

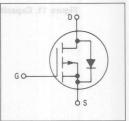
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS 8 AMPERES rDS(on) = 0.4 OHM 80 and 100 VOLTS



MAXIMUM RATINGS

3

Poster and	Combal	MTM	11-14	
Rating	Symbol	8P08	8P10	Unit
Drain-Source Voltage	V _{DSS}	80	100	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	8 25		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		R_{θ} JC	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta}JA$	30	
	TO-220	111 6	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C



MTM8P08 MTM8P10 CASE 1-04 TO-204AA



MTP8P08 MTP8P10 CASE 221A-04 TO-220AB

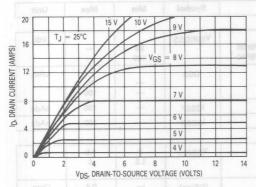
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Max	Unit
OFF CHARACTERISTICS		THE SECOND	Vel	10 /4		
Drain-Source Breakdown Voltage $(V_{GS} = 0, I_D = 0.25 \text{ mA})$		MTM/MTP8P08 MTM/MTP8P10	V _{(BR)DSS}	80 100	=	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, T	J = 125°C)		IDSS		10 100	μAdc
Gate-Body Leakage Current, Forward (V _{GSF} = 20 Vdc, V _{DS} = 0)			IGSSF	-	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)			IGSSR		100	nAdc
ON CHARACTERISTICS*		10	1/2			
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C			VGS(th)	1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 4 Adc)			rDS(on)	_	0.4	Ohm
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 8 \text{ Adc}$) ($I_D = 4 \text{ Adc}$, $T_J = 100^{\circ}\text{C}$)			V _{DS(on)}	HAU ANTHON	4.8 3	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 4 A)			gFS	2	_	mhos
DYNAMIC CHARACTERISTICS			TITUT			
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 11		C _{iss}		1200	pF
Output Capacitance			Coss	_	600	
Reverse Transfer Capacitance			C _{rss}	-	180	
WITCHING CHARACTERISTICS* (TJ	= 100°C)	63 %		4		
Turn-On Delay Time		5.5	td(on)	7/-	80	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms) See Figures 9, 13 and 14		t _r	77.	150	
Turn-Off Delay Time			td(off)	7	200	
Fall Time			tf		150	1
Total Gate Charge		0 4	Q_g	33 (Typ)	50	nC
Gate-Source Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V)		Qgs	16 (Typ)	-	
Gate-Drain Charge	- ID - Hated I	D, vGS = 10 v/	Q _{gd}	17 (Typ)	_	
OURCE DRAIN DIODE CHARACTERIS	STICS*		goilteirean	anther Charge	ar content	d
Forward On-Voltage	(I _S = Rated I _D V _{GS} = 0)		V _{SD}	3 (Typ)	6	Vdc
Forward Turn-On Time			ton	Limited	by stray ind	uctance
Reverse Recovery Time			t _{rr}	300 (Typ)	_	ns
NTERNAL PACKAGE INDUCTANCE (ГО-204)	8				
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		Ld	5 (Typ)	-	nH	
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L _S	12.5 (Typ)			
NTERNAL PACKAGE INDUCTANCE (1	ГО-220)	-				
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die) Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)			L _d	3.5 (Typ) 4.5 (Typ)	=	nH
			L _S	7.5 (Typ)		

3

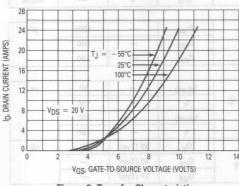
TYPICAL ELECTRICAL CHARACTERISTICS TO SOLITABILITY OF THE PROPERTY OF THE PROP



GATE THRESHOLD VOLTAGE (NORMALIZED) $V_{DS} = V_{GS}$ $I_{D} = 1 \text{ mA}$ 1.1 0.9 0.8 0.7 25 50 75 100 125 -50-25TJ, JUNCTION TEMPERATURE (°C)

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation With Temperature



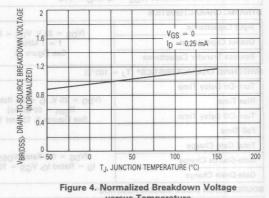
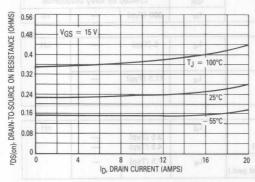


Figure 3. Transfer Characteristics

Figure 4. Normalized Breakdown Voltage versus Temperature



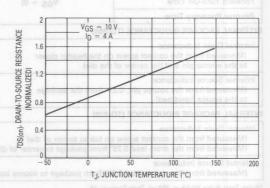


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

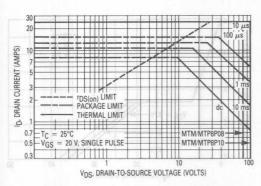


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

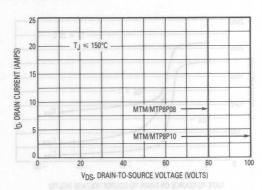


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

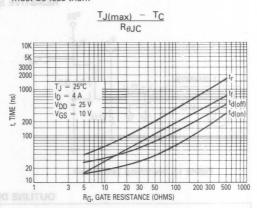
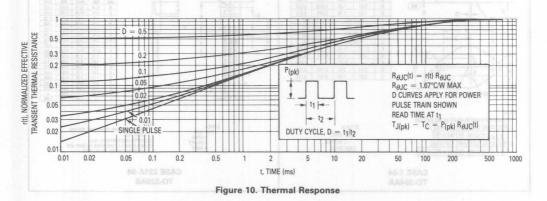
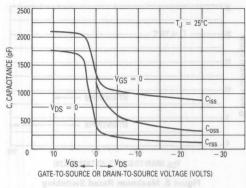


Figure 9. Resistive Switching Time Variation versus Gate Resistance



MOTOROLA TMOS POWER MOSFET DATA



MTP8P10 V_{GS}, GATE SOURCE VOLTAGE (VOLTS) $T_J = 25^{\circ}C$ $-I_D = 8 A$ $V_{DS} = 30 V$ - 12 80 V 20 40 50 Qg, TOTAL GATE CHARGE (nC)

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus **Gate-to-Source Voltage**

RESISTIVE SWITCHING

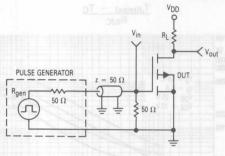


Figure 13. Switching Test Circuit

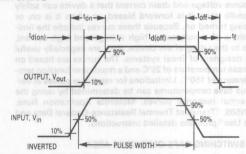
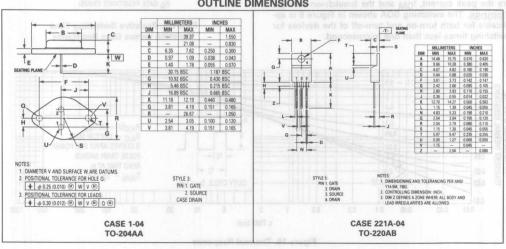


Figure 14. Switching Waveforms



MOTOROLA ■ SEMICONDUCTOR **TECHNICAL DATA**

Advance Information

Power Field Effect Transistors

P-Channel Enhancement-Mode Silicon Gate TMOS

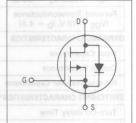
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and motor drives.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designers Data IDSS, VDS(on), VGS(th), and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive



TMOS POWER FETS 8 AMPERES rDS(on) = 2 OHMS 250 VOLTS

MTM8P25



MAXIMUM RATINGS

Rating	Symbol	MTM8P25	MTP8P25	Unit
Drain-Source Voltage	VDSS	25	50	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)		250		Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)		± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	8 24		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	7 0.	wer and	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 t	o 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	R_{θ} JC	R _θ JC 1.67		°C/W
Junction to Ambient	$R_{\theta}JA$	30	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
DFF CHARACTERISTICS				R.E.
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA)	V(BR)DSS	250	100.0	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0, TJ = 125°C)	IDSS		0.2	mAdc

(continued)





CASE 221A-04 TO-220AB

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		IGSSF	-	100	nAdc
Gate-Body Leakage Current, Rever (VGSR = 20 Vdc, VDS = 0)	se	IGSSR	NITEMIN	100	nAdc
N CHARACTERISTICS*	STOJSISHET	1 306	TEN L	HOLL.	ISALO
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C		VGS(th)	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 4 Adc)	m voltage,	rDS(on)	are design	Power FETI	Ohms
Drain-Source On-Voltage ($V_{GS} = (I_D = 8 \text{ Adc})$ ($I_D = 4 \text{ Adc}$, $T_J = 100^{\circ}\text{C}$)	EN SHIERT I	V _{DS} (on)	approsud nd meter d tching Spee	1 18	Vdc oo
Forward Transconductance (V _{DS} = 10 V, I _D = 4 A)	OA Spacified	9FS	V (no)eqv	ta — Toss	mhos
YNAMIC CHARACTERISTICS		betimil	Dissipation	DA is Power	ligged — Si
Input Capacitance	Inductive	Ciss	iarat <u>ta</u> rized	2200	rd-opForus
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	_	500	Loads
Reverse Transfer Capacitance	See Figure 14	C _{rss}	_	300	
WITCHING CHARACTERISTICS* (T	J = 100°C)				
Turn-On Delay Time		td(on)	-	40	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms) See Figures 11, 12 and 13	t _r		100	INUM RAT
Turn-Off Delay Time		td(off)	_	160	
Fall Time	DSS 250 Vdc	tf	_	90	N-Source V
Total Gate Charge	(Vps = 0.8 Rated Vpss,	Qg	20 (Typ)	40	nC nC

SOURCE DRAIN DIODE CHARACTERISTICS*

Gate-Source Charge

Gate-Drain Charge

Forward On-Voltage	- PS	V _{SD}	3 (Typ)	5	Vdc
Forward Turn-On Time	(I _S = Rated I _D V _{GS} = 0)	ton	200 (Typ)	25°C :	ns
Reverse Recovery Time	0° 100 00 00 00 00 00 00 00 00 00 00 00 00	t _{rr}	250 (Typ)	Storage Temy	bas ns

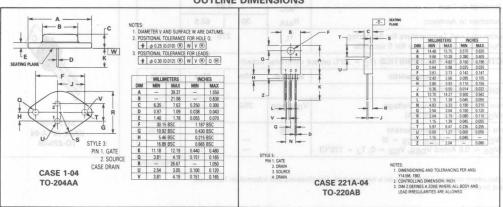
 $(V_{DS} = 0.8 \text{ Rated } V_{DSS},$ $I_{D} = \text{Rated } I_{D}, V_{GS} = 10 \text{ V})$ See Figure 10

 Q_{gs}

 Q_{gd}

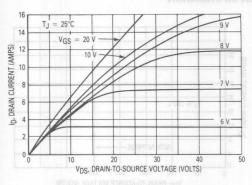
10 (Typ)

10 (Typ)



^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

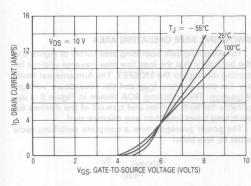
TYPICAL ELECTRICAL CHARACTERISTICS



1.1 VDS = VGS ID = 1 mA VDS = VGS ID = VGS ID = 1 mA VDS = VGS ID =

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



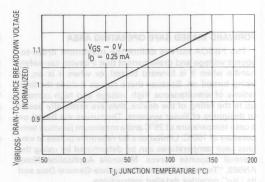
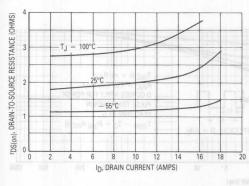


Figure 3. Transfer Characteristics

Figure 4. Normalized Breakdown Voltage versus Temperature



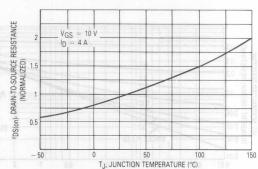


Figure 5. On-Resistance versus Drain Current

Figure 6. Normalized On-Resistance versus Temperature

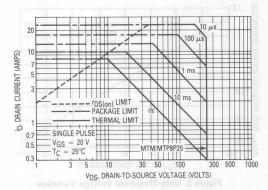


Figure 7. Maximum Rated Forward Bias Safe Operating Area

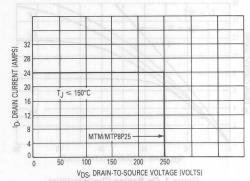


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

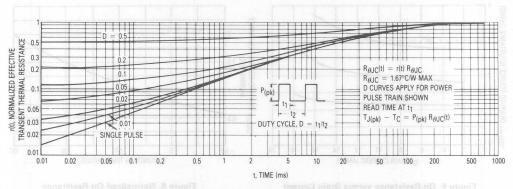
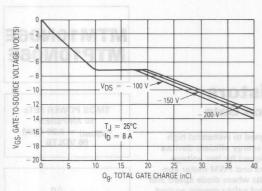


Figure 9. Thermal Response

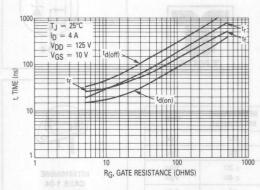
RESISTIVE SWITCHING



PULSE GENERATOR $z = 50 \Omega$ 0Ω 0

Figure 10. Gate Charge versus Gate-To-Source Voltage

Figure 11. Switching Test Circuit



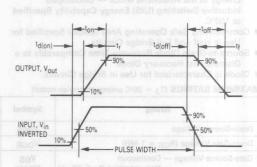


Figure 12. Resistive Switching versus Gate Resistance

Figure 13. Switching Waveforms

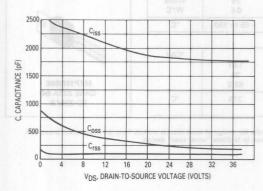


Figure 14. Capacitance Variation

MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Designer's Data Sheet

TMOS IV

Power Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

MAXIMUM RATINGS (T.) = 25°C unless otherwise noted)

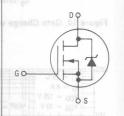
Rating	Symbol	MTM10N06E MTP10N06E	Unit
Drain-Source Voltage	VDSS	60	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	10 28	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

THERWAL CHARACTERIST	00			
Thermal Resistance Junction to Case Junction to Ambient	MTM10N06E MTP10N06E	R _θ JC R _θ JA	1.67 30 62.5	°C/W
Maximum Lead Temp. for S Purposes, 1/8" from case f		TL	275	°C



TMOS POWER FETS
10 AMPERES
rDS(on) = 0.20 OHM
60 VOLTS





MTM10N06E CASE 1-04 TO-204AA



MTP10N06E CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

TMOS

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characte	ristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				_	T
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	MTM/MTP10N06E	V(BR)DSS	60	Noval	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ = $\frac{1}{2}$	125°C)	IDSS	- V8	10 100	μΑ
Gate-Body Leakage Current, Forward (\		IGSSF	v2 - 1	100	nAdc
Gate-Body Leakage Current, Reverse (V		IGSSR	-	100	nAdc
ON CHARACTERISTICS*	8 1			TYT	
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C		V _{GS(th)}	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (VG:	s = 10 Vdc, In = 5 Adc)	rDS(on)	V3	0.2	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 10 Adc) (I _D = 5 Adc, T _J = 100°C)		V _{DS(on)}	2 '	2.2	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 5 A)		9FS	3.8	-	mhos
DRAIN-TO-SOURCE AVALANCHE STRESS	O A STUDIES AS A	001701101001	drid neigon	gure 1. ter	-
Unclamped Inductive Switching Energy (ID = 28 A, VDD = 10 V, TC = 25°C, (ID = 10 A, VDD = 10 V, TC = 25°C, (ID = 4 A, VDD = 10 V, TC = 100°C,	Single Pulse, Non-repetitive) P.W. ≤ 200 μs, Duty Cycle ≤ 1%)	W _{DSR}	=	35 55 22	mJ
DYNAMIC CHARACTERISTICS	9	1	0.00 - 01		
Input Canacitance		C _{iss}	-	600	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	A L	350	Pi
Reverse Transfer Capacitance	See Figure 16	C _{rss}	///	100	SI
SWITCHING CHARACTERISTICS* (TJ = 1	100°C)	orss	71	100	
Turn-On Delay Time	100 A B	t _{d(on)}		50	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	tr	1	120	
Turn-Off Delay Time	R _{gen} = 50 ohms)	td(off)	-111	50	11110
Fall Time	See Figures 9, 14 and 15	tf	- 13	60	
Total Gate Charge	0 02 - 07 or	Qq	15 (Typ)	26	nC
Gate-Source Charge MAT MOTOMULE	$(V_{DS} = 0.8 \text{ Rated } V_{DSS},$ $I_{D} = \text{Rated } I_{D}, V_{GS} = 10 \text{ V})$	Qgs	8 (Typ)	Vag. 6A0	
Gate-Drain Charge	See Figures 17 and 18	Qgd	7 (Typ)	Figure 3.	
SOURCE DRAIN DIODE CHARACTERISTIC	CS*	gu			
Forward On-Voltage		V _{SD}	1.1 (Typ)	1.5	Vdc
Forward Turn-On Time	$(I_S = 0.5 \text{ Rated } I_D \text{ V}_{GS} = 0)$	ton		by stray ind	luctance
Reverse Recovery Time		t _{rr}	70 (Typ)	90	ns
NTERNAL PACKAGE INDUCTANCE (TO-2	204)				ar
Internal Drain Inductance (Measured from the contact screw or to the source pin and the center of the		Ld	5 (Typ)		nH
Internal Source Inductance (Measured from the source pin, 0.25" to the source bond pad)	from the package	L _S	12.5 (Typ)		80
NTERNAL PACKAGE INDUCTANCE (TO-2	220)				
Internal Drain Inductance (Measured frrom the contact screw o (Measured from the drain lead 0.25" t		Ld	3.5 (Typ) 4.5 (Typ)		nH
		- 01			

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

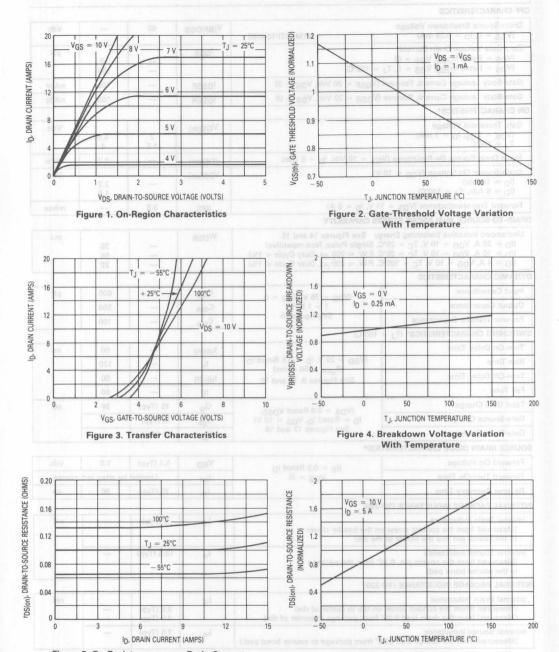


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

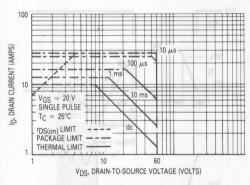


Figure 7. Maximum Rated Forward Biased Safe Operating Area

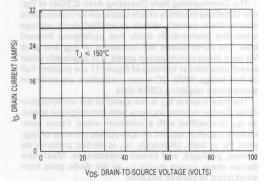


Figure 8. Maximum Rated Switching

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

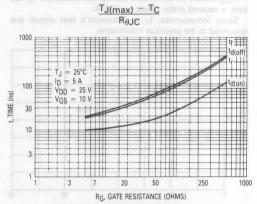


Figure 9. Resistive Switching Time Variation versus Gate Resistance

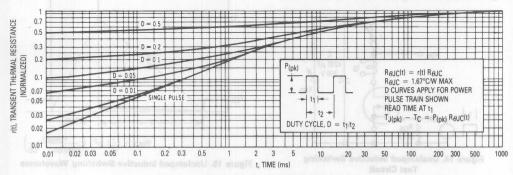


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of $I_{\mbox{FM}}$ and peak $V_{\mbox{R}}$ for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM} , peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

 $V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

 V_{R} is specified at 80% of $V_{\left(BR\right)DSS}$ to ensure that the CSOA stress is maximized as IS decays from IRM to zero.

RGS should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

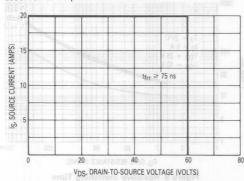


Figure 12. Commutating Safe Operating Area (CSOA)

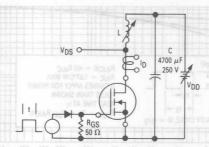


Figure 14. Unclamped Inductive Switching Test Circuit

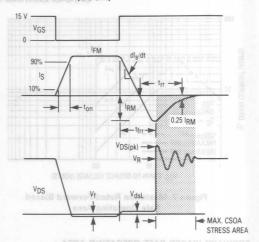


Figure 11. Commutating Waveforms

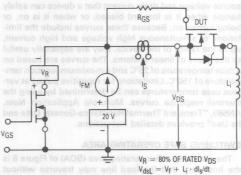


Figure 13. Commutating Safe Operating Area
Test Circuit

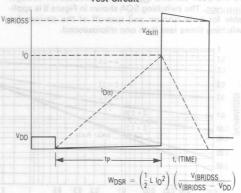


Figure 15. Unclamped Inductive Switching Waveforms

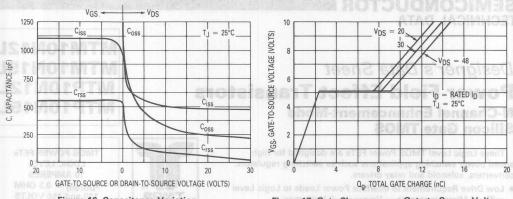


Figure 16. Capacitance Variation

Figure 17. Gate Charge versus Gate-to-Source Voltage

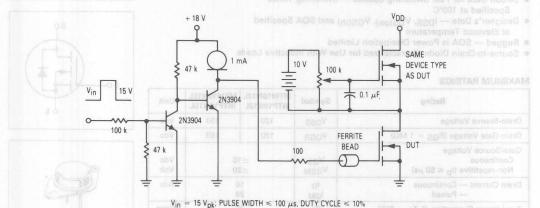
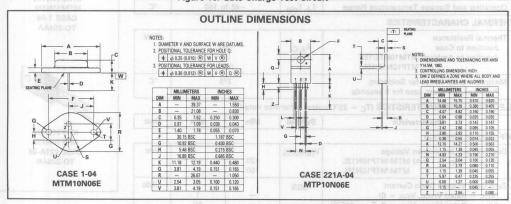


Figure 18. Gate Charge Test Circuit



Designer's Data Sheet

Power Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate TMOS

These Logic Level TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)} = 2 \text{ Volts max}$
- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

Rating	Symbol	MTM10N12L MTP10N12L	MTM10N15L MTP10N15L	Unit
Drain-Source Voltage	VDSS	120	150	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	120	150	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 15 ± 20		Vdc Vpk
Drain Current — Continuous = — Pulsed	I _D	10 28		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient MTM10N12/15L MTP10N12/15L	R _θ JC R _θ JA	1.67 30 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

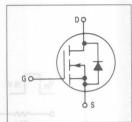
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	-6 -6-3	1 38	3 32 0	
Drain-Source Breakdown Voltage (VGS = 0, I _D = 1 mA) MTM/MTP10N12L MTM/MTP10N15L	V _{(BR)DSS}	120 150	753 271.02 94 70.63 950 To 1 1715 Au	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ = 125°C)	IDSS	- 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1	1 50	μAdo

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics are given to facilitate "worst case" design.

MTM10N12L MTM10N15L MTP10N12L MTP10N15L

TMOS POWER FETS LOGIC LEVEL 10 AMPERES rDS(on) = 0.3 OHM 120 and 150 VOLTS





MTM10N12L MTM10N15L **CASE 1-06** TO-204AA



MTP10N12L MTP10N15L **CASE 221A-04** TO-220AB

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Cha	racteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continue	d)	lya P	V68 = 7 V		
Gate-Body Leakage Current, For (VGSF = 15 Vdc, VDS = 0)	ward	IGSSF	13	100	nAdc
Gate Body Leakage Current, Rev (VGSR = 15 Vdc, VDS = 0)	verse	IGSSR	1-7	100	nAdc
ON CHARACTERISTICS	e e			3/1/-	
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) (TJ = 100°C)	20 32	VGS(th)	1 0.75	2 1.5	Vdc
Static Drain-Source On-Resistan	ce (VGS = 5 Vdc, ID = 5 Adc)	rDS(on)		0.3	Ohm
Drain-Source On-Voltage (V _{GS} (I _D = 10 Adc) (I _D = 5 Adc, T _J = 100°C)	0 00- 2 01	V _{DS(on)}	S = .	4 3.5	Vdc
Forward Transconductance (VDS	s = 10 V, I _D = 5 A)	9FS	4	nO 1 FramFi	mhos
OYNAMIC CHARACTERISTICS	W				
Input Capacitance	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	Ci-		1200	pF
input Capacitance	V _{GS} = 15 V, V _{DS} = 0, f = 1 MHz	Ciss		2800] Pr
Reverse Transfer Capacitance	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	C	14/-	60	pF
neverse transfer Capacitance	V _{GS} = 15 V, V _{DS} = 0, f = 1 MHz	C _{rss}	1	2400	Pr
Output Capacitance	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	Coss	1 4//	250	pF
WITCHING CHARACTERISTICS (Г _Ј = 100°С)	V08 = 10			
Turn-On Delay Time		t _d (on)		60	ns
Rise Time	$(V_{DD} = 25 \text{ V}, I_{D} = 7.5 \text{ A},$	tr	_	135	
Turn-Off Delay Time	V _{GS} = 5 V, R _{gen} = 50 ohms)	td(off)		135	
Fall Time		tf		135	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Qg	14 (typ)	20	nC
Gate-Source Charge	I _D = 15 A, V _{GS} = 5 Vdc)	Qgs	7 (typ)	- 1	
Gate-Drain Charge	See Figures 6 and 10.	Qgd	7 (typ)	Vois GATE-T	
SOURCE DRAIN DIODE CHARACT	ERISTICS				
Forward On-Voltage	Figure 4. Capac	V _{SD}	1.6 (typ)	Figure 3, Tri	Vdc
Forward Turn-On Time	$(I_S = Rated I_D, V_{GS} = 0)$	ton	Limited	d by stray indi	uctance
Reverse Recovery Time		t _{rr}	150 (typ)	_	ns
NTERNAL PACKAGE INDUCTANO	E (TO-204)				
Internal Drain Inductance (Measured from the contact so to the source pin and the cent		Ld	5 (Typ)		nH
Internal Source Inductance (Measured from the source pi to the source bond pad)	n, 0.25" from the package	L _S	12.5 (Typ)	NO IN IT	à
NTERNAL PACKAGE INDUCTANO	E (TO-220)				
Internal Drain Inductance (Measured from the contact scre (Measured from the drain lead (ew on tab to center of die) 0.25" from package to center of die)	Ld	3.5 (Typ) 4.5 (Typ)	25	nH
Internal Source Inductance	0.25" from package to source bond pad.)	L _s	7.5 (Typ)	6	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.



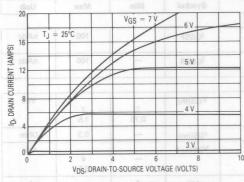
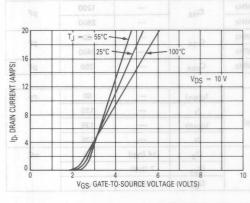


Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



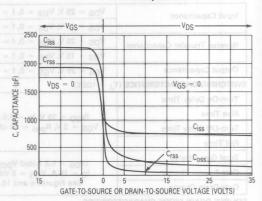
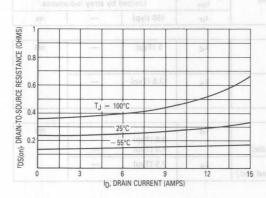


Figure 3. Transfer Characteristics

Figure 4. Capacitance Variation With Voltage



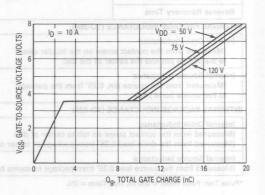
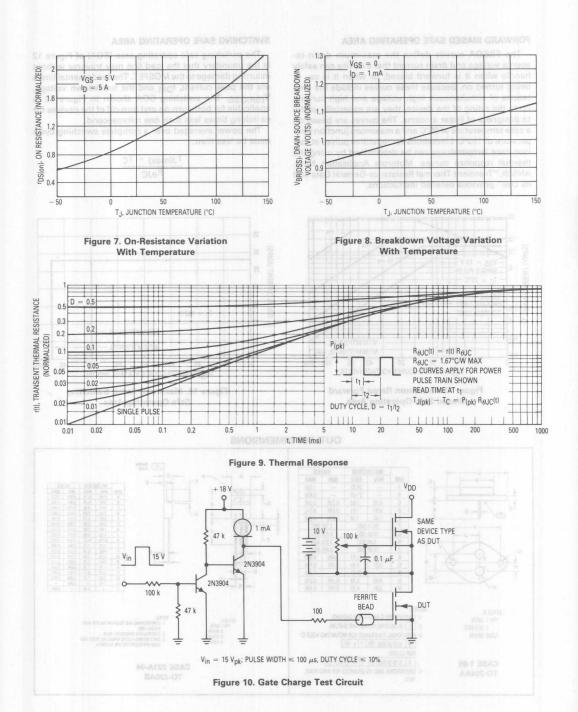


Figure 5. On-Resistance Variation With Drain Current

Figure 6. Gate Charge versus Gate-To-Source Voltage



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-tosource voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

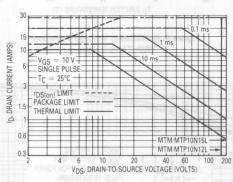


Figure 11. Maximum Rated Forward **Biased Safe Operating Area**

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 12 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 12 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{\mathsf{T}_{\mathsf{J}(\mathsf{max})} - \mathsf{T}_{\mathsf{C}}}{\mathsf{R}_{\theta}\mathsf{J}\mathsf{C}}$$

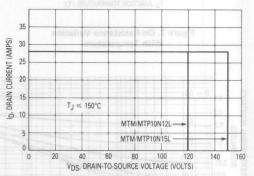
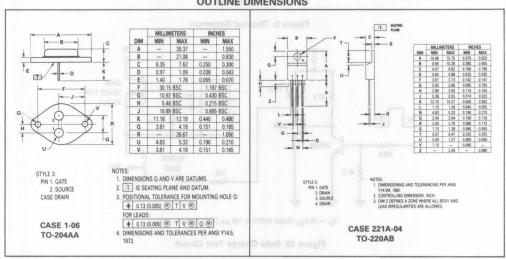


Figure 12. Maximum Rated Switching Safe Operating Area



MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

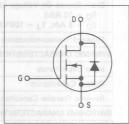
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS 10 AMPERES rDS(on) = 0.45 OHM 250 VOLTS



MAXIMUM RATINGS

OS Rating	Cumbal	MTM or MTP	Unit
us nating	Symbol	10N25	Onit
Drain-Source Voltage	V _{DSS}	250	Vdc
Drain-Gate Voltage (R _{GS} = 1 M Ω)	VDGR	250	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	IDM	10 30	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	100 0.8	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance				°C/W
Junction to Case		R _θ JC	1.25	
Junction to Ambient	TO-204	$R_{\theta JA}$	30	0.280 Erom
	TO-220		62.5	-
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C



MTM10N25 CASE 1-04 TO-204AA



MTP10N25 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Characteristic			Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	$(V_{GS} = 0, I_D = 0.25 \text{ mA})$		V _{(BR)DSS}	250	_	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0 (VDS = 0.8 Rated VDSS, VGS			IDSS	lata_Si	0.2	mAdc
Gate-Body Leakage Current, Forv	vard (V _{GSF} = 20 Vdc, V _{DS} = 0)	S CARD II	IGSSF	E mail 8-071	100	nAdc
Gate-Body Leakage Current, Reve	erse (V _{GSR} = 20 Vdc, V _{DS} = 0)	91	IGSSR	megns	100	nAdc
ON CHARACTERISTICS*				SON	T effet	con
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C	, high julators,	vallege hing reg	VGS(th)	2 1.5 2001331100	4.5 4	Vdc
Static Drain-Source On-Resistance	e (V _{GS} = 10 Vdc, I _D = 5 Adc)		rDS(on)	TEVERY DEVE	0.45	Ohm
Drain-Source On-Voltage (V _{GS} = (I _D = 10 Adc) (I _D = 5 Adc, T _J = 100°C)	10 V)	SOA Sp	V _{DS(on)}	S VDS(on)	5.6 4.5	Vdc
Forward Transconductance (VDS	= 15 V, I _D = 5 A)		9FS	3.5	SOA is Pow	mhos
DYNAMIC CHARACTERISTICS	absol evis	th Induc	d tor Use W	Characterize	rain Diode	d-of-som
Input Capacitance	(Vpc = 25 V Vcc = (2	Ciss	_	1500	pF
Output Capacitance	f = 1 MHz	(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 11			400	
Reverse Transfer Capacitance	See Figure 11				100	
SWITCHING CHARACTERISTICS* (Γ _J = 100°C)					
Turn-On Delay Time			td(on)	_	50	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rat	ed ID	t _r	_	250	SI IMESMI
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 1	14	td(off)	_	100	TI MILITAN
Fall Time	find a service	Symbol	tf	- 60	120	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DS}	C. Table	Qg	37 (Typ)	60	nC
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10		Qgs	21 (Typ)	And north	of areasts as
Gate-Drain Charge	See Figure 12	PICHU -	Q_{gd}	16 (Typ)	Charles and all	The STEEL ST
SOURCE DRAIN DIODE CHARACTE	RISTICS*	Vasiv	(en 03 > n3)	avidager-no	N —	
Forward On-Voltage	(IS = Rated ID	el l	V _{SD}	1.6 (Typ)	2.5	Vdc
Forward Turn-On Time	V _{GS} = 0)	MOI	ton	Limited	by stray ind	uctance
Reverse Recovery Time	200 V 300	69	t _{rr}	300 (Typ)	Dissipation (ns
NTERNAL PACKAGE INDUCTANCE	(TO-204)			All and the contract of	Tanana A	no nation
Internal Drain Inductance (Measured from the contact so to the source pin and the center			Ld	5 (Typ)	ARACTERN	nH AAAA
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L _S	12.5 (Typ)	Case_ Ambient	or notion totalan te	
NTERNAL PACKAGE INDUCTANCE	(TO-220)		Want of			
Internal Drain Inductance (Measured from the contact sc (Measured from the drain lead	rew on tab to center of die) 0.25" from package to center of di	ie)	Ld	3.5 (Typ) 4.5 (Typ)	18" from cas	nH
Internal Source Inductance (Measured from the source lea	d 0.25" from package to source bo	nd pad.)	L _S	7.5 (Typ)	-	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

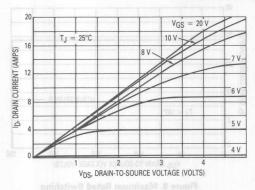


Figure 1. On-Region Characteristics

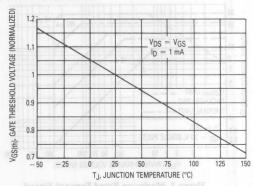


Figure 2. Gate-Threshold Voltage Variation With Temperature

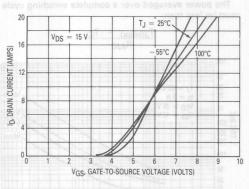


Figure 3. Transfer Characteristics

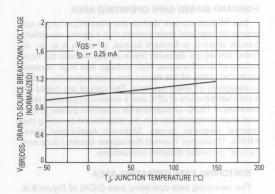


Figure 4. Breakdown Voltage Variation
With Temperature

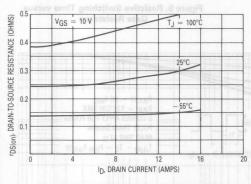


Figure 5. On-Resistance versus Drain Current

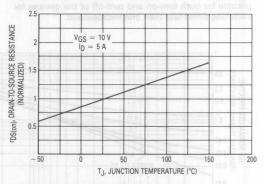


Figure 6. On-Resistance Variation With Temperature

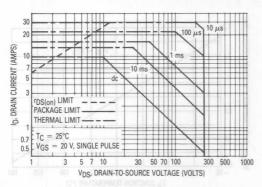


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

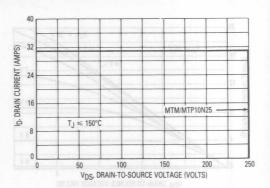


Figure 8. Maximum Rated Switching
Safe Operating Area

The power averaged over a complete switching cycle must be less than:

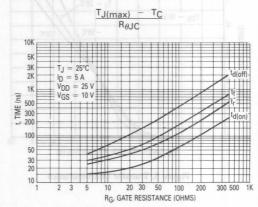


Figure 9. Resistive Switching Time versus
Gate Resistance

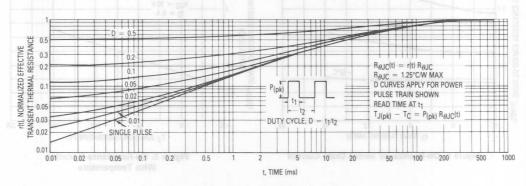
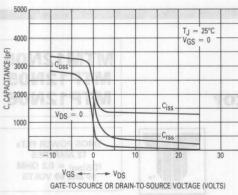


Figure 10. Thermal Response



T_J = 25°C GATE SOURCE VOLTAGE (VOLTS) ID = 10 A 125 V V_{DS} = 80 V ,GS, (20 10 Q₀, TOTAL GATE CHARGE (nC)

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-To-Source Voltage



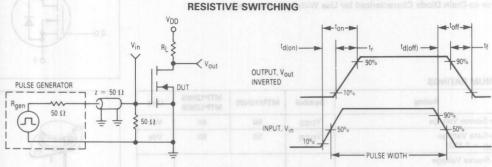
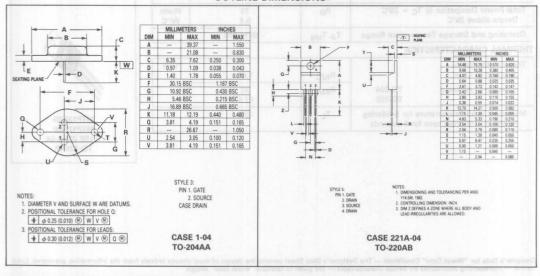


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

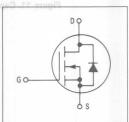
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MTM12N05 MTP12N05 MTP12N06



TMOS POWER FETS
12 AMPERES
rDS(on) = 0.2 OHM
50 and 60 VOLTS



MAXIMUM RATINGS

3

Rating	Symbol	MTM12N05	MTP12N05 MTP12N06	Unit
Drain-Source Voltage	V _{DSS}	50	60	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	V _{DGR}	50	60	Vdc
Gate-Source Voltage Continuous Non-repetitive $(t_p \leqslant 50~\mu s)$	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current Continuous Pulsed	I _D	12 243440 3 30 TUO		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204 TO-220	$R_{\theta JA}$	30 62.5	28 (8 t) 28 (8 t) 21 (4.6
Maximum Lead Temperatu Purposes, 1/8" from case		TL	275	°C



MTM12N05 CASE 1-04 TO-204AA



MTP12N05 MTP12N06 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Charac	Characteristic		Min	Max	Unit
OFF CHARACTERISTICS				TXT	
Drain-Source Breakdown Voltage $(V_{GS} = 0, I_D = 0.25 \text{ mA})$	MTM/MTP12N05 MTP12N06	V(BR)DSS	50 60	1-/m	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ	= 125°C)	IDSS	E	10 100	μAde
Gate-Body Leakage Current, Forward	(V _{GSF} = 20 Vdc, V _{DS} = 0)	IGSSF		100	nAde
Gate-Body Leakage Current, Reverse	(V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR		100	nAde
ON CHARACTERISTICS*	8.0 th	I V B			737
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$ $T_{J} = 100^{\circ}\text{C}$	0 85 - 08 - 01	V _{GS(th)}	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (V	'GS = 10 Vdc, I _D = 6 Adc)	rDS(on)	10-50 <u>JR</u> DE VOU	0.2	Ohn
Drain-Source On-Voltage ($V_{GS} = 10$ ($I_D = 12$ Adc) ($I_D = 6$ Adc, $T_J = 100^{\circ}$ C)	Figure 2. (W	VDS(on)	n-Region Ch	3 2.8	Vdc
Forward Transconductance (VDS =	15 V, I _D = 6 A)	9FS	4	·—	mho
DYNAMIC CHARACTERISTICS	2				
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0,	Ciss		400	pF
Output Capacitance	f = 1 MHz	Coss	-	300	Vne =
Reverse Transfer Capacitance	See Figure 11	C _{rss}	- SH2	100	
SWITCHING CHARACTERISTICS* (TJ	= 100°C)		36-36		
Turn-On Delay Time		td(on)	W	60	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r	1//-	160	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)		80	
Fall Time	0.4	tf		110	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Qg	13 (Typ)	26	nC
Gate-Source Charge	ID = Rated ID, VGS = 10 V)	Qgs	6 (Typ)	1-	
Gate-Drain Charge	See Figure 12	Q _{gd}	7 (Typ)	VGS-DRAIR	
SOURCE DRAIN DIODE CHARACTERIS	TICS*	enitaisetos	randO valence	T E amol?	
Forward On-Voltage	(I _S = Rated I _D	V _{SD}	1.8 (Typ)	3.2	Vdd
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	luctance
Reverse Recovery Time		t _{rr}	300 (Typ)		ns
NTERNAL PACKAGE INDUCTANCE (T	0-204)				
	nternal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		5 (Typ)	V W = 80	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L _S	12.5 (Typ)	, T	
NTERNAL PACKAGE INDUCTANCE (T	0-220)	-	25°C		
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L _d	3.5 (Typ) 4.5 (Typ)	=	nH
Internal Source Inductance (Measured from the source lead 0.	25" from package to source bond pad.)	L _S	7.5 (Typ)		

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

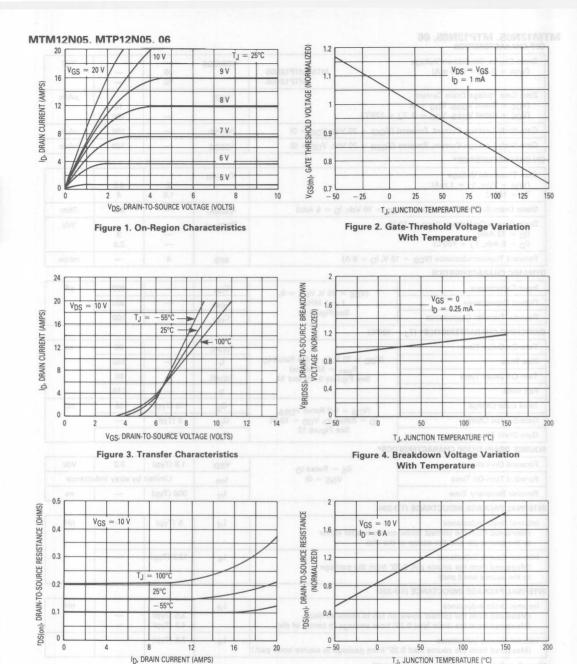


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

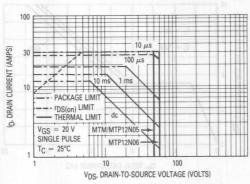


Figure 7. Maximum Rated Forward Biased Safe Operating Area

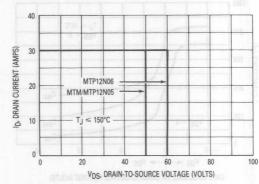


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{BR}DSS$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

Figure 9. Resistive Switching Time Variation versus Gate Resistance

RG, GATE RESISTANCE (OHMS)

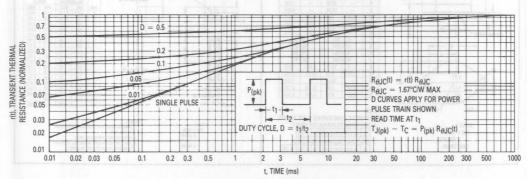
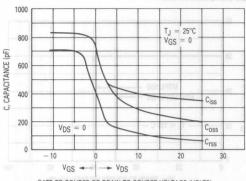


Figure 10. Thermal Response





GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 11. Capacitance Variation

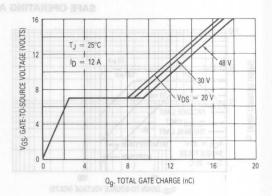


Figure 12. Gate Charge versus

Gate-to-Source Voltage

RESISTIVE SWITCHING

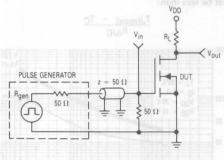


Figure 13. Switching Test Circuit

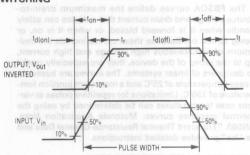
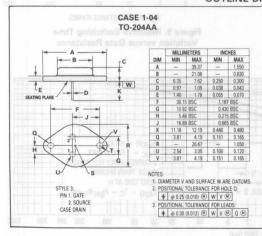
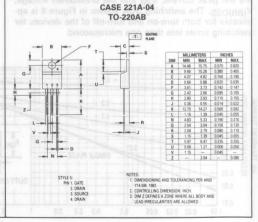


Figure 14. Switching Waveforms





MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

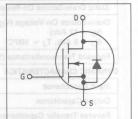
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS
12 AMPERES
rDS(on) = 0.18 OHM
80 and 100 VOLTS



MAXIMUM RATINGS

Rating	Symbol	MTM12N10	MTP12N08 MTP12N10	Unit
Drain-Source Voltage	VDSS	80	100	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	80	100	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous (QVT) 9 — Pulsed	I _D	27 en 12 l ee8 30		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75 0.6		Watts W/°C
Operating and Storage Temperature Range	TJ, Tstq	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance				°C/W
Junction to Case	(Typ)	R_{θ} JC	1.67	
Junction to Ambient	TO-204	$R_{\theta JA}$	30	ert ellt no wer
	TO-220		62.5	1016 513 10 1
Maximum Lead Temperatu Purposes, 1/8" from case		TL	275	°C



MTM12N10 CASE 1-04 TO-204AA



MTP12N08 MTP12N10 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Citat a Citat	eristic	Symbol	IVIIN	IVIax	Oilit
OFF CHARACTERISTICS		V(BR)DSS			
Drain-Source Breakdown Voltage			80 100	Q ⊋'ne	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ	= 125°C)	IDSS	HI b	10 100	μAdc
Gate-Body Leakage Current, Forward		IGSSF		100	nAdc
Gate-Body Leakage Current, Reverse	(V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR		100	nAdc
ON CHARACTERISTICS*	postlov m	ilham sol has	intent our sT	22 may 9	2015T as
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C	witching regu-	V _{GS(th)}	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (V	GS = 10 Vdc, I _D = 6 Adc)	rDS(on)	_	0.18	0 Ohm
Drain-Source On-Voltage ($V_{GS} = 10$) ($I_D = 12$ Adc) ($I_D = 6$ Adc, $T_J = 100$ °C)	V) beilinge AO.	V _{DS(on)}	VDS(on): ure er Dissipatio	2.6 2.2	Vdc
Forward Transconductance (V _{DS} = 1	9FS	3	ann Diode	mhos	
DYNAMIC CHARACTERISTICS					
Input Capacitance	N 25 V V 0	Ciss	_	800	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz})$	Coss	_	400	1
Reverse Transfer Capacitance	See Figure 11	C _{rss}	_	100	
WITCHING CHARACTERISTICS* (TJ =	100°C)			SEMIL	AR MUIN
Turn-On Delay Time	MITPIZNIO WITPIZNOS U	td(on)	_	50	ns
Rise Time	$(V_{DD} = 25 \text{ V}, I_{D} = 0.5 \text{ Rated } I_{D}$	tr	_	150	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	7000.0	200	10 10 0 G-11
Fall Time		tf	1100	100	NA STREET
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	ων Q _g	17 (Typ)	36	nC
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 V)	an Ogs	8 (Typ)	ve (1 ₀ ≤ 80 /	ilteder-no
Gate-Drain Charge	See Figure 12	Qgd	9 (Typ)	— Continuos	n Current
OURCE DRAIN DIODE CHARACTERIST	TICS*	hear .	2000 - 27	S. moitonias	O. w. inn 9:1
Forward On-Voltage	(I _S = Rated I _D	V _{SD}	1.2 (Typ)	2.5	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	luctance
Reverse Recovery Time		t _{rr}	325 (Typ)	ALA,CTERIS	ns
NTERNAL PACKAGE INDUCTANCE (TO	0-204)			90/18/	ninal Regist
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		ALSA Ld	5 (Typ)	Case Ambjent	Hnon to
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L _S	12.5 (Typ)	d Tamperati 8" from case	imum Les iposes, 1
NTERNAL PACKAGE INDUCTANCE (TO)-220)				-
Internal Drain Inductance (Measured from the contact screw (Measured from the drain lead 0.25	L _d	3.5 (Typ) 4.5 (Typ)	_	nH	
Internal Source Inductance (Measured from the source lead 0.2	L _S	7.5 (Typ)	_		

TYPICAL ELECTRICAL CHARACTERISTICS

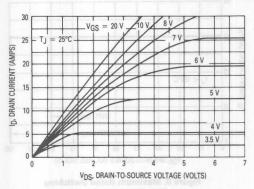


Figure 1. On-Region Characteristics

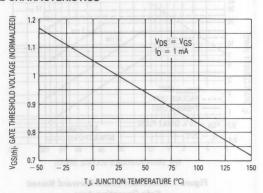


Figure 2. Gate-Threshold Voltage Variation With Temperature

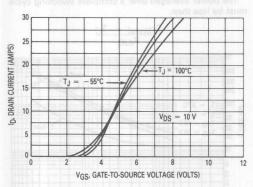


Figure 3. Transfer Characteristics

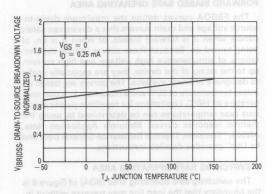


Figure 4. Breakdown Voltage Variation
With Temperature

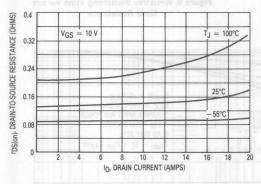


Figure 5. On-Resistance versus Drain Current

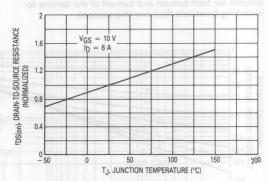


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

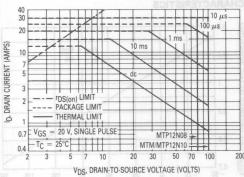


Figure 7. Maximum Rated Forward Biased Safe Operating Area

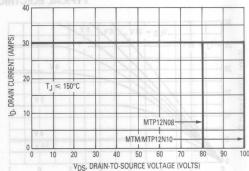


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{BR}DSS$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

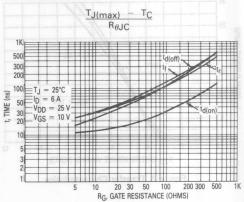


Figure 9. Resistive Switching Time versus
Gate Resistance

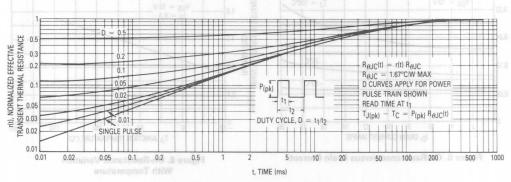
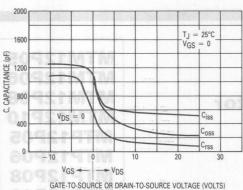


Figure 10. Thermal Response



GATE SOURCE VOLTAGE (VOLTS) T_J = 25°C $I_D = 12 A$ 50 V VDS = 30 V-VGS, Qq, TOTAL GATE CHARGE (nC)

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-To-Source Voltage

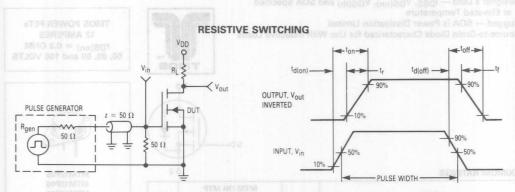
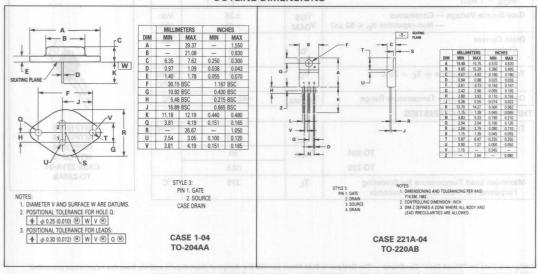


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms



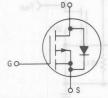
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MTM12P05 MTM12P06 MTM12P08 MTM12P10 MTP12P05 MTP12P06 MTP12P08 MTP12P10



TMOS POWER FETS
12 AMPERES
rDS(on) = 0.3 OHM
50, 60, 80 and 100 VOLTS





3

P-4i		MTM OR MTP				11-14
Rating Adding At mage	Symbol	12P05	12P06	12P08	12P10	Unit
Drain-Source Voltage	V _{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	50	60	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40		89313	Vdc Vpk	
Drain Current Continuous Pulsed	I _D	12 28		X688 10.60 80.70 53.1	Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75 0.6		8.1	Watts W/°C	
Operating and Storage Temperature Range	TJ, Tstg	-65 to 150			°C	

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		R _θ JC	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta}JA$	30	RIA IKE
	TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	2° 57 1 64



MTM12P05 MTM12P06 MTM12P08 MTM12P10 CASE 1-04 TO-204AA



MTP12P05 MTP12P06 MTP12P08 MTP12P10 CASE 221A-04 TO-220AB

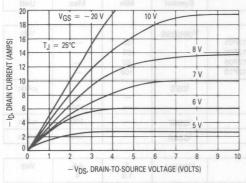
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Chara	cteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS				or JA	M.— = 50A	1
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)		MTM/MTP12P05 MTM/MTP12P06 MTM/MTP12P08 MTM/MTP12P10	V(BR)DSS	50 60 80 100	7 - 24 -	Vdc
Zero Gate Voltage Drain Current $(V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0)$ $(V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0,\ T$	J = 125°C)	08.0 CD	IDSS		10 100	μAdc
Gate-Body Leakage Current, Forwar		c, V _{DS} = 0)	IGSSF		100	nAdc
Gate-Body Leakage Current, Revers	e (VGSR = 20 Vd	c, V _{DS} = 0)	IGSSR	77-7-	100	nAdo
ON CHARACTERISTICS*		ma E				1 50
Gate Threshold Voltage (V _{DS} = V _C T _J = 100°C	SS, ID = 1 mA)		VGS(th)	1.5	4.5	Vdc
Static Drain-Source On-Resistance	VGS = 10 Vdc, Ic) = 6 Adc)	rDS(on)	n-Region Cl	0.3	Ohm
Drain-Source On-Voltage ($V_{GS} = 1$ ($I_D = 12$ Adc) ($I_D = 6$ Adc, $T_J = 100$ °C)	0 V)		V _{DS(on)}	=	4.2 3.8	Vdc
Forward Transconductance (VDS =	15 V, I _D = 6 A)	8	9FS	2		mhos
DYNAMIC CHARACTERISTICS				NI		
Input Capacitance	(Vpc =	25 V Voo = 0	Ciss	44	920	pF
Output Capacitance	$V_{DS} = 25 \text{ V, } V_{GS} = 0,$ $V_{GS} = 1 \text{ MHz}$		Coss	- N - / -	575	
Reverse Transfer Capacitance	See	Figure 10	C _{rss}	7//	200	
SWITCHING CHARACTERISTICS* (TJ	= 100°C)	八隻第 一十				
Turn-On Delay Time	1 88		td(on)	- 1	50	ns
Rise Time		/, I _D = 0.5 Rated I _D	any t _r	- 1	150	
Turn-Off Delay Time		= 50 ohms) ures 12 and 13	td(off)	_	150	
Fall Time		100	tf	-	150	
Total Gate Charge	(Vps = (0.8 Rated V _{DSS} ,	Q_g	33 (Typ)	50	nC
Gate-Source Charge	I _D = Rated	$d I_D, V_{GS} = 10 V)$	Qgs	16 (Typ)	STWIT SDA	
Gate-Drain Charge	See See	Figure 11	Q_{gd}	17 (Typ)	Figure 3. 7	
SOURCE DRAIN DIODE CHARACTERI	STICS*					
Forward On-Voltage	(Is	= Rated I _D	V _{SD}	4 (Typ)	5.5	Vdc
Forward Turn-On Time	V	GS = 0)	ton	Limited	by stray ind	uctance
Reverse Recovery Time		a g	t _{rr}	300 (Typ)		ns
NTERNAL PACKAGE INDUCTANCE (TO-204)	ar 3		0.00	-6	
	Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		Ld	5 (Typ)	1	nH
internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L _S	12.5 (Typ)			
NTERNAL PACKAGE INDUCTANCE (TO-220)					1
Internal Drain Inductance (Measured from the contact screv (Measured from the drain lead 0.			Ld	3.5 (Typ) 4.5 (Typ)		nH
Internal Source Inductance (Measured from the source lead	Lq.T		L _S (2704)		gl = 8	0 9

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS



1.1 VDS = VGS ID = 1 mA

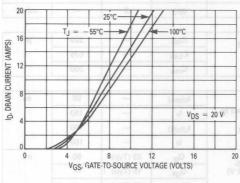
VDS = VGS
ID = 1 mA

VDS = VGS
ID = 1 mA

VDS = VGS
ID = 1 mA

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



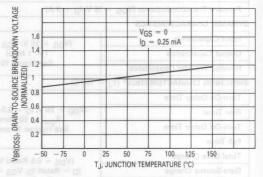
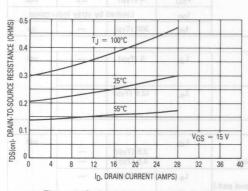


Figure 3. Transfer Characteristics

Figure 4. Normalized Breakdown Voltage versus Temperature



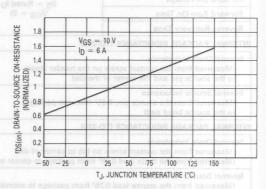


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

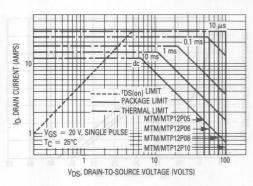


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

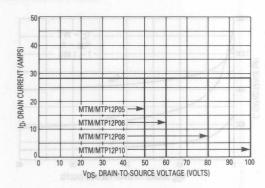


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

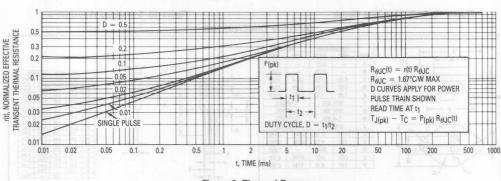


Figure 9. Thermal Response

3

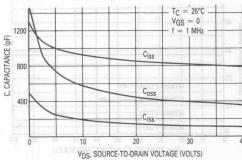


Figure 10. Capacitance Variation

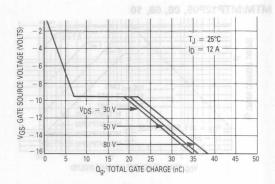


Figure 11. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

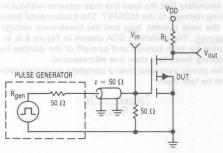


Figure 12. Switching Test Circuit

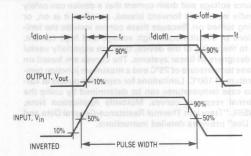
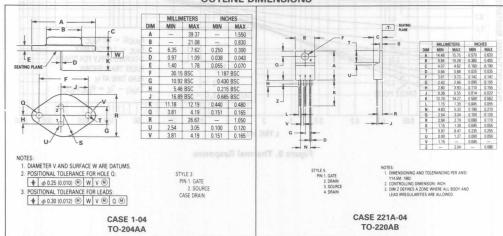


Figure 13. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA TMOS POWER MOSFET DATA

Designer's Data Sheet

Power Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate TMOS

These Logic Level TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — V_{GS(th)} = 2 Volts max
- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

Rating	Symbol	MTM15N05L MTP15N05L	MTM15N06L MTP15N06L	Unit
Drain-Source Voltage	V _{DSS}	50	60	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	50	60	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	A & X = 0 V & S = 12 15 16 16 16 16 16 16 16		Vdc Vpk
Drain Current — Continuous — Pulsed	I _D			Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	4 000	5 85 A 86	Watts W/°C
Operating and Storage Temperature Range	TJ, Tstg	-65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	R_{θ} JC	1.67 AT 19100	°C/W
Junction to Ambient MTM15N05 MTP15N05		30 62.5	1505-0
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 second	T _L	275	°C

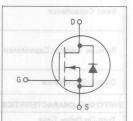
ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (VGS = 0, ID = 1 mA) MTM/MTP15N05L MTM/MTP15N06L	V(BR)DSS	50 60	ih to saturo	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ = 125°C)	IDSS	tter of dia)	1 50	μAdc

(continued)

MTM15N05L MTM15N06L MTP15N05L MTP15N06L

TMOS POWER FETS LOGIC LEVEL 15 AMPERES rDS(on) = 0.15 OHM 50 and 60 VOLTS





MTM15N05L MTM15N06L CASE 1-04 TO-204AA



MTP15N05L MTP15N06L CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

source bond pad.)

Cha	racteristic	Symbol	Min	Max	Un
OFF CHARACTERISTICS (continue	d)				
Gate-Body Leakage Current, For	ward (VGSF = 15 Vdc, VDS = 0)	IGSSF	_	100	nAd
Gate Body Leakage Current, Rev	verse (VGSR = 15 Vdc, VDS = 0)	IGSSR		100	nAd
ON CHARACTERISTICS			199110 1	210/7 0	1031
Gate Threshold Voltage	avotaiar	V _{GS(th)}	56PF	blail	Vd
$(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$		- 1 7 - 1	1 0.75	2 1.5	
(T _J = 100°C)	-	5D01VI	0.75	0.15	Oh
Static Drain-Source On-Resistan (VGS = 5 Vdc, ID = 7.5 Adc)	Ce	rDS(on)	- 0	0.15	Olli
Drain-Source On-Voltage (VGS	= 5 V)	V _{DS(on)}	wer FETs are	el TVIDS Per	Vd
(ID = 15 Adc)		switching ne	tions such at	3 1.5	diwa 18
(I _D = 7.5 Adc, T _J = 100°C)	2 - 15 V Ip - 7 5 A)	are	mevish 5	volet bos bi	mh
Forward Transconductance (VD: DYNAMIC CHARACTERISTICS	S = 15 V, 10 = 7.5 A)	9FS	1990 1 10001101	rement to la	Micros
DITAMIN ONANACIENISTICS	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	Switching	VGS(th) = 2 ng Speeds	900	tot ster
Input Capacitance		C _{iss}		0.00	18 be
QQ .	V _{GS} = 15 V, V _{DS} = 0, f = 1 MHz See Figure 4	9155	Slou). Vesin	2800	ple pl
	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	ted	miJ r oi tsgis:	200	408 -
Reverse Transfer Capacitance	V _{GS} = 15 V, V _{DS} = 0, f = 1 MHz	C _{rss}	tot besitela	2400	of pl
	See Figure 4			90	arrain i
Output Capacitance	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz See Figure 4	Coss	_	450	pl
SWITCHING CHARACTERISTICS (T _J = 100°C)				
Turn-On Delay Time	SO GO Vdo	td(on)	- (0	40	name n
Rise Time	(V _{DD} = 25 V, I _D = 7.5 A,	t _r	_	260	raioV en
Turn-Off Delay Time	V _{GS} = 5 V, R _{gen} = 50 ohms)	td(off)	_	200	Buc
Fall Time	XQV USE	tf		200	etiliya
Total Gate Charge	(Vec = 0.9 Poted Vece	Qq	14 (typ)	22	n
Gate-Source Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = 15 A, V _{GS} = 5 Vdc)	Qgs	7 (typ)	oT (W op) in	in idla
Gate-Drain Charge	See Figures 6 and 10.	Q _{gd}	7 (typ)	- 0°	to avod
SOURCE DRAIN DIODE CHARACT	ERISTICS OUT OF 39 -	preT.LT	dure Range	rage Tempera	and Sto
Forward On-Voltage		V _{SD}	1.8 (typ)	CTEMETICS	Vo
Forward Turn-On Time	(I _S = Rated I _D , V _{GS} = 0) See Figures 14 and 15.	ton	Limited	d by stray indi	uctance
Reverse Recovery Time	See Figures 14 dilu 15.	Rajo	300 (typ)		to Case
INTERNAL PACKAGE INDUCTANO	CF (TO-204)	t _{rr}	300 (typ)	TM Justic	mA or
Internal Drain Inductance	(10-204)	Ld	5 (Typ)	imp. for Solds	Tosen
The state of the s	crew on the header closer to the	-a	sbroose	om case for 6	1/8"
Internal Source Inductance	vinti vata jas	Ls	12.5 (Typ)	Abota Total	AHO JI
(Measured from the source pi source bond pad.)	n 0.25" from the package to the	I CONTRACT		neracceristic 108	PERSTO
INTERNAL PACKAGE INDUCTANO	E (TO-220)	V(BR)DSS	- 0	kdown Voltag	ser8 apr
Internal Drain Inductance		Ld	TOWALL PRINCET	MINA DAIN D	nl
(Measured from the contact s (Measured from the drain lead	crew on tab to center of die) d 0.25" from package to center of die)	aant	3.5 (Typ) 4.5 (Typ)	nsonu Z ninsci	inestell.

3

TYPICAL CHARACTERISTICS

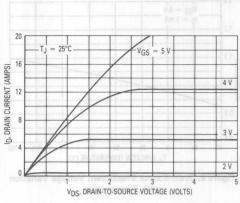


Figure 1. On-Region Characteristics

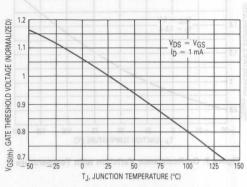


Figure 2. Gate-Threshold Voltage Variation With Temperature

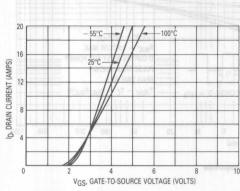


Figure 3. Transfer Characteristics

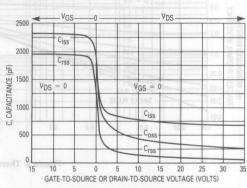


Figure 4. Capacitance Variation

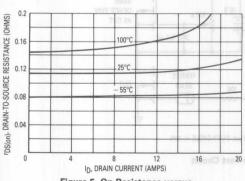


Figure 5. On-Resistance versus Drain Current

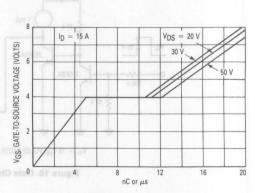


Figure 6. Gate Charge Variation

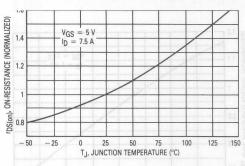


Figure 7. On-Resistance Variation with Temperature

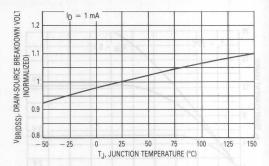


Figure 8. Drain-Source Breakdown Voltage Variation with Temperature

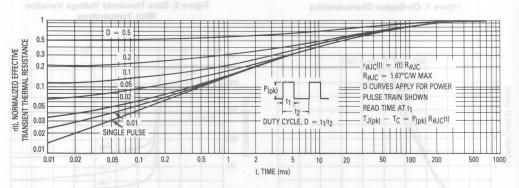


Figure 9. Thermal Response

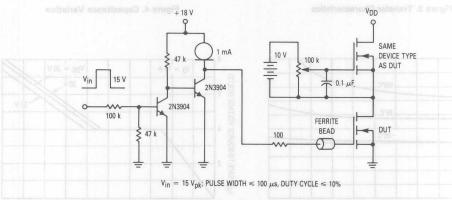


Figure 10. Gate Charge Test Circuit

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 12 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, V_{BR} DSS. The switching SOA shown in Figure 12 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{\mathsf{T}\mathsf{J}(\mathsf{max}) - \mathsf{T}\mathsf{C}}{\mathsf{R}_{\theta}\mathsf{J}\mathsf{C}}$$

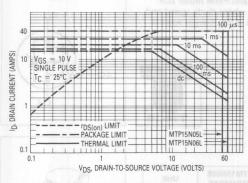


Figure 11. Maximum Rated Forward Biased Safe Operating Area

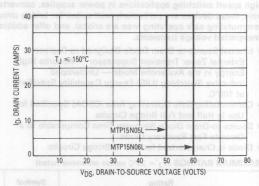
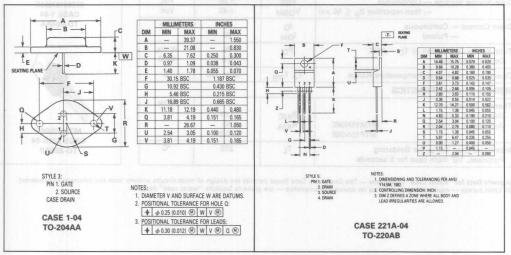


Figure 12. Maximum Rated Switching Safe Operating Area

OUTLINE DIMENSIONS



■ SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet TMOS IV and be no multiple for exception

Power Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	MTM15N06E MTP15N06E	Unit
Drain-Source Voltage A gnillang Q alas	V _{DSS}	60	Vdc
Drain-Gate Voltage (R _{GS} = 1 M Ω)	VDGR	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	15 40	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

TILITIMAL OTTATIAOTETIOT	100			
Thermal Resistance Junction to Case Junction to Ambient	MTM15N06E MTP15N06E	R_{θ} JC R_{θ} JA	1.67 30 62.5	°C/W
Maximum Lead Temp. for S Purposes, 1/8" from case f		TL	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



TMOS POWER FETs 15 AMPERES rDS(on) = 0.15 OHM 60 VOLTS





MTM15N06F **CASE 1-04** TO-204AA



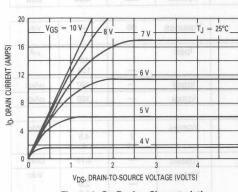
MTP15N06E **CASE 221A-04** TO-220AB

ELECTRICAL	CHARACTERISTICS	(Tc =	25°C unless	otherwise	noted)

	racteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	9			_	
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	278	V(BR)DSS	60	7 701 =	Vdc
Zero Gate Voltage Drain Current (Vps = Rated Vpss, Vgs = 0) (Vps = Rated Vpss, Vgs = 0,	T _J = 125°C)	IDSS	va F	10 100	μΑ
Gate-Body Leakage Current, Forwa	ard (VGSF = 20 Vdc, VDS = 0)	IGSSF	- 1	100	nAdc
Gate-Body Leakage Current, Rever	se (V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR		100	nAdc
N CHARACTERISTICS*			V8 5V		70
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C	30 30	V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	(V _{GS} = 10 Vdc, I _D = 7.5 Adc)	rDS(on)		0.15	Ohm
Drain-Source On-Voltage (VGS = (ID = 15 Adc) (ID = 7.5 Adc, TJ = 100°C)		V _{DS} (on)	HO SOUNCE VOLT	2.6 1.3	Vdc
Forward Transconductance (VDS		9FS	4	_	mhos
RAIN-TO-SOURCE AVALANCHE ST	RESS CAPABILITY				
$(I_D = 18 \text{ A}, V_{DD} = 6 \text{ V}, T_C = 29 \text{ A})$	nergy See Figures 14 and 15 5°C, Single Pulse, Non-repetitive) 5°C, P.W. ≤ 200 µs, Duty Cycle ≤ 1%) 0°C, P.W. ≤ 200 µs, Duty Cycle ≤ 1%)	WDSR	- y 20 U	35 55 22	mJ
YNAMIC CHARACTERISTICS	Am 85.0 = gl - 8.1 8	Seon	7354		
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 16	Ciss	17/1	600	pF
Output Capacitance		Coss	1//-	400	
Reverse Transfer Capacitance		C _{rss}	1	100	
WITCHING CHARACTERISTICS* (T	J = 100°C)				
Turn-On Delay Time		td(on)	-\	50	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r	+ ///	150	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 14 and 15	td(off)	+ 1	200	
Fall Time	0 03- 4 01	8 tf	3 - 5	100	0
Total Gate Charge	(VDS = 0.8 Rated VDSS,	Qg	15 (Typ)	35	nC
Gate-Source Charge	I_D = Rated I_D , V_{GS} = 10 V)	Qgs	6 (Typ)	Piguro 3. 1	159.
Gate-Drain Charge	See Figures 17 and 18	Q_{gd}	9 (Typ)	_	
OURCE DRAIN DIODE CHARACTER	RISTICS*				
Forward On-Voltage	(I _S = 0.5 Rated I _D	V _{SD}	1.2 (Typ)	1.6	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray inc	luctance
Reverse Recovery Time	V01 = 20V	t _{rr}	70 (Typ)	90	ns
NTERNAL PACKAGE INDUCTANCE	(TO-204)		3"001		
Internal Drain Inductance (Measured from the contact screeto to the source pin and the center		Ld	5 (Typ)		nH
Internal Source Inductance (Measured from the source pin, to the source bond pad)	0.25" from the package	L _S	12.5 (Typ)		
NTERNAL PACKAGE INDUCTANCE	(TO-220)				
Internal Drain Inductance (Measured frrom the contact scr		L _d	3.5 (Typ)	TI,	nH
Internal Source Inductance	0.25" from package to center of die)	L _s	4.5 (Typ) 7.5 (Typ)	igi	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

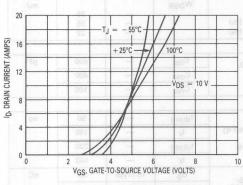
TYPICAL ELECTRICAL CHARACTERISTICS 11 2011 SHEETOARAHO JAQUITO 219



1.1 VDS = VGS | VD

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



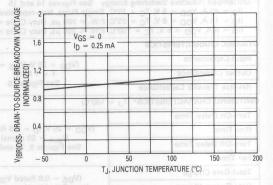
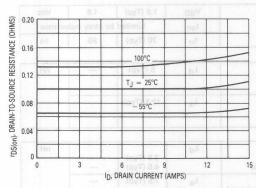


Figure 3. Transfer Characteristics





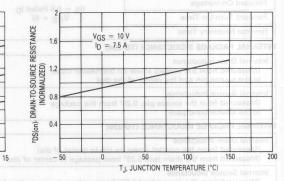


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

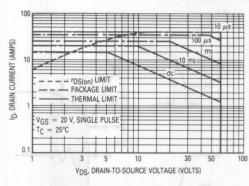


Figure 7. Maximum Rated Forward Biased Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

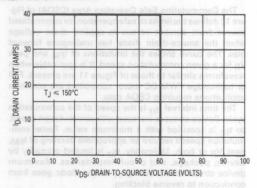


Figure 8. Maximum Rated Switching

The power averaged over a complete switching cycle must be less than:



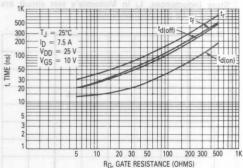
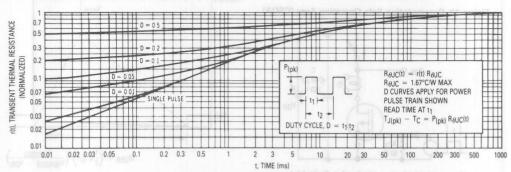


Figure 9. Resistive Switching Time versus
Gate Resistance



amolevsM polishtw2 systement begins and Figure 10. Thermal Response

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of IFM and peak VR for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval tfrr is the speed of the commutation cycle. Device stresses increase with commutation speed, so tfrr is specified with a minimum value. Faster commutation speeds require an appropriate derating of IFM, peak VR or both. Ultimately, tfrr is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during trr as the diode goes from conduction to reverse blocking.

VDS(pk) is the peak drain-to-source voltage that the device must sustain during commutation; IFM is the maximum forward source-drain diode current just prior to the onset of commutation.

VR is specified at 80% of V(BR)DSS to ensure that the CSOA stress is maximized as IS decays from IRM to zero.

RGS should be minimized during commutation. TJ has only a second order effect on CSOA.

Stray inductances, Li in Motorola's test circuit are assumed to be practical minimums.

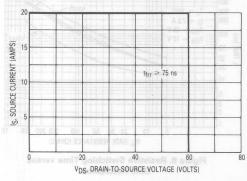


Figure 12. Commutating Safe Operating Area (CSOA)

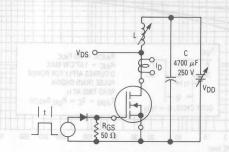


Figure 14. Unclamped Inductive Switching **Test Circuit**

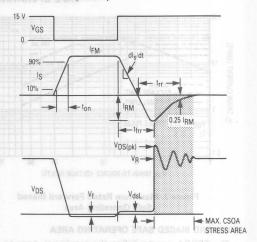


Figure 11. Commutating Waveforms

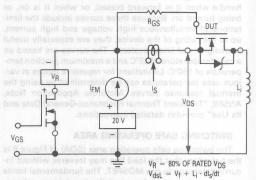


Figure 13. Commutating Safe Operating Area **Test Circuit**

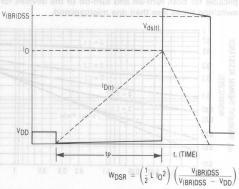


Figure 15. Unclamped Inductive Switching Waveforms

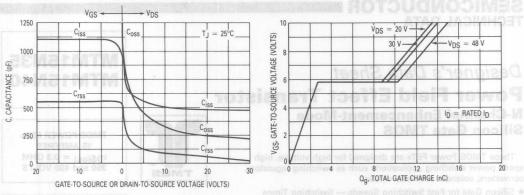
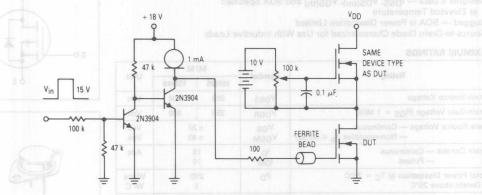


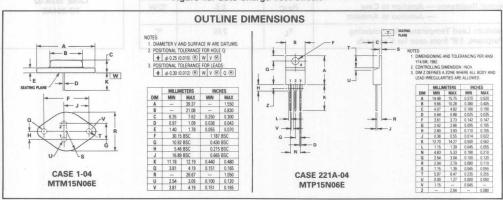
Figure 16. Capacitance Variation

Figure 17. Gate Charge versus Gate-to-Source Voltage



 $V_{in} = 15 V_{pk}$; PULSE WIDTH $\leq 100 \ \mu s$, DUTY CYCLE $\leq 10\%$

Figure 18. Gate Charge Test Circuit



Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

Pating	0	M	U S	
Rating	Symbol	15N35	15N40	Unit
Drain-Source Voltage	V _{DSS}	350	400	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	350	400	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	I _D		5	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		50	Watts W/°C
Operating and Storage Temperature Range	TJ, Tstq	-65 1	to 150	°C

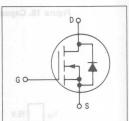
THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	R _θ JC	0.5	°C/W
— Junction to Ambient	RθJA	30	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

MTM15N35 MTM15N40



TMOS POWER FETS 15 AMPERES rDS(on) = 0.3 OHM 350 and 400 VOLTS





CASE 197A-02 TO-204AE

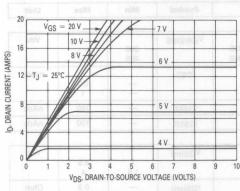
CASE 1-04 MITMISMOSE

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL	CHARACTERISTICS	(Tc = 25°C unless otherwise noted)

Cha	racteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS			LXX	V dS =	2DV
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	MTM15N35 MTM15N40	V(BR)DSS	350 400	A 01	Vdc
Zero Gate Voltage Drain Current $(V_{DS} = Rated V_{DSS}, V_{GS} = 0)$ $(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0)$	0, T _J = 125°C)	IDSS	-	0.2	mAdc
Gate-Body Leakage Current, Forwa	ard (V _{GSF} = 20 Vdc, V _{DS} = 0)	IGSSF	1 - 1	100	nAdc
Gate-Body Leakage Current, Rever	se (V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR	- 1	100	nAdc
N CHARACTERISTICS*	8.0 8				- PALE
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C	0 25 37 01	VGS(th)	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	(V _{GS} = 10 Vdc, I _D = 7.5 Adc)	rDS(on)	_	0.3	Ohm
Drain-Source On-Voltage ($V_{GS} = (I_D = 15 \text{ Adc})$ ($I_D = 7.5 \text{ Adc}$, $T_J = 100^{\circ}\text{C}$)	10 V)	V _{DS(on)}	- Hegion Chi	gure.r. u	Vdc
Forward Transconductance (VDS	= 15 V, I _D = 7.5 A)	9FS	6	_	mhos
YNAMIC CHARACTERISTICS		Total Visia	AV I I		
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 11	Ciss		3000	pF
Output Capacitance		Coss	1/1/2012 - 5	500	
Reverse Transfer Capacitance		C _{rss}	V V-	200	
WITCHING CHARACTERISTICS* (T	J = 100°C)		N.W.		
Turn-On Delay Time	59	t _{d(on)}	14	60	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r	1 4/1	180	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	1 -//	450	
Fall Time	8.0	t _f		180	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Qg	110 (Typ)	160	nC
Gate-Source Charge	I_D = Rated I_D , V_{GS} = 10 V)	Qgs	50 (Typ)	Y-STAD GOV	
Gate-Drain Charge	See Figure 12	Qgd	60 (Typ)	_	
OURCE DRAIN DIODE CHARACTER	ISTICS*	eterlatics	ransfer Chare		
Forward On-Voltage	(I _S = Rated I _D	V _{SD}	1.3 (Typ)	1.6	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray inc	luctance
Reverse Recovery Time	- 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	t _{rr}	1200 (Typ)		ns
ITERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screeto the source pin and the center		Ld	5 (Typ)		nH
Internal Source Inductance (Measured from the source pin, to the source bond pad)	0.25" from the package	L _S	12.5 (Typ)		

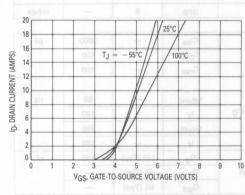
TYPICAL ELECTRICAL CHARACTERISTICS 1 801T888TOARAND JAOISTO BER



1.1 VDS = VGS VGS VD = 1 mA VDS = VGS VD = 1 mA VDS = VGS VD = 1 mA VDS = VDS VD = 1 mA VDS VD = 1 m

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation With Temperature



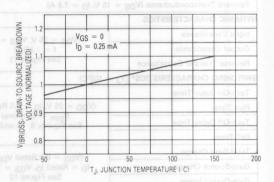
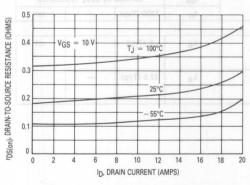


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation With Temperature



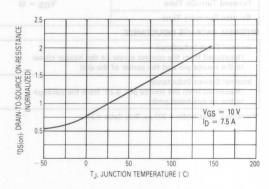


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

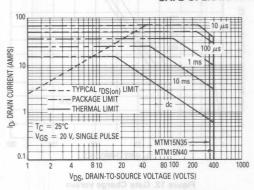


Figure 7. Maximum Rated Forward Biased Safe Operating Area

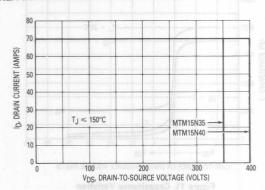


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

RG, GATE RESISTANCE (OHMS)

Figure 9. Resistive Switching Time Variation
With Gate Resistance

300 500

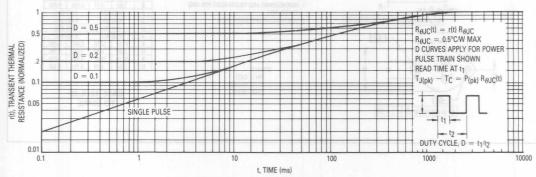


Figure 10. Thermal Response

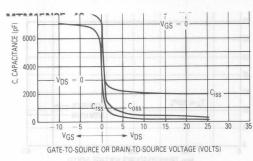


Figure 11. Capacitance Variation

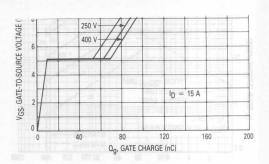


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

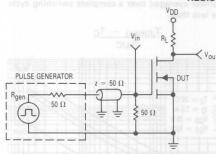


Figure 13. Switching Test Circuit

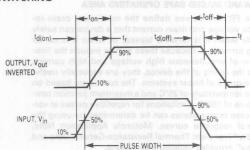
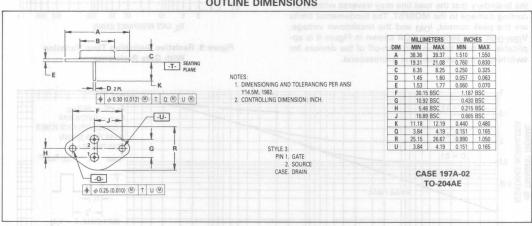


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

ad Mare — sel	0	= 80V M	11-14	
Rating	Symbol	15N45	15N50	Unit
Drain-Source Voltage	V _{DSS}	450	500	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	450	500	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}		20 40	Vdc Vpk
Drain Current — Continuous — Pulsed	IDM	bris 61 .61	5 5	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	250		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150		°C

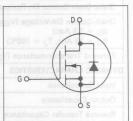
THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	R _θ JC R _θ JA	0.5	°C/W
Maximum Lead Temperature for Soldering	TL	275	°C
Purposes, 1/8" from case for 5 seconds			





TMOS POWER FETS 15 AMPERES rDS(on) = 0.4 OHM 450 and 500 VOLTS





CASE 197A-02 TO-204AE

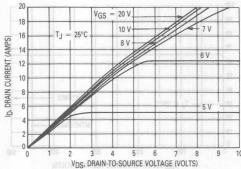
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Characteristic			Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)		MTM15N45 MTM15N50	V _{(BR)DSS}	450 500	r's_Da	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0 (VDS = 0.8 Rated VDSS, VGS		125°C)	IDSS	d Eff	0.2 1	mAdc
Gate-Body Leakage Current, Forw	vard (VGS	$F = 20 \text{ Vdc}, V_{DS} = 0)$	IGSSF	300	100	nAdc
Gate-Body Leakage Current, Reve	erse (VGSF	$R = 20 \text{ Vdc}, V_{DS} = 0)$	IGSSR	_	100	nAdc
N CHARACTERISTICS*	I I III	ge, high	d for high volta	s are designe	Power FET	ap VV gs
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C	BON	regulators. Times	VGS(th)	2 75	4.5	SbV (S) ters, sole on Gate
Static Drain-Source On-Resistanc	e (V _{GS} =	10 Vdc, I _D = 7.5 Adc)	rDS(on)	_	0.4	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 7.5 Adc) (I _D = 15 Adc, T _J = 100°C)			VDS(on)	VDS(en), VI Ire Diss <u>in</u> etion	6 5.8	Vdc
Forward Transconductance (VDS	= 15 V, I _[o = 7.5 A)	9FS	4	J spoid m	mhos
YNAMIC CHARACTERISTICS					9151140	TAS BEIN
Input Capacitance		$(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz})$	Ciss	_	3000	pF
Output Capacitance	tint		Coss	_	500	
Reverse Transfer Capacitance	SKW	See Figure 11	C _{rss}	_	200	V serios?
WITCHING CHARACTERISTICS* (ГJ = 100°	C) 088 088	anV V	(DM)	= 0.081 en	Care Velts
Turn-On Delay Time	No.V	00-	td(on)	200000	60	ns
Rise Time	(V	DD = 25 V, ID = 0.5 Rated ID	(t _r 02 >	gt) sv ist regen-	180	
Turn-Off Delay Time	ploA	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	-	450	Current -
Fall Time			ACI t _f	_	180	
Total Gate Charge	20000	(VDS = 0.8 Rated VDSS,	Qg	110 (Typ)	160	nC
Gate-Source Charge	59 1	D = Rated ID, VGS = 10 V)	Qgs	50 (Typ)	enaT Roscot	bris node
Gate-Drain Charge		See Figure 12	Q _{gd}	60 (Typ)	TRIBET TAR	AND IND
OURCE DRAIN DIODE CHARACTE	RISTICS*	20		and out mail	nout - non	etalanti bee
Forward On-Voltage		(Is = Rated ID	V _{SD}	1.1 (Typ)	1.4	Vdc
Forward Turn-On Time	D°	1/ 0)	ton	Limited	by stray ind	luctance
Reverse Recovery Time			t _{rr}	1200 (Typ)	from page.	ns
NTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L _d	5 (Typ)	_	nH	
Internal Source Inductance (Measured from the source pin to the source bond pad)	, 0.25" fro	m the package	L _S	12.5 (Typ)	-	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS



- 50 25 50

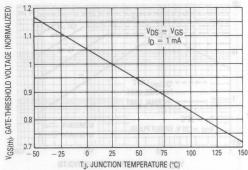
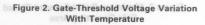
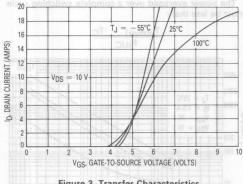


Figure 1. On-Region Characteristics





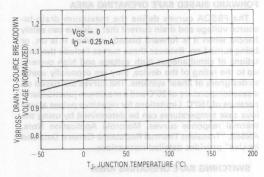
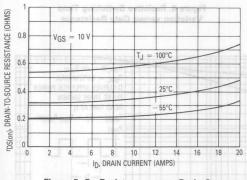


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation With Temperature



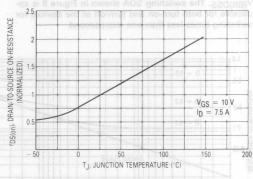


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

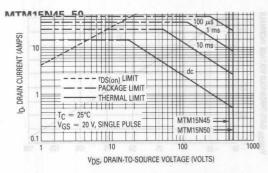


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

90 80 70 60 60 30 T_J ≤ 150°C MTM15N50 20 10 0 100 200 300 400 500 V_{DS}, DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

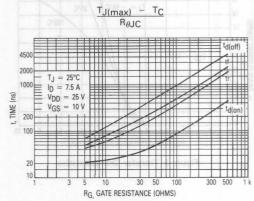


Figure 9. Resistive Switching Time Variation versus Gate Resistance

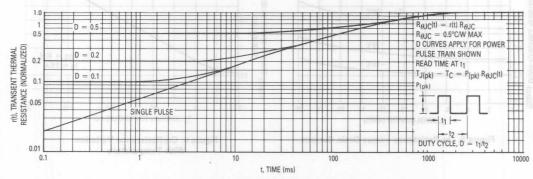


Figure 10. Thermal Response

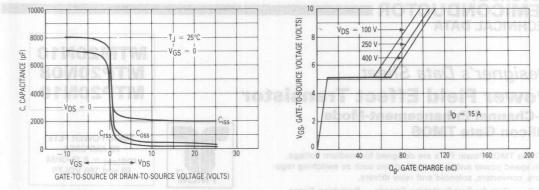


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

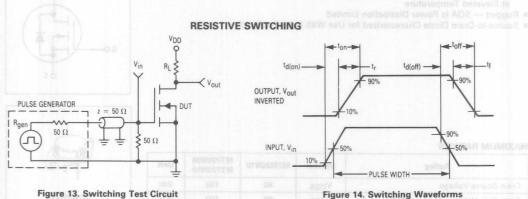
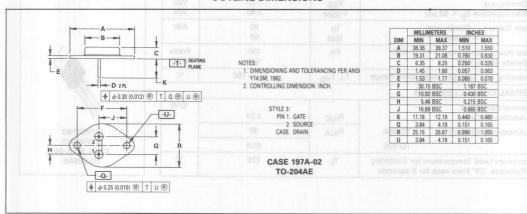


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

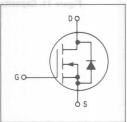
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS 20 AMPERES rDS(on) = 0.15 OHM 80 and 100 VOLTS



MAXIMUM RATINGS

Rating	Symbol	MTM20N10	MTP20N08 MTP20N10	Unit
Drain-Source Voltage	V _{DSS}	80	100	Vdc
Drain-Gate Voltage (R _{GS} = 1 M Ω)	VDGR	80	100	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	20 60		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	100 0.8		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	「J, T _{stg} −65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		$R_{ heta JC}$	### 1.25	°C/W
Junction to Ambient	TO-204	$R_{\theta JA}$	30	
	TO-220		62.5	R
Maximum Lead Temperatu Purposes, 1/8" from case		TL S	100 Head 275	°C



MTM20N10 CASE 1-04 TO-204AA



MTP20N08 MTP20N10 CASE 221A-04 TO-220AB

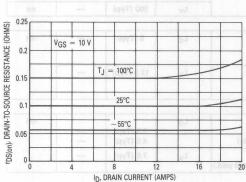
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

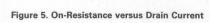
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

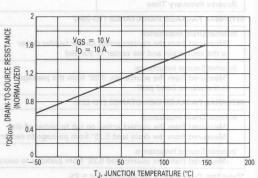
Characte	Characteristic		Min	Max	Unit
OFF CHARACTERISTICS	Day Inc.				0.5
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)	MTP20N08 MTM/MTP20N10	V _{(BR)DSS}	80 100	20 V	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ =	125°C)	IDSS	=	10 100	μAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	IGSSF		100	nAdc
Gate-Body Leakage Current, Reverse (\	/GSR = 20 Vdc, V _{DS} = 0)	IGSSR		100	nAdc
ON CHARACTERISTICS*		V8		1	
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C	10 8 Dest =	VGS(th)	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (VG	S = 10 Vdc, I _D = 10 Adc)	rDS(on)	IN 30RUGA-01-M	0.15	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V (I _D = 20 Adc) (I _D = 10 Adc, T _J = 100° C)		V _{DS(on)}	noig a rl-nO	3.6	Vdc
Forward Transconductance (V _{DS} = 15		9FS	6	_	mhos
DYNAMIC CHARACTERISTICS	. 19				
Input Capacitance	(Vp. = 25 V Vc. = 0	Ciss		1200	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	= 17-	600	
Reverse Transfer Capacitance	See Figure 11	C _{rss}		200	1 01
SWITCHING CHARACTERISTICS* (TJ =	100°C)	2°801 - A\\			
Turn-On Delay Time		td(on)		50	ns
Rise Time	$(V_{DD} = 25 \text{ V}, I_{D} = 0.5 \text{ Rated } I_{D}$	tr		450	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)		100	
Fall Time	1 1 1 1 8	tf	X-1	200	1
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Qg	28 (Typ)	50	nC
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 V)	Qgs	15 (Typ)		
Gate-Drain Charge (ASSM) NOTONOL T	See Figure 12	Q _{gd}	13 (Typ)	Vos. GATI	
SOURCE DRAIN DIODE CHARACTERISTI	CS*				
Forward On-Voltage	(I _S = Rated I _D	V _{SD}	1.8 (Typ)	3.6	Vdc
Forward Turn-On Time	$V_{GS} = 0$	ton	Limited	by stray ind	uctance
Reverse Recovery Time		t _{rr}	300 (Typ)	_	ns
NTERNAL PACKAGE INDUCTANCE (TO-	204)				7 7 65
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		Ld	5 (Typ)	GS = 10 A	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L _S	12.5 (Typ)	UT -	ō)
NTERNAL PACKAGE INDUCTANCE (TO-	220)		0.00		
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L _d	3.5 (Typ) 4.5 (Typ)		nH
Internal Source Inductance (Measured from the source lead 0.25				-	0

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS VGS(th), GATE THRESHOLD VOLTAGE (NORMALIZED) VGS = 20 V $V_{DS} = V_{GS}$ $I_{D} = 1 \text{ mA}$ ID, DRAIN CURRENT (AMPS) 12 7 V 0.9 6 V $T_J = 25^{\circ}C$ 5 V 25 50 75 100 - 25 -50VDS, DRAIN-TO-SOURCE VOLTAGE (VOLTS) TJ, JUNCTION TEMPERATURE (°C) Figure 2. Gate-Threshold Voltage Variation Figure 1. On-Region Characteristics With Temperature V(BR)DSS, DRAIN-TO-SOURCE BREAKDOWN VOLTAGE (NORMALIZED) 20 $V_{GS} = 0$ $I_{D} = 0.25 \text{ mA}$ $V_{DS} = 10 V$ TJ = --55°C 25°C DRAIN CURRENT (AMPS) - 100°C 0.8 ò 0.4 0L 100 -50 50 VGS, GATE-TO-SOURCE VOLTAGE (VOLTS) TJ, JUNCTION TEMPERATURE (°C) Figure 3. Transfer Characteristics Figure 4. Breakdown Voltage Variation With Temperature 0.25 VGS = 10 V







125

150

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

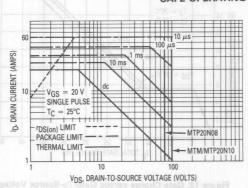


Figure 7. Maximum Rated Forward Biased Safe Operating Area

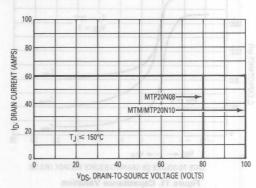


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

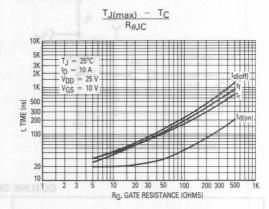


Figure 9. Resistive Switching Time versus
Gate Resistance

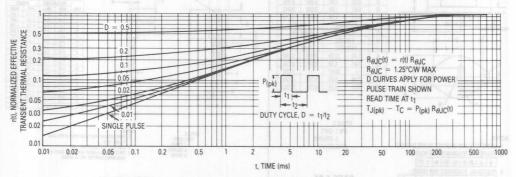


Figure 10. Thermal Response



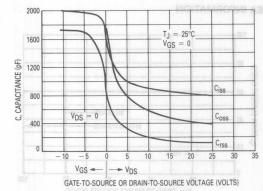


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

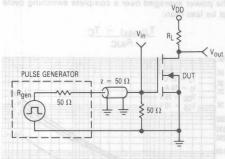


Figure 13. Switching Test Circuit

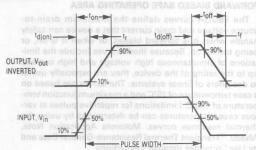
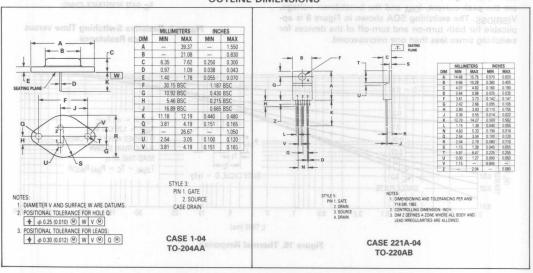


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

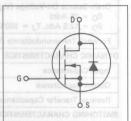
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
 A B ST = Of War = 200





TMOS POWER FETS
25 AMPERES
rDS(on) = 0.08 OHM
50 and 60 VOLTS



MAXIMUM RATINGS

Part of the Part of	88	MTM	I I with	
Rating (gvT) 88	Symbol	25N05	25N06	Unit
Drain-Source Voltage	V _{DSS}	50	60	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	50	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 0 = ± 40		Vdc Vpk
Drain Current — Continuous (QVT) (QUE) — Pulsed	I _D	25 80		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	100		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150		°C ∘

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		$R_{\theta JC}$	1.25	°C/W
Junction to Ambient	TO-204	R_{θ} JA	30	1002-0417
	TO-220		(alb 62.5 map of d	a) no wen
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		T _L telb to	275	°C



MTM25N05 MTM25N06 CASE 1-04 TO-204AA



MTP25N05 MTP25N06 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

	Characteristi	ic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS							
Drain-Source Breakdown Vo (VGS = 0, I _D = 0.25 mA)	Itage	MTM/MTP MTM/MTP		V _(BR) DSS	50 60	10 E 1	Vdc
Zero Gate Voltage Drain Cur (VDS = Rated VDSS, VGS (VDS = Rated VDSS, VGS	(= 0)	5°C)	ens'	IDSS	11 <u>3</u> b	10 100	μAdc
Gate-Body Leakage Current,	Forward (VGS	SF = 20 Vdc, V _{DS} = 0)	- 8	IGSSF	emeane	100	nAdc
Gate-Body Leakage Current,	Reverse (VGS	R = 20 Vdc, V _{DS} = 0)		IGSSR	201	100	nAdc
ON CHARACTERISTICS*			ald aveile			W. 10	make a see
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C	.,\	,eace,	aluger go	VGS(th)	2 1.5	4.5	Vdc
Static Drain-Source On-Resis	stance (VGS =	10 Vdc, ID = 12.5 Add	c)	rDS(on)	ando Buman	0.08	Ohm
Drain-Source On-Voltage (Voltage (Voltage (Voltage (ID = 25 Adc) (ID = 12.5 Adc, TJ = 100°)		bell	OA Speci	V _{DS(on)}	VDS(on): V	2.4	Vdc
Forward Transconductance		n = 12.5 A) sheed s	n inductiv	9FS	6 5 6	ain Dade C	mhos
DYNAMIC CHARACTERISTICS				01.0			
Input Capacitance				Ciss	_	1000	pF
Output Capacitance		(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 11		Coss	_	600	
Reverse Transfer Capacitano	e			C _{rss}	_	300	
SWITCHING CHARACTERISTIC		°C)		100			
Turn-On Delay Time				td(on)	_	50	ns
Rise Time	(V	DD = 25 V, ID = 0.5 R	lated ID	t _r	_	450	
Turn-Off Delay Time		R _{gen} = 50 ohms See Figures 9, 13 and	114	td(off)	_	100	
Fall Time		occ rigaros e, re un		tf	_	200	
Total Gate Charge		(V== 0.9 Pated V=		Qq	60 (Typ)	150	nC
Gate-Source Charge	riptr .	$(V_{DS} = 0.8 \text{ Rated } V_{D})$ $I_{D} = \text{Rated } I_{D}, V_{GS} = 0.8 \text{ Rated } V_{D}$		Qgs	32 (Typ)	- Ratin	
Gate-Drain Charge		See Figure 12		Q _{gd}	28 (Typ)		1
SOURCE DRAIN DIODE CHAR	ACTERISTICS*	08 00	Reda			pgelio/	100 to 10
Forward On-Voltage		(Is = Rated Ip	NOCA	V _{SD}	1.4 (Typ)	2.5	Vdc
Forward Turn-On Time	XIIV	$V_{GS} = 0$	VGSM	ton	Limited	by stray ind	uctance
Reverse Recovery Time	alıA	25	al	t _{rr}	300 (Typ)	Continuos	ns
NTERNAL PACKAGE INDUCT	ANCE (TO-204)	08	Magi			besluff	
Internal Drain Inductance (Measured from the conta to the source pin and the			d9	Ld	5 (Typ)	issipation @ e 26°C	MewnH yods ers
Internal Source Inductance	nternal Source Inductance (Measured from the source pin, 0.25" from the package		L _S	12.5 (Typ)	ARACTERIS LENCE		
NTERNAL PACKAGE INDUCT	ANCE (TO-220)	65.7	DUEF			6560	OT BIDLION
Internal Drain Inductance (Measured from the conta (Measured from the drain			die)	Ld 102-00	3.5 (Typ) 4.5 (Typ)	medinA	nH
Internal Source Inductance (Measured from the source	e lead 0.25" fro	om package to source l	bond pad.)	L _S	7.5 (Typ)	18" fro m çuşu	rposes, 1

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

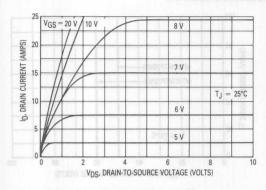


Figure 1. On-Region Characteristics

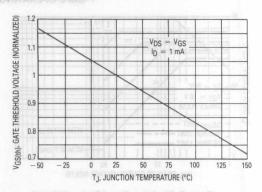


Figure 2. Gate-Threshold Voltage Variation With Temperature

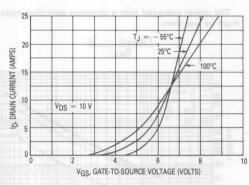


Figure 3. Transfer Characteristics

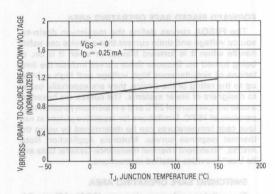


Figure 4. Breakdown Voltage Variation
With Temperature

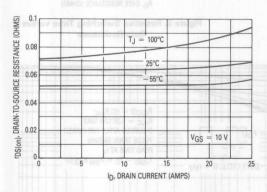


Figure 5. On-Resistance versus Drain Current

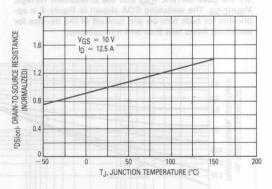


Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

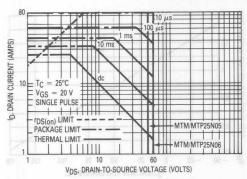


Figure 7. Maximum Rated Forward Biased Safe Operating Area

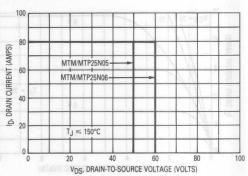


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

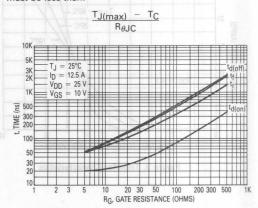


Figure 9. Resistive Switching Time versus
Gate Resistance

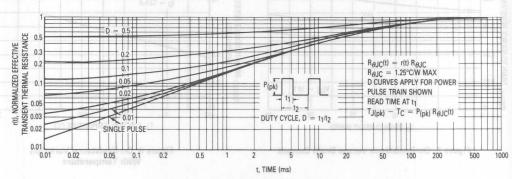


Figure 10. Thermal Response

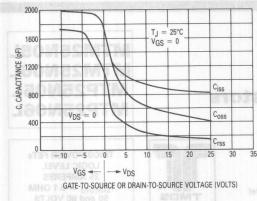


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-To-Source Voltage

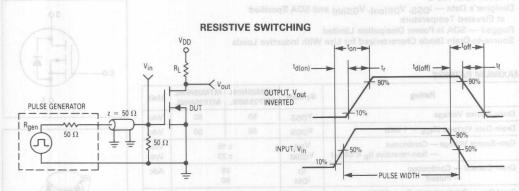
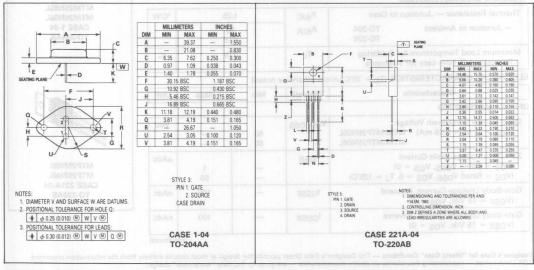


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — VGS(th) = 2 Volts max
- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

Rating	Symbol	MTM25N05L MTP25N05L	MTM25N06L MTP25N06L	Unit
Drain-Source Voltage	V _{DSS}	50	60	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	50	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 15 ± 20		Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	25 80		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	100 0.8		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case		$R_{\theta}JC$	1.25	°C/W
— Junction to Ambient	TO-204 TO-220	R_{θ} JA	30 62.5	1951 34 AU. 2014 AM 12514 AM 1
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

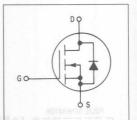
Characteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS			20 CAD 5751	KI
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA) MTM/MTP25N05L MTM/MTP25N06L	V _{(BR)DSS}	50 60		Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, T_J = 125°C)	IDSS	=	1 50	μAdc
Gate-Body Leakage Current, Forward (VGSF = 15 Vdc, VDS = 0)	IGSSF		100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 15 Vdc, VDS = 0)	IGSSR	-	100	nAdc

(continued)

MTM25N05L MTM25N06L MTP25N05L MTP25N06L



TMOS POWER FETS LOGIC LEVEL 25 AMPERES rDS(on) = 0.1 OHM 50 and 60 VOLTS





MTM25N05L MTM25N06L CASE 1-04 TO-204AA



MTP25N05L MTP25N06L CASE 221A-04 TO-220AB

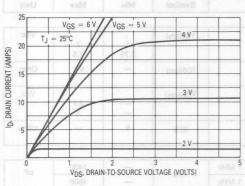
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS		TI	/Ven = 5.V	Vac = 6V	The second
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) (T _{.J} = 100°C)	u §	V _{GS(th)}	1 0.75	2 1.5	Vdc
Static Drain-Source On-Resistance (VGS = 5 Vdc, ID = 12.5 Adc)		rDS(on)	-	0.1	Ohm
Drain-Source On-Voltage (V _{GS} = 5 V) (I _D = 25 Adc) (I _D = 12.5 Adc, T _J = 100°C)		V _{DS(on)}		2.7	Vdc
Forward Transconductance (Vps = 15 V, lp = 12.5 A)	010 5	9FS	9		mhos
DYNAMIC CHARACTERISTICS	00.0 8				TA
Input Capacitance	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	C _{iss}	S ON SOUTH	1400	pF
	V _{GS} = 15 V, V _{DS} = 0, f = 1 MHz		_	4800	
Reverse Transfer Capacitance	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	C _{rss}	io noi gs A-ni	250	pF
	V _{GS} = 15 V, V _{DS} = 0, f = 1 MHz		_	4000	
Output Capacitance	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz)	Coss	_	750	pF
SWITCHING CHARACTERISTICS (TJ	= 100°C)		- TAW		251
Turn-On Delay Time	(V _{DD} = 25 V, I _D = 12.5 A, V _{GS} = 5 V, R _{gen} = 50 ohms) See Figures 8 and 9	td(on)		50	ns DS
Rise Time		tr		300	
Turn-Off Delay Time		td(off)	- 1	300	
Fall Time	2 2400	tf		350	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = 25 A, V _{GS} = 5 Vdc)	Q_g	24 (Typ)	36	nC
Gate-Source Charge		Qgs	13 (Typ)	1 -	
Gate-Drain Charge	See Figures 6 and 10	Q _{gd}	11 (Typ)	1	
SOURCE DRAIN DIODE CHARACTER	IISTICS*			13/1	1 10
Forward On-Voltage	(I _S = Rated I _D , V _{GS} = 0) See Figures 14 and 15	V _{SD}	2.5 (typ)	- <u></u>	Vdc
Forward Turn-On Time		ton	50 (typ)	2_	ns
Reverse Recovery Time		t _{rr}	300 (typ)	NO SOV	ns
NTERNAL PACKAGE INDUCTANCE	(TO-204)	antulvatnova	Tennalis Ch	Flance 2	
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L _d	5 (Typ)	=	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L _S	12.5 (Typ)	T	0.14
NTERNAL PACKAGE INDUCTANCE	(TO-220)			F001 = 1T	
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L _d	3.5 (Typ) 4.5 (Typ)	2810	nH 80.0
nternal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)		Ls	7.5 (Typ)		







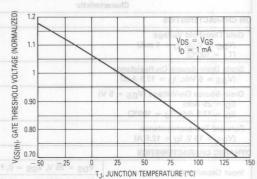
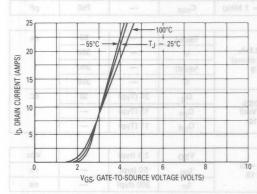


Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



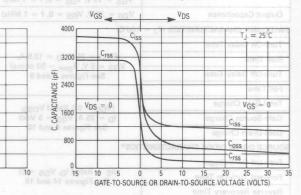
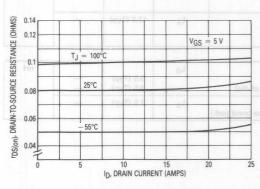


Figure 3. Transfer Characteristics

Figure 4. Capacitance Variation



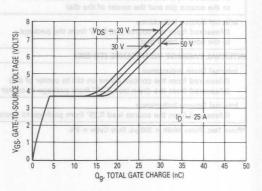


Figure 5. On-Resistance versus Drain Current

Figure 6. Gate Charge Variation

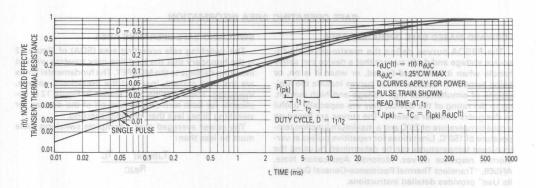
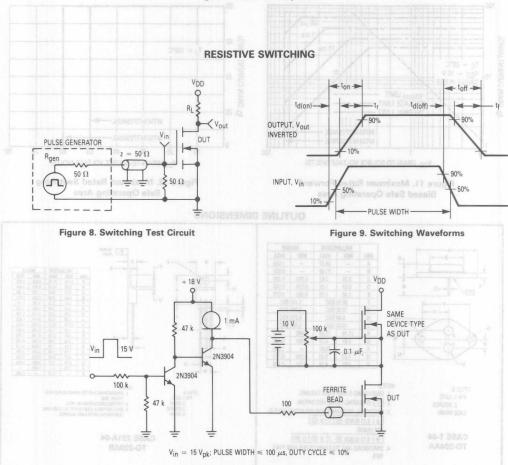


Figure 7. Thermal Response



MOTOROLA TMOS POWER MOSFET DATA

Figure 10. Gate Charge Test Circuit

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 12 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 12 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{\mathsf{T}\mathsf{J}(\mathsf{max}) - \mathsf{T}\mathsf{C}}{\mathsf{R}_{\theta}\mathsf{J}\mathsf{C}}$$

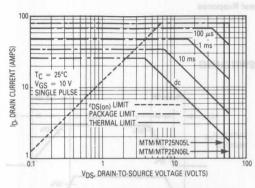


Figure 11. Maximum Rated Forward Biased Safe Operating Area

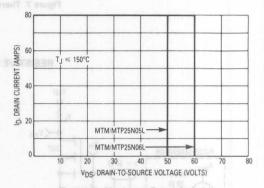
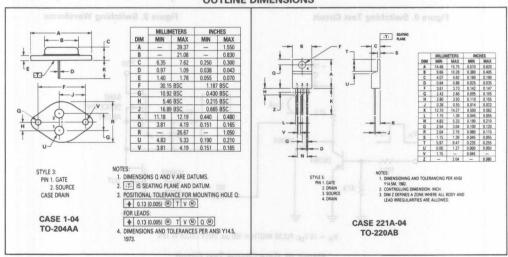


Figure 12. Maximum Rated Switching Safe Operating Area

OUTLINE DIMENSIONS



3

MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

This TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

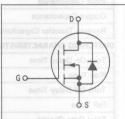
- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MTM40N20

TMOS POWER FET 40 AMPERES rDS(on) = 0.08 OHM 200 VOLTS



MAXIMUM RATINGS

Rating	Symbol	Value 0 = a	Unit
Drain-Source Voltage	VDSS	200	Vdc
Drain-Gate Voltage ($R_{GS} = 1 M\Omega$)	VDGR	200	Vdc
Gate-Source Voltage Continuous (tp \leq 50 μ s)	V _{GS} V _{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	40 200	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	250 2	Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta J A}$	0.5 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C



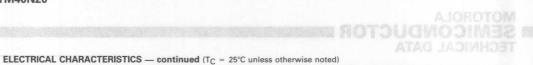
CASE 197A-02 TO-204AE

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
FF CHARACTERISTICS					
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA) MTM40N20	V(BR)DSS	200	-	Vdc	
Zero Gate Voltage Drain Current (Vps = Rated Vpss, Vgs = 0) (Vps = Rated Vpss, Vgs = 0, $T_J = 125^{\circ}C$)	IDSS	=	10 100	μAdc	
Gate-Body Leakage Current, Forward (V _{GSF} = 20 Vdc, V _{DS} = 0)	IGSSF	-	100	nAdd	
Gate-Body Leakage Current, Reverse (V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR	_	100	nAdd	

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



Characterist	tic	Symbol	Min	Max	Unit
ON CHARACTERISTICS*		100	d2 str	1 2'10	dois
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C	istor	VGS(th)	2 1.5	4.5	Vdc

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C	VGS(th)	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 20 Adc)	rDS(on)	meane	0.08	Ohm
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 40 \text{ Adc}$) ($I_D = 20 \text{ Adc}$, $T_J = 100^{\circ}\text{C}$)	V _{DS(on)}	NOS s destruned	3.8 3.2	Vdc
Forward Transconductance (VDS = 15 V, ID = 20 A)	ges alu	10	s su dous es s	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	Shurt Bo	C _{iss}	ade Buross	5500	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss and	Vostonie	1500	
Reverse Transfer Capacitance		C _{rss}	_ 81	500	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time		td(on)	_	60	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms) See Figures 13 and 14	tr	-	300	
Turn-Off Delay Time		td(off)	_	400	
Fall Time		tf	_	250	RR MUNRX
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V) See Figure 12	Ω_{g}	85 (Typ)	95	nC
Gate-Source Charge		Qgs	45 (Typ)	Sostio	rain-Source
Gate-Drain Charge		Q _{gd}	40 (Typ)	e acili ana	nV areD-nier

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage		V _{SD}	2.0 (Typ)	2.5	Vdc
Forward Turn-On Time	(I _S = Rated I _D , V _{GS} = 0)	ton	Limited by stray inductance		nce
Reverse Recovery Time	OBA GOO	t _{rr}	200 (Typ)	healig _	ns

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance	Ld	5 (Typ)	9.25°C-	vodenHateO
(Measured from the contact screw on the header closer to the source pin and the center of the die)			Storage Ten	berating and
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source	L _S	12.5 (Typ)	RACE - Jun	AMAL CHA
bond pad)				GISTAT TETTTE

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

	xsM		

3

TYPICAL ELECTRICAL CHARACTERISTICS

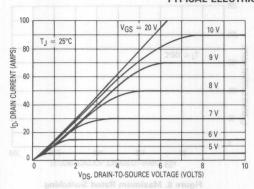


Figure 1. On-Region Characteristics

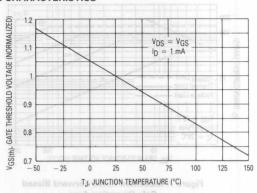


Figure 2. Gate-Threshold Voltage Variation With Temperature

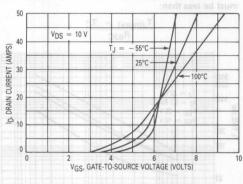


Figure 3. Transfer Characteristics

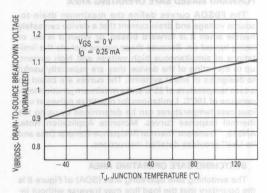


Figure 4. Breakdown Voltage Variation
With Temperature

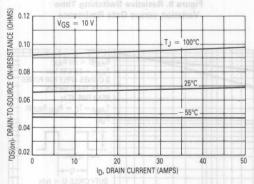


Figure 5. On-Resistance versus Drain Current

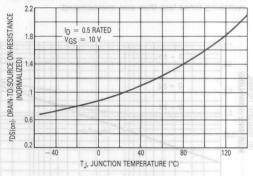


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

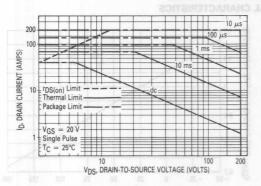


Figure 7. Maximum Rated Forward Biased Safe Operating Area

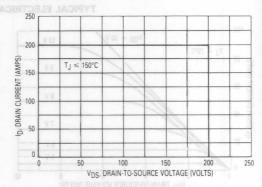


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V(\mbox{\footnotesize BR})_{\mbox{\footnotesize DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

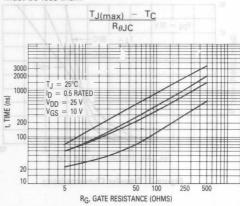


Figure 9. Resistive Switching Time Variation versus Gate Resistance

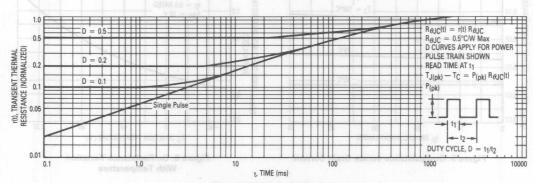
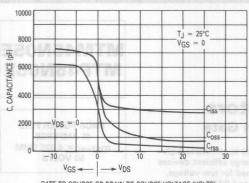


Figure 10. Thermal Response



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

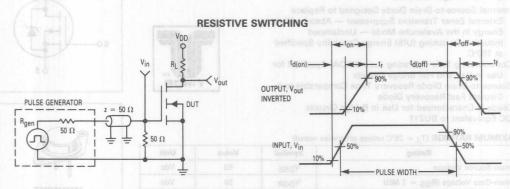
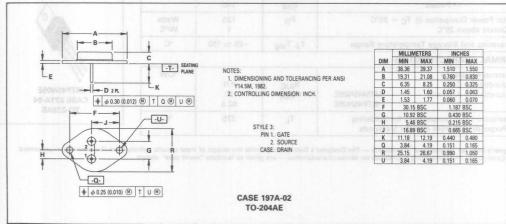


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

TMOS IV

Power Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- DC Equivalent to BUZ11

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	50	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous (T _C = 25°C) — Pulsed	I _{DM}	45 UO 145	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	125 1	Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stg}	-65 to 150	°C

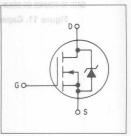
THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	MTM45N05E MTP45N05E	R_{θ} JC R_{θ} JA	1.0 30 62.5	© U D O T I
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		T _L	275	°C 11_)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MTM45N05E MTP45N05E

TMOS POWER FETS
45 AMPERES
rDS(on) = 0.035 OHM
50 VOLTS





TMOS

MTM45N05E CASE 197A-02 TO-204AE



MTP45N05E CASE 221A-04 TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristi	c	Symbol	Min	Max	Unit
FF CHARACTERISTICS		Ty = 25°C		1 -	loV]
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)		V(BR)DSS	50	71	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ = 125	5°C)	IDSS	=	10 100	μΑ
Gate-Body Leakage Current, Forward (VGS)		IGSSF	- 1	100	nAdo
Gate-Body Leakage Current, Reverse (VGSF	$R = 20 \text{ Vdc}, V_{DS} = 0)$	IGSSR	-	100	nAdd
N CHARACTERISTICS*				M	11 00
Gate Threshold Voltage (VDS = VGS, ID = 250 μ A) TJ = 100°C	8 000	VGS(th)	2.0 1.5	4 3.5	Vdc
Static Drain-Source On-Resistance (VGS =	10 Vdc, ID = 29 Adc)	rDS(on)	95. 10) 102.03 WAST	0.035	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 45 Adc) (I _D = 22.5 Adc, T _J = 100°C)		V _{DS(on)}	On-Region (1.5 0.9	Vdc
Forward Transconductance (V _{DS} = 15 V, I _I	o = 29 A)	9 _{FS}	17	_	mhos
RAIN-TO-SOURCE AVALANCHE CHARACTE	RISTICS				
	ngle Pulse, Non-repetitive) I. ≤ 45 μs, Duty Cycle ≤ 1%)	WDSR	=	50 110 40	mJ
YNAMIC CHARACTERISTICS	1 8 8 1 7 7	205			
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Ciss	+ 1	3000	pF
Output Capacitance		Coss	+ 1	1500	
Reverse Transfer Capacitance	See Figure 16	C _{rss}		400	
WITCHING CHARACTERISTICS* (TJ = 100°	C)				08
Turn-On Delay Time		td(on)	+ 1	25	ns
Rise Time	(V _{DD} = 25 V, I _D = 29 A R _{gen} = 4.7 ohms)	t _r		60	
Turn-Off Delay Time	See Figure 9	td(off)	-	70	
Fall Time (7) BRUTARBOMET MOTOMUL LT		tf Tov	GATE-TO-SOURCE	25	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Q_g	55 (Typ)	60	nC
	$I_D = Rated I_D, V_{GS} = 10 V)$	Qgs	30 (Typ)	_	
Gate-Drain Charge	See Figures 17 and 18	Q_{gd}	25 (Typ)	-	
OURCE DRAIN DIODE CHARACTERISTICS*					man avid
Forward On-Voltage	(Is = 46 A	V _{SD}	1.8 (Typ)	2.2	Vdc
Forward Turn-On Time	(I _S = 46 A V _{GS} = 0	ton	Limited	by stray ind	uctance
Reverse Recovery Time	$dig/dt = 100 A/\mu s)$	t _{rr}	200 (Typ)		ns
ITERNAL PACKAGE INDUCTANCE (TO-204)	1 58 1		J-001 =		100
Internal Drain Inductance (Measured from the contact screw on the to the source pin and the center of the d		L _d	5 (Typ)	-	nH 20.02
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L _S	12.5 (Typ)		10.0
ITERNAL PACKAGE INDUCTANCE (TO-220)	3				
Internal Drain Inductance (Measured from the contact screw on tak (Measured from the drain lead 0.25" from		Ld 85	3.5 (Typ) 4.5 (Typ)	25	nH
Internal Source Inductance (Measured from the source lead 0.25" from	om package to source bond pad.)	L _S	7.5 (Typ)	R-mO_2 sou	g/R

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

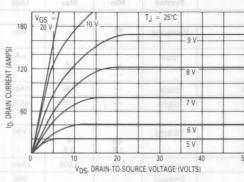


Figure 1. On-Region Characteristics

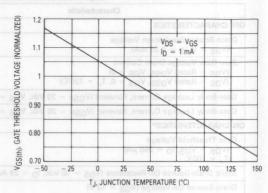
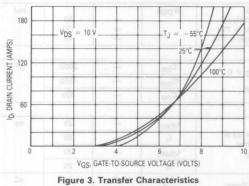


Figure 2. Gate-Threshold Voltage Variation With Temperature



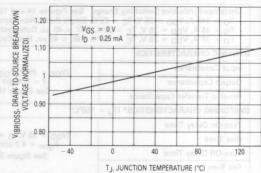


Figure 4. Breakdown Voltage Variation
With Temperature

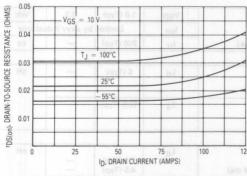


Figure 5. On-Resistance versus Drain Current

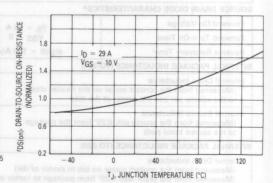


Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

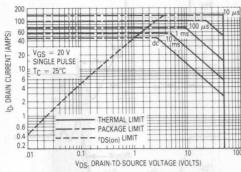


Figure 7. Maximum Rated Forward Bias Safe Operating Area

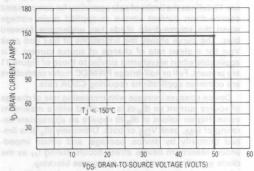


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

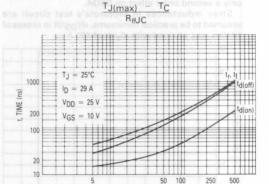


Figure 9. Resistive Switching Time Variation versus Gate Resistance

RG, GATE RESISTANCE (OHMS)

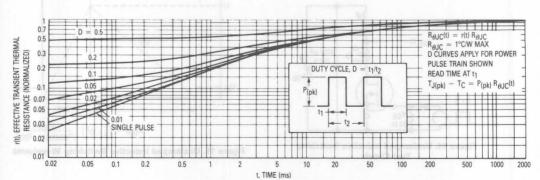


Figure 10. Thermal Response

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of IFM and peak VDS for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so $dl_{\rm S}/dt$ is specified with a maximum value. Higher values of $dl_{\rm S}/dt$ require an appropriate derating of $l_{\rm FM}$, peak $V_{\rm DS}$ or both. Ultimately $dl_{\rm S}/dt$ is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during $t_{\rm rr}$ as the diode goes from conduction to reverse blocking.

 $V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; IFM is the maximum forward source-drain diode current just prior to the onset of commutation.

 $V_{\mbox{\scriptsize R}}$ is specified at 80% of $V_{\mbox{\scriptsize (BR)DSS}}$ to ensure that the CSOA stress is maximized as IS decays from IRM to zero.

RGS should be minimized during commutation. TJ has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dl_{S}/dt of 400 A/ μ s.

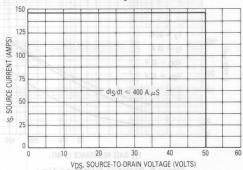


Figure 12. Commutating Safe Operating Area (CSOA)

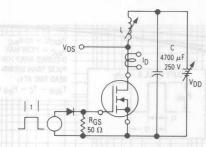


Figure 14. Unclamped Inductive Switching
Test Circuit

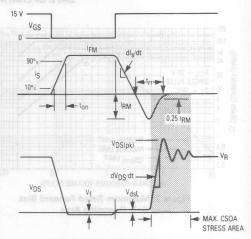


Figure 11. Commutating Waveforms

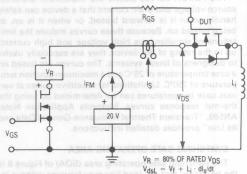


Figure 13. Commutating Safe Operating Area Test Circuit

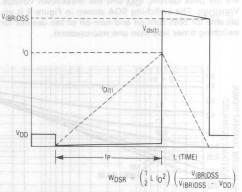
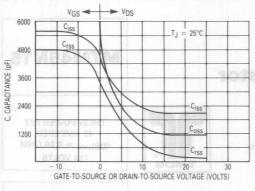


Figure 15. Unclamped Inductive Switching Waveforms



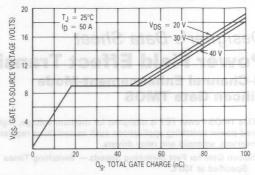
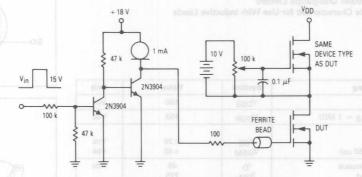


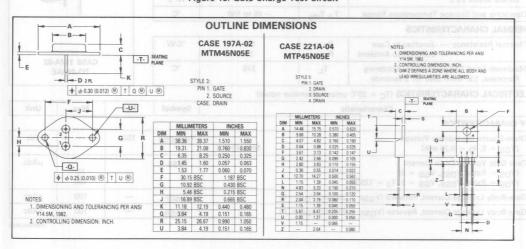
Figure 16. Capacitance Variation

Figure 17. Gate Charge versus Gate-to-Source Voltage



 $V_{in} = 15 V_{pk}$; PULSE WIDTH $\leq 100 \mu s$, DUTY CYCLE $\leq 10\%$

Figure 18. Gate Charge Test Circuit



Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

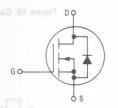
This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

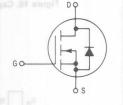
- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FET 45 AMPERES rDS(on) = 0.06 OHM 150 VOLTS





MAXIMUM RATINGS

3

Rating	Symbol	Value	Unit
Drain-Source Voltage	VDSS	150	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	150	Vdc
Gate-Source Voltage Continuous Non-repetitive $(t_p \le 50 \ \mu s)$	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	45 225	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	250 T op 185 2	Watts W/°C
Operating and Storage Temperature Range	TJ, Tstg	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	R_{θ} JC R_{θ} JA	0.5 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C



CASE 197A-02 TO-204AE

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

	Symbol	Min	Max	Unit
2004	RESTORAÇÃO I	1	VZ	
MTM45N15	V _{(BR)DSS}	150	Ø-1	Vdc
199.0 \$26.0 (970.0 \$46.0 229.782.1 528.065.0	IDSS	6 y r	10 100	μAdc
	IGSSF	-	100	nAdd
201 B 1814	IGSSR	SUL NU DAG	100	nAdd
	MTM45N15	MTM45N15 V(BR)DSS IDSS	MTM45N15	MTM45N15

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves - representing boundaries on device characteristics - are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS*			HA	
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C	VGS(th)	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 22.5 Adc)	rDS(on)		0.06	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 45 Adc) (I _D = 22.5 Adc, T _J = 100°C)	VDS(on)	=	3.24 2.7	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 22.5 A)	9FS	10	1 + 1	mhos
YNAMIC CHARACTERISTICS	8	à	8	
Input Capacitance	Ciss	MIDON BORDON	5500	pF

Input Capacitance	THE ST.	Ciss	SOURCE VOLTAGE	5500	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	_	1500	
Reverse Transfer Capacitance	-6189 77 91984	C _{rss}	PERSON MOISS	500	St. r

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time		td(on)	-	60	ns
Rise Time	$(V_{DD} = V, I_D = 0.5 \text{ Rated } I_D)$	t _r	1-1	300	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 13 and 14	td(off)		400	- anV
Fall Time		tf	- Tal- 1	250	000
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V) See Figure 12	Qg	85 (Typ)	95	nC
Gate-Source Charge		Qgs	45 (Typ)	-	
Gate-Drain Charge		Qgd	40 (Typ)	_	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage		V _{SD}	2 (Typ)	2.5	Vdc
Forward Turn-On Time	$(I_S = Rated I_D, V_{GS} = 0)$	ton	Limited by stray inductance		nce
Reverse Recovery Time	33 00	t _{rr}	200 (Typ)		ns

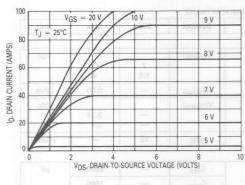
INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	Ld	5 (Typ)	Tree 3 Tree	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)	L _S	12.5 (Typ)	-	

^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS



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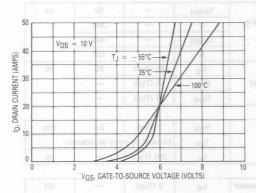
VDS = VGS
ID = 1 mA

VDS = VGS
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VDS =

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation With Temperature



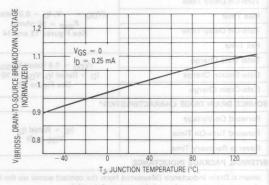
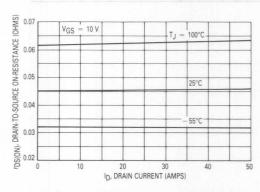


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation
With Temperature



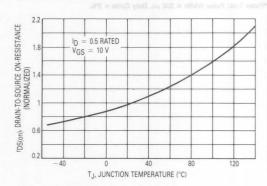


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation
With Temperature

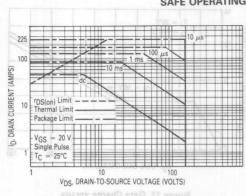


Figure 7. Maximum Rated Forward Biased Safe Operating Area

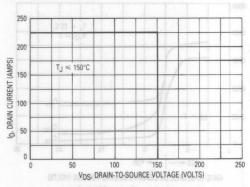


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

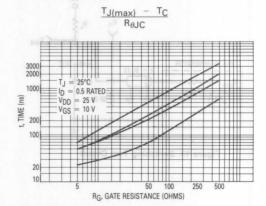


Figure 9. Resistive Switching Time Variation versus Gate Resistance

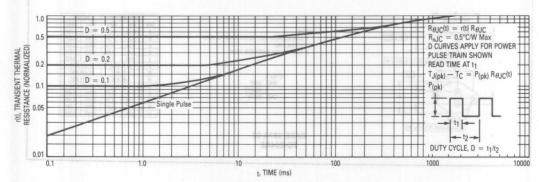
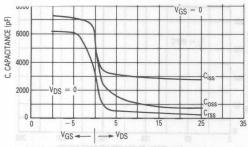


Figure 10. Thermal Response



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 11. Capacitance Variation

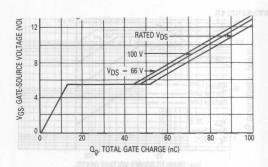


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

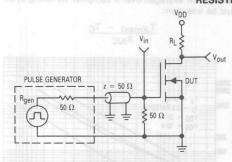


Figure 13. Switching Test Circuit

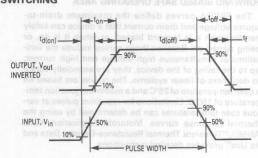


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

TMOS IV

Power Field Effect Transistors N-Channel Enhancement-Mode Silicon Gate

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- DC Equivalent to IRFZ40

MAXIMUM RATINGS (T = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	VDSS	amno 150 - napi	Vdc
Drain-Gate Voltage (R _{GS} = 1 MΩ)	VDGR	50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous (T _C = 25°C) — Pulsed	I _D	50 160	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	125 1	Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stg}	-65 to 150	°C

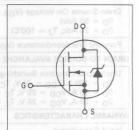
THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		$R_{\theta JC}$	1	°C/W
Junction to Ambient	MTM50N05E MTP50N05E	$R_{\theta}JA$	30 62.5	on the head
Maximum Lead Temperature Purposes, 1/8" from case for		TL	275	°C



TMOS POWER FETS
50 AMPERES

*DS(on) = 0.028 OHM
50 VOLTS





TMOS

MTM50N05E CASE 197A-02 TO-204AE



MTP50N05E CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

- Contract of the contract of	cteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS	M. C. III					
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)			V(BR)DSS	50		Vdc
Zero Gate Voltage Drain Current			IDSS	mo b.	10M C	μΑ
(VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0)	D. Tı = 125	°C)		_	10	30
Gate-Body Leakage Current, Forwar			IGSSF	3.3-70	100	nAdc
Gate-Body Leakage Current, Reverse		20 1 5 5 5 5 6 6 6 6 6 7 6	IGSSR	1115	100	nAdc
ON CHARACTERISTICS*		Silicon Gate	ebolvi-zn	nceme	tenna i	ennsi
Gate Threshold Voltage			V _{GS(th)}			Vdc
$(V_{DS} = V_{GS}, I_{D} = 250 \mu A)$ $T_{J} = 100^{\circ}C$			ower MOSFET ion modes. Th	1.5	3.5	idvanced in the avi
Static Drain-Source On-Resistance (III VYEWSTERS THE	I milw_aabo	0.028	Ohm
Drain-Source On-Voltage (VGS = 10	1100 100	rdc, ID = 23 Adc)	rDS(on)	id ni enolit	skilges gnid	Vdc
$(I_D = 50 \text{ Adc})$		VDS(on)	cutarly well	1.4	esc devic	
(ID = 25 Adc, IJ = 100 C)			area_are cl	1.3	Plow both	
Forward Transconductance (V _{DS} =			⁹ FS	17	d high of o	mhos
DRAIN-TO-SOURCE AVALANCHE CHA		118111	WDSR	Suppress	er Translent	emal Zen
Unclamped Inductive Switching Ene (ID = 160 A, VDD = 25 V, TC = 2	5°C. Single	rgy See Figures 14 and 15		Mode — I	erionalevA e	II nimJii
$(I_D = 50 \text{ A}, V_{DD} = 25 \text{ V}, T_C = 25 \text{ A})$	°C. P.W. ≤	35 µs. Duty Cycle ≤ 1%)	apability Spac	- 10.000	100	.000
(I _D = 20 A, V _{DD} = 25 V, T _C = 10	00°C, P.W. ≤	35 μs, Duty Cycle ≤ 1%)	SOA) Specific	ing Area (C	35	pnitsrue
DYNAMIC CHARACTERISTICS	801	AT BOL	Alderson and Dis	ge Uncurs	one no-tone	and-ole
Input Capacitance	(V	$DS = 25 \text{ V}, V_{GS} = 0,$	Coss	sboil	3000	pF
Output Capacitance		f = 1 MHz) See Figure 16		Use in Brit	1200	is Chara
Reverse Transfer Capacitance	400001		C _{rss}		400	jurvaleni
SWITCHING CHARACTERISTICS* (TJ	= 100°C)		otherwise noted	5°C unless a	MGS IT J = 1	ITAR MU
Turn-On Delay Time	(Vpp	= 25 V, I _D = 0.5 Rated I _D	td(on)	_	25	ns
Rise Time	Vdc	R _{gen} = 4.7 ohms)	V t _r	_	60	Source Vo
Turn-Off Delay Time	oloV"	See Figure 9		- COM	70	Sate Volte
Fall Time	650/	103 4.20	tf	80000	25	lov samo
Total Gate Charge	V) Vpk	DS = 0.8 Rated VDSS,	Qg	55 (Typ)	mg// 60	nC
Gate-Source Charge	obAD =	Rated ID, VGS = 10 V) see Figures 17 and 18	Q _{gs}	30 (Typ)	Commuous	- InemuS
Gate-Drain Charge		INC.	Ω_{gd}	25 (Typ)	Pasina	
SOURCE DRAIN DIODE CHARACTERIS	STICS*	130 IS		J:05 =	HOATION (E. T.C.	nevode et
Forward On-Voltage	(I	SD = 51 A, VGS = 0,	VSD	1.9 (Typ)	2.5	Vdc
Forward Turn-On Time		$dl_S/dt = 100 A/\mu s$	ton		d by stray inc	luctance
Reverse Recovery Time	157777		t _{rr}	(Typ)	250	ns
NTERNAL PACKAGE INDUCTANCE (1	O-204)	1 308			600	o nesista
Internal Drain Inductance (Measured from the contact screw to the source pin and the center of		oder closer		5 (Typ)	meldn	A or nHis
Internal Source Inductance (Measured from the source pin, 0 to the source bond pad)	.25" from th	e package	L _S	12.5 (Typ)	from case for	oses, 1/8
NTERNAL PACKAGE INDUCTANCE (T	O-220)	ics — are given to facilitate "wo	teviçe charecterisi	o no asinebnuo	epresenting be	t cakhes —
Internal Drain Inductance (Measured frrom the contact scre (Measured from the drain lead 0.2			L _d	3.5 (Typ) 4.5 (Typ)	=	nH
Internal Source Inductance (Measured from the source lead 0			L _S	7.5 (Typ)	_	

TYPICAL ELECTRICAL CHARACTERISTICS

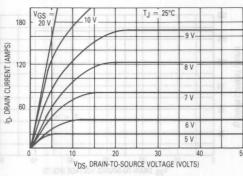


Figure 1. On-Region Characteristics

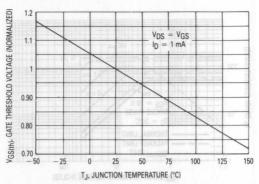


Figure 2. Gate-Threshold Voltage Variation With Temperature

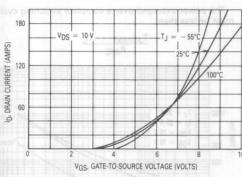
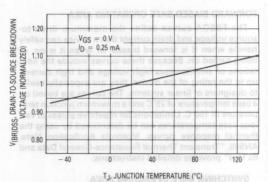


Figure 3. Transfer Characteristics





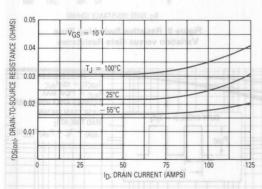


Figure 5. On-Resistance versus Drain Current

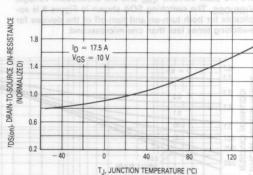


Figure 6. On-Resistance Variation With Temperature

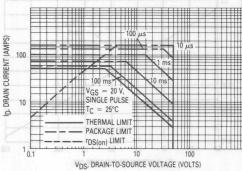


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

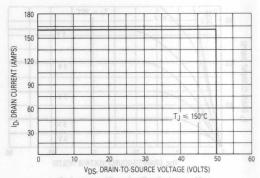


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

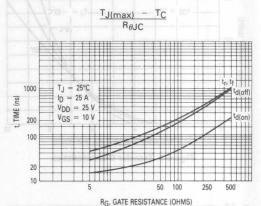


Figure 9. Resistive Switching Time Variation versus Gate Resistance

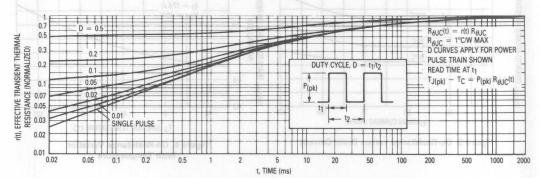


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so $dl_{\rm S}/dt$ is specified with a maximum value. Higher values of $dl_{\rm S}/dt$ require an appropriate derating of $l_{\rm FM}$, peak $V_{\rm DS}$ or both. Ultimately $dl_{\rm S}/dt$ is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during $t_{\rm rr}$ as the diode goes from conduction to reverse blocking.

VDS(pk) is the peak drain-to-source voltage that the device must sustain during commutation; IFM is the maximum forward source-drain diode current just prior to the onset of commutation.

 V_R is specified at 80% of $V_{\{BR\}DSS}$ to ensure that the CSOA stress is maximized as IS decays from I_{RM} to zero.

RGS should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dl_{S}/dt of 400 A/ μ s.

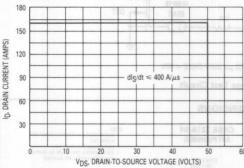


Figure 12. Commutating Safe Operating Area (CSOA)

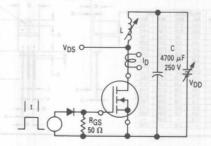


Figure 14. Unclamped Inductive Switching Test Circuit

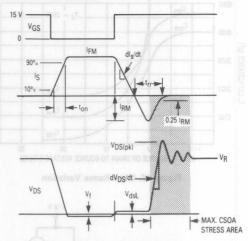


Figure 11. Commutating Waveforms

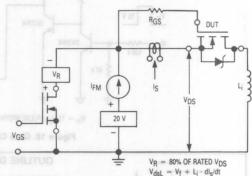


Figure 13. Commutating Safe Operating Area Test Circuit

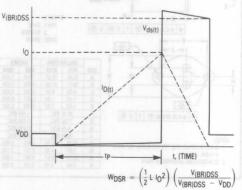


Figure 15. Unclamped Inductive Switching Waveforms

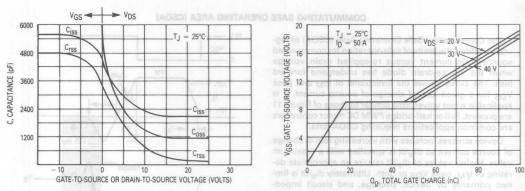


Figure 16. Capacitance Variation

Figure 17. Gate Charge versus Gate-to-Source Voltage

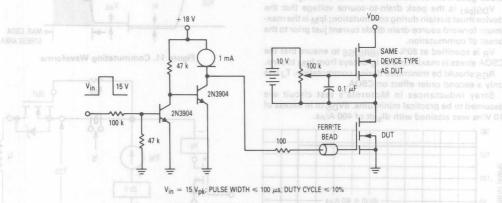
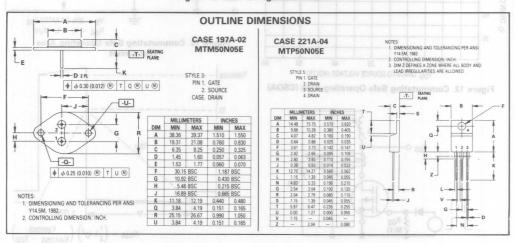


Figure 18. Gate Charge Test Circuit



MOTOROLA SEMICONDUCTOR **TECHNICAL DATA**

MTM60N06

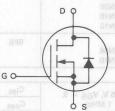
Designer's Data Sheet

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MAXIMUM RATINGS

			M	TM		
Rating	Symbol	60N05	60N06	55N08	55N10	Unit
Drain-Source Voltage	VDSS	50	60	80 0	100	Vdc
Drain-Gate Voltage (RGS = 1 MΩ)	VDGR	50	60	80	100	Vdc
Gate-Source Voltage Continuous Non-repetitive $(t_p \le 50 \ \mu s)$	V _{GS} V _{GSM}	± 20 . Sared = 0.8 Eared = 0.8 Eared = 0.8 Eared = 0.9				Vdc Vpk
Drain Current Continuous Pulsed	I _D	60 55 300 275		55	Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD PD	250 0 = 30V			Watts W/°C	
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	R _θ JC	0.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8"	TL	275 d soruce	ed) of eg°C a
from case for 5 seconds			

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.

55 and 60 AMPERE

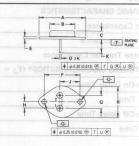
N-CHANNEL TMOS POWER FETs

rDS(on) = 0.04 OHM 80 and 100 VOLTS

rDS(on) = 0.028 OHM50 and 60 VOLTS

> MTM55N08 MTM55N10 MTM60N05 MTM60N06





- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

PIN 1. GATE 2. SOURCE CASE. DRAIN

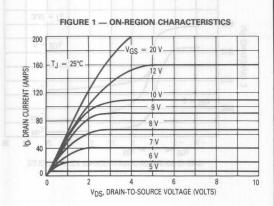
	MILLIN	MILLIMETERS		HES	
DIM	MIN	MAX	MIN	MAX	
A	38.36	39.37	1.510	1.550	
В	19.31	21.08	0.760	0.830	
C	6.35	8.25	0.250	0.325	
D	1.45	1.60	0.057	0.063	
E	1.53	1.77	0.060	0.070	
F	30.15	BSC	1.187 BSC		
G	10.92	10.92 BSC		BSC	
Н	5.46	5.46 BSC		BSC	
J	16.89 BSC		0.665	BSC	
K	11.18	12.19	0.440	0.480	
Q	3.84	4.19	0.151	0.165	
R	25.15	26.67	0.990	1.050	
U	3.84	4.19	0.151	0.165	

CASE 197A-02 TO-204AE

Drain-Source Breakdown Voltage (VGS = 0, ID = 5.0 mA)	MTM60N05 MTM60N06 MTM55N08 MTM55N10	V _{BR} (DSS)	50 60 80 100	Ξ	Vdc
Zero Gate Voltage Drain Current (V _{DS} = Rated V _{DS} , V _{GS} = 0) T _C = 125°C	E SILICON GATE	IDSS	HA <u>M</u> CEN	10 100	μAdc
Gate-Body Leakage Current (VGS = 20 Vdc, VDS = 0)	RANSISTOR for low veltage, high	IGSS	o <u>lan nav</u> se sT33 se	100	nAdc
ON CHARACTERISTICS*	swecning regulators,	se uppe such	ng applicati	WEI SWITCH	od peads
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA}), V_{DS} = V_{J} = 100^{\circ}\text{C}$	- Switching Times	VGS(th)	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 30 Adc) (V _{GS} = 10 Vdc, I _D = 27.5 Adc)	MTM60N05/MTM60N06 MTM55N08/MTM55N10	rDS(on)	1088, VDI ted <u>Te</u> mpa Po ve r Dis	0.028 0.04	Ohm
Drain-Source On-Voltage (V _{GS} = 10 \ (I _D = 60 Adc) (I _D = 30 Adc, T _J = 100°C) (I _D = 55 Adc) (I _D = 27.5 Adc, T _C = 100°C)	/) MTM60N05/MTM60N06 MTM60N05/MTM60N06 MTM55N08/MTM55N10 MTM55N08/MTM55N10	V _{DS} (on)	fode Chara	1.98 1.68 2.6 2.2	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 30 A) (V _{DS} = 15 V, I _D = 27.5 A)	MTM60N05/MTM60N06 MTM55N08/MTM55N10	9FS	10 10	=	mhos
DYNAMIC CHARACTERISTICS		00			
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss	- 504	5000	pF
Output Capacitance	f = 1 MHz)	Coss		2500	
Reverse Transfer Capacitance	See Figure 8	C _{rss}	_	1000	
SWITCHING CHARACTERISTICS* (TJ	= 100°C)			869/111/	N MUNI
Turn-On Delay Time	100 J (00 J (0)))(00 J (00 J (td(on)	_	70	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D ,	t _r	Semine -	350	100
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figure 16	td(off)	SBUY	350	ooupos
Fall Time		tf	HOID -	400	IM I = 3
	V _{DS} = 0.8 Rated,	Ωg	105 (Typ)	120	V eo nC
Total Gate Charge	I _D = Rated, 05 = V _{GS} = 10 V 05 =	Qgs	74 (Typ)	- C	evoundr
YARAM 1882 2 CORTROLLING OWENSION: INCH.	See Figure 15	Q _{gd}	31 (Typ)	_	THE STATE OF
SOURCE DRAIN DIODE CHARACTERIS	STICS*	00			sugenitr
Forward On-Voltage	I _S = Rated I _D	V _{SD}	3.5	4	Vdc
Forward Turn-On Time	V _{GS} = 0	ton	Limited	by stray ind	uctance.
Reverse Recovery Time	2 W/°C	t _{rr}	200	28°C_	ns
INTERNAL PACKAGE INDUCTANCE (T	O-204)		DET LT	Storage	bns gnite
Internal Drain Inductance (Measured from the contact screw on and the center of the die)	the header closer to the source pin	L _d	5 (Typ)	ARACTERS	nH HMAL C
Internal Source Inductance (Measured from the source pin 0.25" fro pad)	om the package to the source bond	L _S	12.5 (Typ)	ase long, for courses 1/8"	stien to C mum Lead Idening Pu

TYPICAL CHARACTERISTICS

MTM60N05, MTM60N06



MTM55N08, MTM55N10

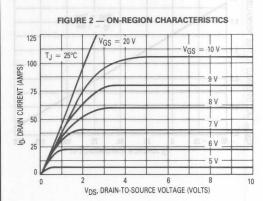


FIGURE 3 — TRANSFER CHARACTERISTICS

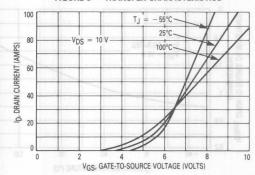


FIGURE 4 — TRANSFER CHARACTERISTICS

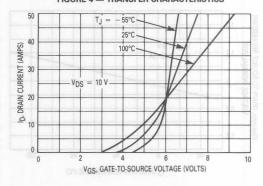


FIGURE 5 — ON-RESISTANCE versus DRAIN CURRENT

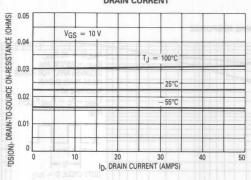


FIGURE 6 — ON-RESISTANCE versus DRAIN CURRENT

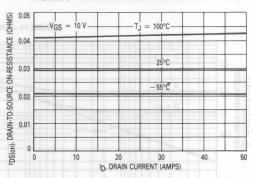


FIGURE 7 — GATE-THRESHOLD VOLTAGE

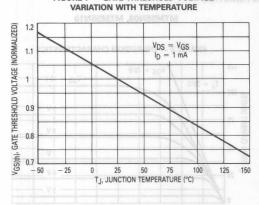


FIGURE 8 — CAPACITANCE VARIATION

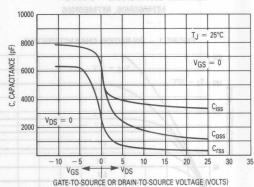


FIGURE 9 — BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE

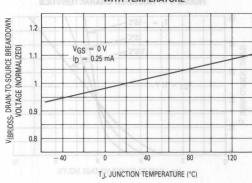
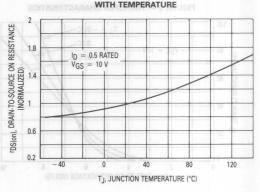
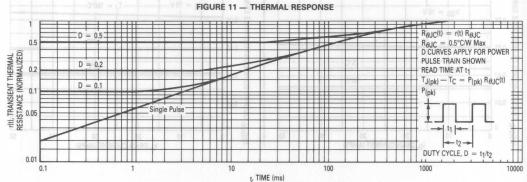


FIGURE 10 — ON-RESISTANCE VARIATION

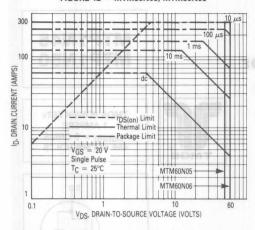


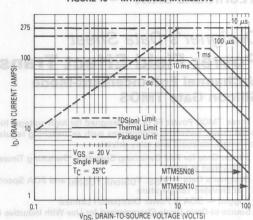


3

FIGURE 12 - MTM60N05, MTM60N06

SAFE OPERATING AREA INFORMATION





FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-tosource voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BB)DSS. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

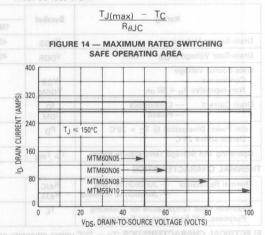


FIGURE 15 — STORED CHARGE versus **GATE-TO-SOURCE VOLTAGE**

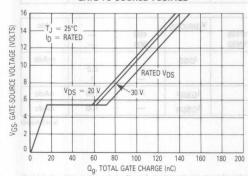
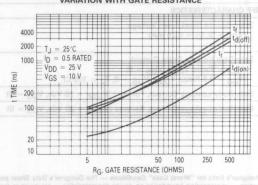


FIGURE 16 — RESISTIVE SWITCHING TIME VARIATION WITH GATE RESISTANCE



3

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

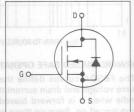
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

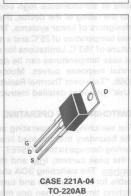
- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MTP1N45 MTP1N50



TMOS POWER FETS
1 AMPERE
rDS(on) = 8 OHMS
450 and 500 VOLTS





MAXIMUM RATINGS

Tumax) = TGaag		M	Unit	
Rating	Symbol	1N45 1N50		
Drain-Source Voltage	VDSS	450	500	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	450	500	Vdc
Gate-Source Voltage Continuous Non-repetitive $(t_p \le 50 \ \mu s)$	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	1 bas stat 4		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		50 1.4	Watts W/°C
Operating and Storage Temperature Range	TJ, Tstq	- 65	to 150	°C

THERMAL CHARACTERISTICS

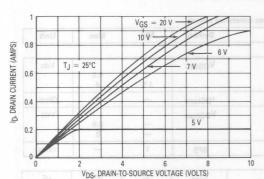
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	llo v °C/W s
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL 0	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Min	Max	Unit
MTP1N45 MTP1N50	V(BR)DSS	450 500	T 0300	Vdc
	IDSS	BATES	0.2	mAdd
	IGSSF	- AUE	100	nAdo
	IGSSR	-	100	nAdd
		MTP1N45 MTP1N50 IDSS	MTP1N45 MTP1N50 V(BR)DSS 450 500 IDSS ——————————————————————————————————	MTP1N45 MTP1N50

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

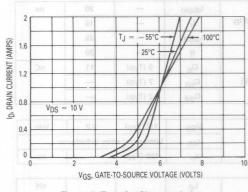
Charac	teristic	Symbol	Min	Max	Unit
N CHARACTERISTICS*		va Ital			
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C	r son	V _{GS(th)}	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (V	GS = 10 Vdc, I _D = 0.5 Adc)	rDS(on)		8	Ohm
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 1 \text{ Adc}$) ($I_D = 0.5 \text{ Adc}$, $T_J = 100^{\circ}\text{C}$)		VDS(on) — 9.5 — 8	Vdc		
Forward Transconductance (V _{DS} = 1	5 V, I _D = 0.5 A)	9FS	1		mhos
YNAMIC CHARACTERISTICS	0 85 - 80 - 80 01	8	a 1	2	
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss	O-SOMEE VOLUE	200	pF
Output Capacitance	f = 1 MHz)	Coss	Section Chara	30	n 73
Reverse Transfer Capacitance	See Figure 11	C _{rss}	_	10	1
WITCHING CHARACTERISTICS* (TJ	= 100°C)				
Turn-On Delay Time	4/2	td(on)	_	20	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	tr	1 -	15	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 13 and 14	td(off)	T _J = 16°C	35	
Fall Time		tf	- D'25-	30	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Qg	9 (Typ)	11	nC
Gate-Source Charge	I_D = Rated I_D , V_{GS} = 10 V)	Qgs	7 (Typ)		
Gate-Drain Charge	See Figure 12	Q _{gd}	2 (Typ)		
OURCE DRAIN DIODE CHARACTERIS	rics*			Vor	= 90/
Forward On-Voltage		V _{SD}	1.8 (Typ)	2.2	Vdc
Forward Turn-On Time	$(I_S = Rated I_D, V_{GS} = 0)$	ton	Limited by st	ray inductai	nce
Reverse Recovery Time	VGS - 0/	t _{rr}	150 (Typ)	SLI	ns
NTERNAL PACKAGE INDUCTANCE	0 00 00	1937 40300 30	MT IOV SOU IDSUM	Man Karry	
Internal Drain Inductance (Measured from the contact screw (Measured from the drain lead 0.25		L _d	3.5 (Typ) 4.5 (Typ)	gure 3 . Tra	nH
Internal Source Inductance (Measured from the source lead 0.	25" from package to source bond pad)	L _S	7.5 (Typ)	-	
Pulse Test: Pulse Width ≤ 300 μs, Duty Cyc	le ≤ 2%.				



QS 1.2 VDS = VGS ID = 1 mA ID = 1 mA

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



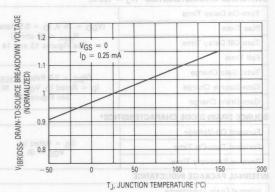
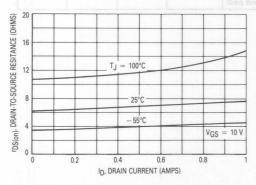


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation
With Temperature



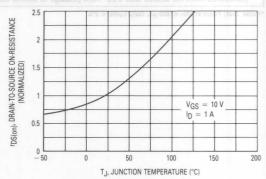


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

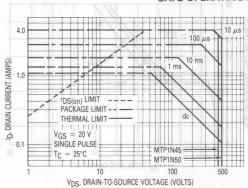


Figure 7. Maximum Rated Forward Biased Safe Operating Area

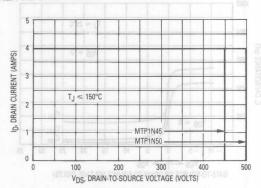


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

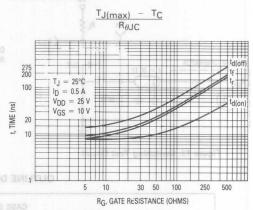


Figure 9. Resistive Switching Time Variation versus Gate Resistance

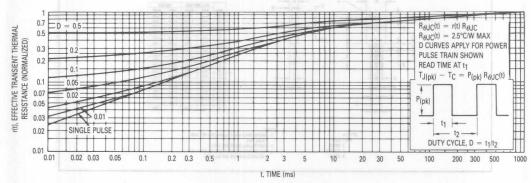


Figure 10. Thermal Response

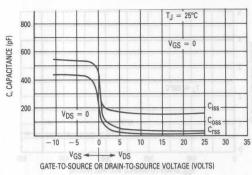


Figure 11. Capacitance Variation

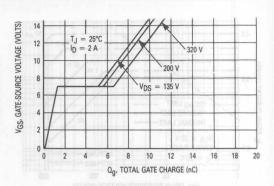


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

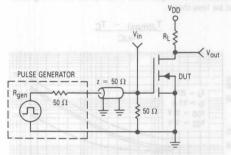


Figure 13. Switching Test Circuit

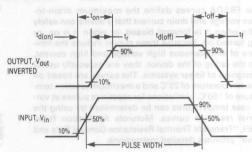
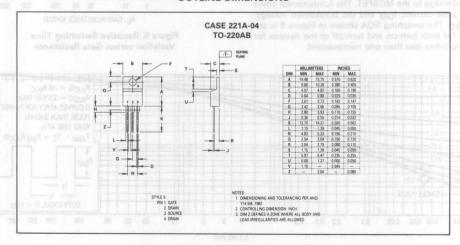


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA ■ SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

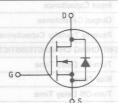
N-Channel Enhancement-Mode Silicon Gate TMOS

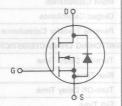
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS

TMOS POWER FETS 1 AMPERE rDS(on) = 12 OHMS 550 and 600 VOLTS





MAXIMUM RATINGS

2.00	0-1-1	MTP		Unit
Rating	Symbol	1N55	1N60	Unit
Drain-Source Voltage	V _{DSS}	550	600	Vdc
Drain-Gate Voltage (R _{GS} = 1 M Ω)	VDGR	550	600	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS}		20 40	Vdc Vpk
Drain Current — Continuous — Pulsed	IDM	3 = 85V		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		0 .4	Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stg}	- 65 1	to 150	°C

THERMAL CHARACTERISTICS

TILMINAL CHANACTERISTICS			
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	%C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C



CASE 221A-04 TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit	
OFF CHARACTERISTICS						
4 40	TP1N55 TP1N60	V _{(BR)DSS}	550 600	=	Vdc	
Zero Gate Voltage Drain Current (Vps = Rated Vpss, Vgs = 0) (Vps = 0.8 Rated Vpss, Vgs = 0, Tj = 125°C)		IDSS	=	0.2	mAdc	
Gate-Body Leakage Current, Forward ($V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$)		IGSSF	_	100	nAdc	
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)		IGSSR	_	100	nAdc	

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Max	Unit
ON CHARACTERISTICS*			16	a She	is Dat	igner
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$ $T_{J} = 100^{\circ}\text{C}$		ansistor	VGS(th)	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (/GS = 10	Vdc, I _D = 0.5 Adc)	rDS(on)	42.01	12	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 0.5 Adc)			VDS(on)	ere designed	6 12	Vdc
Forward Transconductance (V _{DS} =	15 V, I _D =	0.5 A)	9FS	0.5	ngga grimo. dan bisa bisa	mhos
YNAMIC CHARACTERISTICS		n Times	- Switchin	hing Speeds	ntiw2 test	n Gate for
Input Capacitance	(V	DS = 25 V, VGS = 0,	C _{iss}	-	200	ta bpF o
Output Capacitance	1 "	f = 1 MHz	Coss	98(c <u>el</u>) VG8	30	ner's Dat
Reverse Transfer Capacitance		See Figure 11	C _{rss}	II noiseaiseil	10	
WITCHING CHARACTERISTICS* (TJ	= 100°C)	ductive Loads	Use With Inc	acterized for	Diode Char	e-to-Drain
Turn-On Delay Time			td(on)	_	20	ns
Rise Time	(V _{DD}	= 25 V, I _D = 0.5 Rated I _D	t _r	_	15	
Turn-Off Delay Time	s	R _{gen} = 50 ohms) ee Figures 13 and 14	td(off)		35	MITAS IN
Fall Time	tints	ALLW.	t _f	_	30	
Total Gate Charge	(V	DS = 0.8 Rated VDSS,	Qg	8 (Typ)	10	nC
Gate-Source Charge		Rated ID, VGS = 10 V)	Qgs	4 (Typ)	686	loV ecuco
Gate-Drain Charge	Vdc	See Figure 12	Q_{gd}	4 (Typ)	F = 2011 8	iste Veltag
OURCE DRAIN DIODE CHARACTERIS	TICS*	ne -			ab	Ouride Volta
Forward On-Voltage	Vok	±40	V _{SD}	1 (Typ)	(2 u 1.2 = g	Vdc
Forward Turn-On Time	Adc	(I _S = Rated I _D , V _{GS} = 0)	ton	Limited by stray inductance		
Reverse Recovery Time		· G5	Motrr	250 (Typ)	bestun	ns
NTERNAL PACKAGE INDUCTANCE	Watts	50	09	7.97 =	of (a) nortec	liseiQ 18Wo
Internal Drain Inductance (Measured from the contact screw (Measured from the drain lead 0.2			gtaY Ld	3.5 (Typ) 4.5 (Typ)	ogs <u>T</u> empe	Hn ng and St
Internal Source Inductance (Measured from the source lead 0	.25" from p	package to source bond pad)	L _S	7.5 (Typ)	sitonut — s. itonut —	inersistani
Pulse Test: Pulse Width \leq 300 μ s, Duty Cy	cle ≤ 2%.	275	J.	or Soldering	emperature for	um Lead Ti

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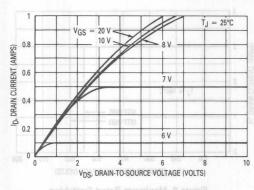


Figure 1. On-Region Characteristics

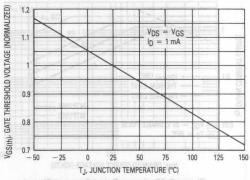


Figure 2. Gate-Threshold Voltage Variation
With Temperature

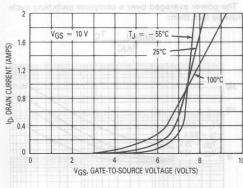


Figure 3. Transfer Characteristics

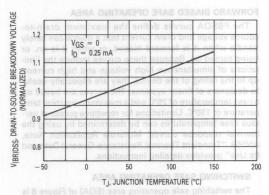


Figure 4. Breakdown Voltage Variation With Temperature

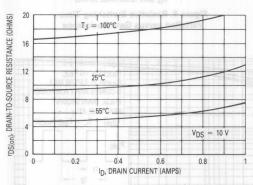


Figure 5. On-Resistance versus Drain Current

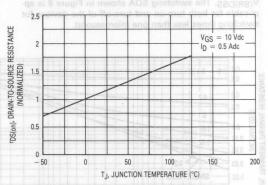


Figure 6. On-Resistance Variation
With Temperature

3

SAFE OPERATING AREA INFORMATION

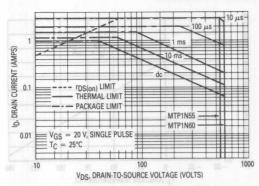


Figure 7. Maximum Rated Forward Biased Safe Operating Area

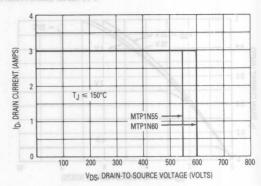


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

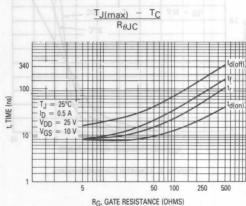


Figure 9. Resistive Switching Time Variation versus Gate Resistance

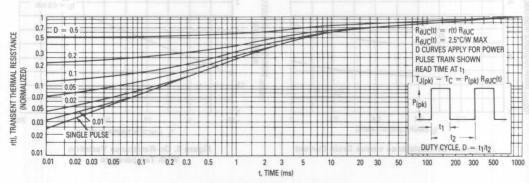


Figure 10. Thermal Response

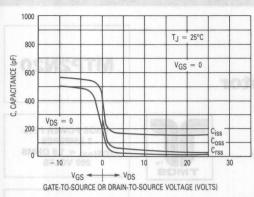


Figure 11. Capacitance Variation

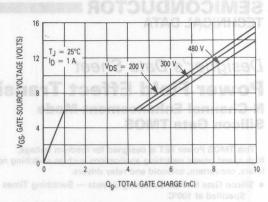


Figure 12. Gate Charge versus Gate-to-Source Voltage

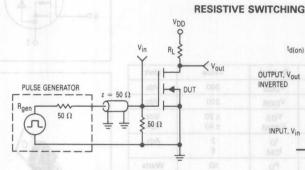


Figure 13. Switching Test Circuit

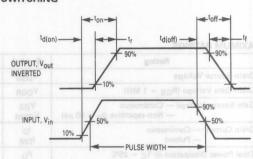
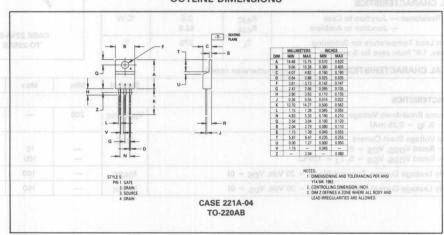


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

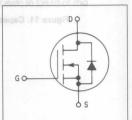
This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS 2 AMPERES rDS(on) = 1.8 OHMS 200 VOLTS

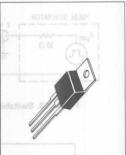


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	VDSS	200	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	200	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	2 6	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	50 0.4	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C



CASE 221A-04 TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

ELECTRICAL CHARACTERISTICS (TC = 25 C utiless otherwise noted)							
Characteristic	Symbol	Min	Max	Unit			
DFF CHARACTERISTICS				III FII			
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)	V _(BR) DSS	200	-	Vdc			
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ = 125°C)	IDSS	=	10 100	μAdc			
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	IGSSF	_	100	nAdc			
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	_	100	nAdo			

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

	Characteristic	Symbol	Min	Max	Unit
N CHARACTERISTICS*	11 5	- A 02 =	SOV	3,57 = f1	
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C	1 N N N N N N N N N N N N N N N N N N N	V _{GS} (th)	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resi	stance (V _{GS} = 10 Vdc, I _D = 1 Adc)	rDS(on)	100	1.8	Ohms
Drain-Source On-Voltage (V (I _D = 2 Adc) (I _D = 1 Adc, T _J = 100°C)		V _{DS} (on)		4.4 3.6	Vdc
Forward Transconductance	(V _{DS} = 15 V, I _D = 1 A)	9FS	0.5	1-10	mhos
YNAMIC CHARACTERISTICS					
Input Capacitance	N== 25 V V== 0	Ciss	N	250	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz})$	Coss	_	100	
Reverse Transfer Capacitan	ce See Figure 11	C _{rss}	n-Re <u>al</u> on Ch	50	
WITCHING CHARACTERISTI	T-1888	100			
Turn-On Delay Time		t _d (on)	_	20	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	tr		30	2
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	t _d (off)		30	
Fall Time	and an analysis	tf		15	
Total Gate Charge		Qq	3.5 (Typ)	10	nC
Gate-Source Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V)	Qgs	2 (Typ)		- S
Gate-Drain Charge	See Figure 12	Qgd	1.5 (Typ)		
OURCE DRAIN DIODE CHAR	ACTERISTICS*	-gu			8
Forward On-Voltage		V _{SD}	1.2 (Typ)	2	Vdc
Forward Turn-On Time	(I _S = Rated I _D , V _{GS} = 0)	ton		tray inductan	ce
Reverse Recovery Time	V _{GS} = 0)	t _{rr}	60 (Typ)		ns
NTERNAL PACKAGE INDUCT	ANCE	1	3 1		
Internal Drain Inductance (Measured from the conta		AGE bLTS)	3.5 (Typ)	V _{GS} , GAT	nH
Internal Source Inductance (Measured from the source	ce lead 0.25" from package to source bond pad	L _S	7.5 (Typ)	-	
Pulse Test: Pulse Width ≤ 300 μ					
	2 VGS = 10 V		V		
	7 VGS = 10 V 10 = 1A VGS = 10 V		A		
	A1 = Q		VI		
	A1 = Q		V		
	15 10 = 1 A		V		
	15 10 = 1 A		V		
	A I — di		V		
001 001	A I — di		1		

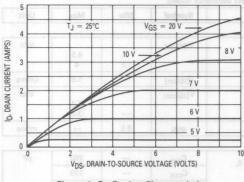


Figure 1. On-Region Characteristics

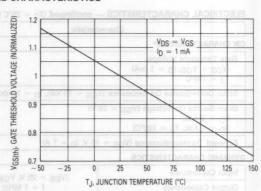


Figure 2. Gate-Threshold Voltage Variation
With Temperature

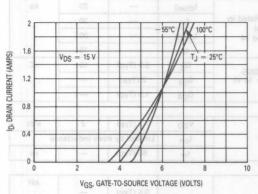


Figure 3. Transfer Characteristics

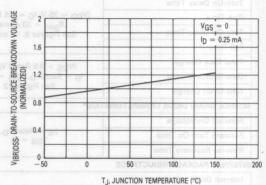


Figure 4. Breakdown Voltage Variation
With Temperature

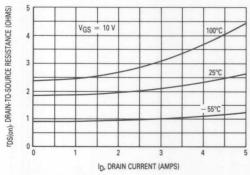


Figure 5. On-Resistance versus Drain Current

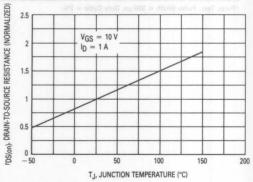


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

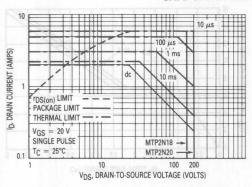


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

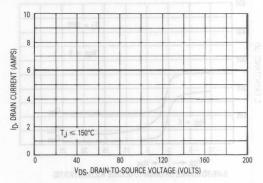


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

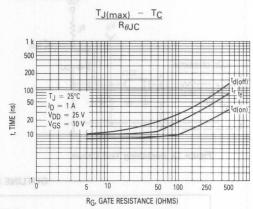


Figure 9. Resistive Switching Time Variation versus Gate Resistance

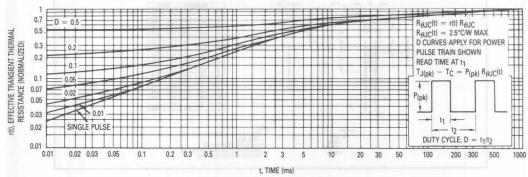


Figure 10. Thermal Response



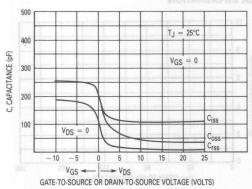


Figure 11. Capacitance Variation

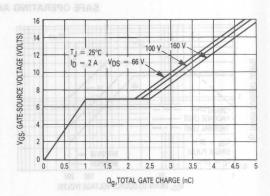


Figure 12. Gate Charge versus

Gate-to-Source Voltage

RESISTIVE SWITCHING

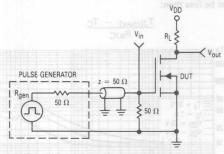


Figure 13. Switching Test Circuit

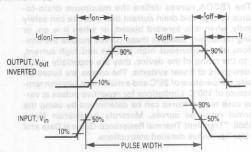
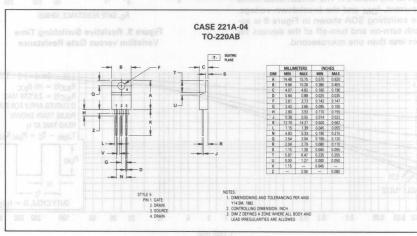


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

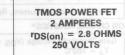
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

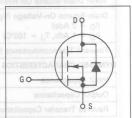
This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times MAT = @ Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS



MAXIMUM RATINGS

	Rating	(no)b ^T	Symbol	MTP2N25	Unit
Drain-Source V	oltage	- Ir	V _{DSS}	250	Vdc
Drain-Gate Vol	tage (R _{GS} = 1 M Ω)	(flo)b ²	VDGR	250	Vdc
Gate-Source V	oltage — Continuous — Non-repetitive (t _p	≤ 50 <i>μ</i> s)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
	- Continuous	ngO	I _D V	= 880 v 2 min = 01	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C		PD	50 0.4	Watts W/°C	
Operating and	Storage Temperature Rang	ge dav	TJ, T _{sta}	65 to 150	°C



THERMAL CHARACTERISTICS

HERIVIAL CHARACTERISTICS			
Thermal Resistance — Junction to Case — Junction to Ambient	R _θ JC R _θ JA	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275 (elb to setneo	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Cha	racterist	tic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	(VGS =	$0, I_D = 0.25 \text{ mA})$		V(BR)DSS	250	J 5,18	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS =		= 125°C)	nst	IDSS	ME b	0.2	mAdo
Gate-Body Leakage Current, Forw	ard (VG	SF = 20 Vdc, V _{DS} = 0)		IGSSF	5/20	100	nAdc
Gate-Body Leakage Current, Reve	rse (VGS	SR = 20 Vdc, V _{DS} = 0)		IGSSR		100	nAdc
ON CHARACTERISTICS*	IN	Speed beeng	de, high	stlev deid so	t bengiseb a	TER 10WG	TWOS P
Gate Threshold Voltage (V _{DS} = V T _J = 100°C	GS, ID	= 1 mA) -100	,eiotslut	V _{GS(th)}	1.5	4.5	Vdc
Static Drain-Source On-Resistance	(VGS	= 10 Vdc, ID = 1 Adc)	miT eni	rDS(on)	itchi ng Spe	2.8	Ohms
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 2 Adc) (I _D = 1 Adc, T _J = 100°C)			V _{DS(on)}	Voston)- V	5.6 4	Vdc	
Forward Transconductance (VDS	= 15 V,	I _D = 1 A)	items beat of	9FS	0.8	abruil nie	mhos
YNAMIC CHARACTERISTICS							
Input Capacitance		(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 10		Ciss	-	400	pF
Output Capacitance				Coss	_	150	
Reverse Transfer Capacitance				C _{rss}	-	65	
WITCHING CHARACTERISTICS* (T	J = 100)°C)				TINGS	AR MUN
Turn-On Delay Time	19-11	MTP2NI2S	lodmy2	td(on)	- 0	25	ns
Rise Time) ($V_{DD} = 25 \text{ V, I}_{D} = 0.5 \text{ Rat}$ $R_{gen} = 50 \text{ ohms}$	ted ID	tr	-	20	Source
Turn-Off Delay Time	abV.	See Figures 12 and 13	3 and	td(off)	TEME	35	r-Gate Volt
Fall Time	- W	420	Vec	tf	evounitre	30	Source V
Total Gate Charge	day	(V _{DS} = 0.8 Rated V _{DS}	VGSM	Qg	6.5 (Typ)	9	nC
Gate-Source Charge	obA	ID = Rated ID, VGS = 1		Qgs	3.5 (Typ)	— Co <u>at</u> laugi	Current
Gate-Drain Charge		See Figure 11	MO	Q_{gd}	3 (Typ)	Decibit	
OURCE DRAIN DIODE CHARACTE	RISTICS	9.0	Q4		267 - 31	25°C	yoda ula
Forward On-Voltage	100	(Is = Rated In	oteT .LT	V _{SD}	2 (Typ)	Storage Ter	Vdc
Forward Turn-On Time		V _{GS} = 0)	100	ton	Limited	by stray ind	uctance
Reverse Recovery Time	MALOS	3.0	Raise	t _{rr}	190 (Typ)	nut — eogs	ns
NTERNAL PACKAGE INDUCTANCE		62.6	ALBR	Ins	etlen te Amble	net —	
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		lie)	L _d Dr	3.5 (Typ) 4.5 (Typ)	Temperatu Tinc — case		
Internal Source Inductance (Measured from the source lead	d 0.25" fr	rom package to source bo	ond pad.)	L _S	7.5 (Typ)	-	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

M TP2N2S

3

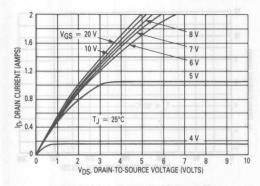


Figure 1. On-Region Characteristics

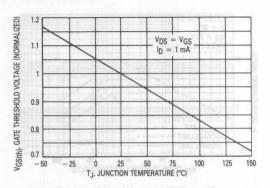


Figure 2. Gate-Threshold Voltage Variation With Temperature

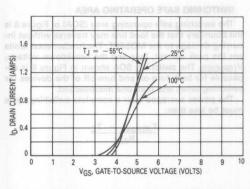


Figure 3. Transfer Characteristics

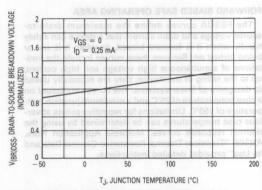


Figure 4. Breakdown Voltage Variation
With Temperature

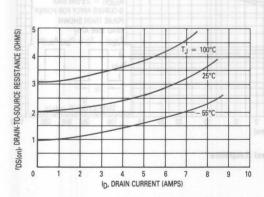


Figure 5. On-Resistance versus Drain Current

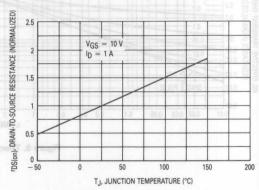


Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

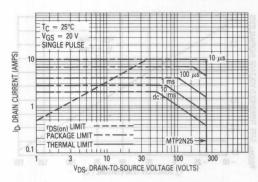


Figure 7. Maximum Rated Forward Biased Safe Operating Area

12 10 (S 8 8 -T J ≤ 150°C 0 50 100 150 200 250 300 VDS, DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

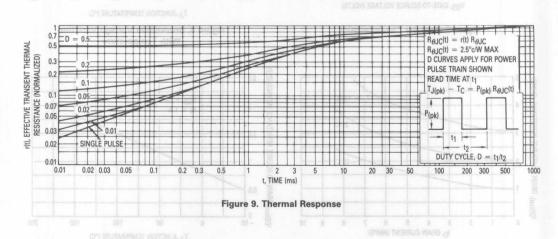
The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

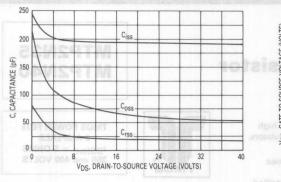
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

 $T_{J(max)} - T_{C}$ $R_{\theta JC}$





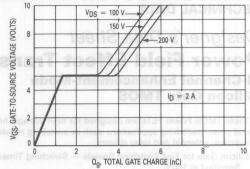


Figure 10. Capacitance Variation

Figure 11. Gate Charge versus Gate-to-Source Voltage

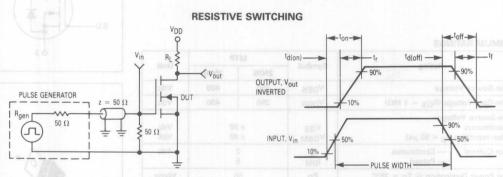
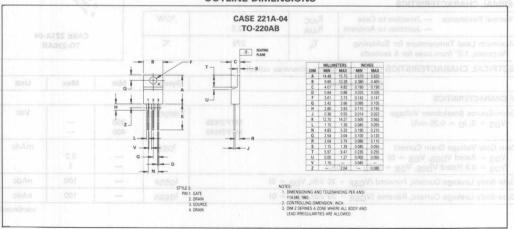


Figure 12. Switching Test Circuit

Figure 13. Switching Waveforms

OUTLINE DIMENSIONS



Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

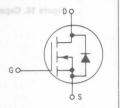
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

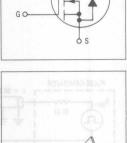
- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

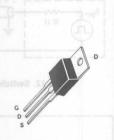




TMOS POWER FETS
2 AMPERES
rDS(cn) = 5 OHMS
350 and 400 VOLTS







CASE 221A-04 TO-220AB

MAXIMUM RATINGS

3

Rating		-st (no.))	M	Unit	
		Symbol	2N35	2N35 2N40	
Drain-Source Voltage		V _{DSS}	350	400	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)		VDGR	350	400	Vdc
Gate-Source Vo Continuous Non-repetitive	(4)-	V _G S V _G SM		20 40	Vdc Vpk
Drain Current	— Continuous — Pulsed	IDM		2 5	Adc
	sipation @ T _C = 25°C 25°C	PD		.4	Watts W/°C
Operating and Storage Temperature Range		T _J , T _{stg}	- 65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	R _θ JC R _θ JA	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit		
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	MTP2N35 MTP2N40	V _{(BR)DSS}	350 400	=	Vdc		
Zero Gate Voltage Drain Current (Vps = Rated Vps, Vgs = 0) (Vps = 0.8 Rated Vps, Vgs = 0, Tj = 125°C)		IDSS	v -	0.2	mAdc		
Gate-Body Leakage Current, Forward ($V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$)		IGSSF	_	100	nAdc		
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	100	IGSSR	_	100	nAdc		

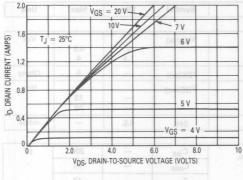
(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

$\textbf{ELECTRICAL CHARACTERISTICS} \ \ - \ \ \textbf{continued} \ \ (T_C = 25^{\circ}\text{C unless otherwise noted})$

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*		VY	NOT NOT		
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C		VGS(th)	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (\	/GS = 10 Vdc, I _D = 2 Adc)	rDS(on)		5	Ohms
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 2 Adc) (I _D = 1 Adc, T _{.I} = 100°C)		V _{DS(on)}	= 1	13 10	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 1 A)		9FS	0.5	-	mhos
DYNAMIC CHARACTERISTICS					1
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	C _{iss}	1.0 m	200	pF
Output Capacitance	f = 1 MHz	Coss	JAPA SCHILLIOS (C) 1-91	30	
Reverse Transfer Capacitance	See Figure 11	C _{rss}	o Ranion Che	10	
WITCHING CHARACTERISTICS* (TJ	= 100°C)				
Turn-On Delay Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _d (on)	-	20	ns
Rise Time		tr	_	15	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	-	35	
Fall Time	12 12 12 12 12 12 12 12 12 12 12 12 12 1	tf	3°80- = 11	30	
Total Gate Charge	(VDS = 0.8 Rated VDSS,	Ωg	9 (Typ)	11	nC
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 V)	Qgs	7 (Typ)	-	5.1
Gate-Drain Charge	See Figure 12	Qgd	2 (Typ)	-	
SOURCE DRAIN DIODE CHARACTERIS	TICS*		11	V 01 = 20	/
Forward On-Voltage	90 = 9	V _{SD}	1.8 (Typ)	2.2	Vdc
Forward Turn-On Time	$(I_S = Rated I_D, V_{GS} = 0)$	ton	Limited by st	ray inductar	nce
Reverse Recovery Time	80 8	t _{rr}	150 (Typ)		ns
NTERNAL PACKAGE INDUCTANCE (T	O-220)			V	ولسل
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L _d	3.5 (Typ) 4.5 (Typ)	Vas. GA	nH
Internal Source Inductance (Measured from the source lead 0	.25" from package to source bond pad.)	L _S	7.5 (Typ)	_	

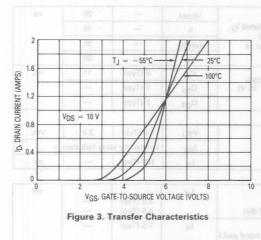
^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.



1.1 VDS = VGS | VG

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



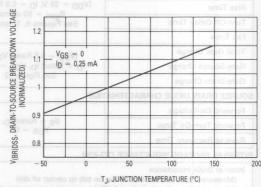
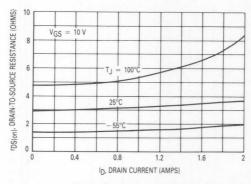


Figure 4. Breakdown Voltage Variation
With Temperature



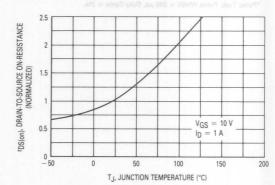


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

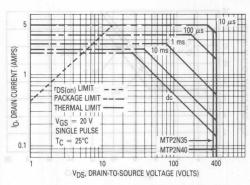


Figure 7. Maximum Rated Forward Biased Safe Operating Area

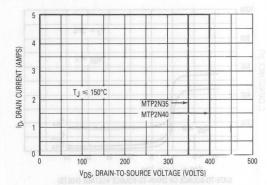


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

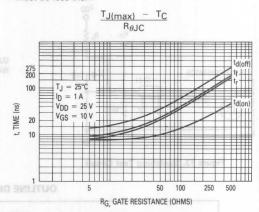


Figure 9. Resistive Switching Time Variation versus Gate Resistance

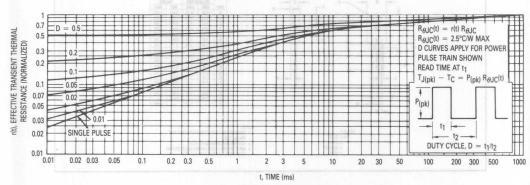


Figure 10. Thermal Response



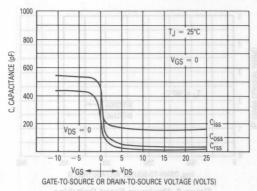


Figure 11. Capacitance Variation

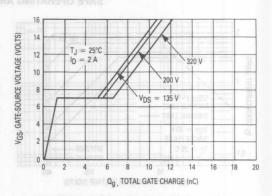


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

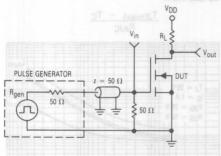


Figure 13. Switching Test Circuit

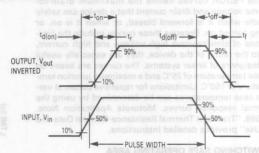


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

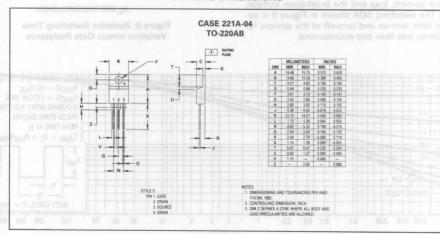


Figure 10. Thermal Response

3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low drive requirements V_{GS(th)} = 4.5 V(max)

MAXIMUM RATINGS

Rating	Symbol	MTP2N55	MTP2N60	Unit
Drain-Sourve Voltage	VDSS	550	600	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	550	600	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS}	±	20 40	Vdc Vpk
Drain Current — Continuous — Pulsed	IDM		2 9 ₁₈ A = 20	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		5 .6	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150		°C

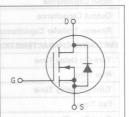
THERMAL CHARACTERISTICS

Thermal Resistance	4.5 (Typ)		telb to remen of die)	°C/W
Junction to Case	F 20 2 2	$R_{\theta}JC$	1.67	
Junction to Ambient	TO-220	$R_{\theta JA}$	62.5	26" favor
Maximum Lead Temperatu Purposes, 1/8" from case		TL	275	°€

TMOS

MTP2N55 MTP2N60

TMOS POWER FETS
2 AMPERES
rDS(on) = 6 OHMS
550 and 600 VOLTS





MTP2N55 MTP2N60 CASE 221A-04 TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS				
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA) MTP2N55 MTP2N60	V(BR)DSS	550 600	=	Vdc
Zero Gate Voltage Drain Current $(V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0)$ $(V_{DS} = 0.8\ Rated\ V_{DSS},\ V_{GS} = 0,\ T_J = 125^{\circ}C)$	IDSS		0.2	mAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	IGSSF	_	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	-	100	nAdc

continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



FLECTRICAL	CHADACTEDICTICS	andimund /T	25°C unless otherwise note	-11
ELECTRICAL	CHARACTERISTICS -	- continued (10 =	25°C unless otherwise note	a)

Characteristic			Symbol	Min	Max	Unit
ON CHARACTERISTICS*			19	แล จกธ	r's Da	angra
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C			VGS(th)	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	$V_{GS} = 10$	Vdc, I _D = 1 Adc)	rDS(on)	-20	6	Ohms
Drain-Source On-Voltage (V _{GS} = (I _D = 1 Adc) (I _D = 1 Adc, T _J = 100°C)	10 V)	tage, high	V _{DS(on)}	are designed	6	Vdc
Forward Transconductance (V _{DS}	= 10 V, I _D =	= 1 A)	9FS	0.75	er bas bior	mhos
DYNAMIC CHARACTERISTICS	1 188	g Times	nirtohin	ching Speed	or Fast Swin	on Gate to
Input Capacitance	23 C3 FV (V _{DS} = 25 V, V _{GS} = 0,	Ciss	-	500	pF pF
Output Capacitance		f = 1 MHz)	Coss	ADS(OU) A(E)	150	Blovetod
Reverse Transfer Capacitance		See Figure 11	C _{rss}	Dissipation L	40	os — be
SWITCHING CHARACTERISTICS* (T	J = 100°C)	ductive Loads	Use With In	aracterized for	n Diede Ch	ce-to-Drain
Turn-On Delay Time				(R) (III)	25	ns
Rise Time	(V _{DD}	= 25 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms)	t _r	_	30	ras sarsa
Turn-Off Delay Time	S	ee Figures 9, 13 and 14	td(off)	-	90	FPSCI BROWN
Fall Time	tinU	089324134 065224334	tf		50	V
Total Gate Charge	350	VDS = 0.8 Rated VDSS,	Qg	16 (Typ)	20	nC
Gate-Source Charge		= Rated ID, VGS = 10 V)	Qgs	7 (Typ)	SEN 198	NOV SIED
Gate-Drain Charge	55V	See Figure 12	Q_{gd}	9 (Typ)	- 1081	augunt
SOURCE DRAIN DIODE CHARACTE	RISTICS*	±40				
Forward On-Voltage	25A		0 V _{SD}	1.1 (Typ)	Iounia 00 -	Vdc
Forward Turn-On Time		(I _S = Rated I _D V _{GS} = 0)	ton	Limited by stray inductance		nce
Reverse Recovery Time	Watts	8.0	t _{rr}	500 (Typ)	28°C —	ns
NTERNAL PACKAGE INDUCTANCE	(TO-220)	-85 to 150	ntaT at	perature Range	meT egator	S bing gnite
Internal Drain Inductance (Measured from contact screw of (Measured from the drain lead)			L _d	3.5 (Typ) 4.5 (Typ)	ACTERIST	
Internal Source Inductance (Measured from the source lead	0.25" from	package to center of pad)	ALAR Ls	7.5 (Typ)	Ineidn	ction to O

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

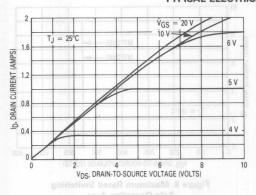


Figure 1. On-Region Characteristics

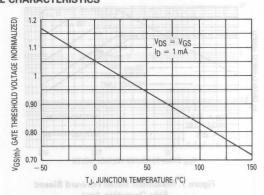


Figure 2. Gate-Threshold Voltage Variation With Temperature

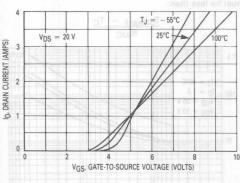


Figure 3. Transfer Characteristics

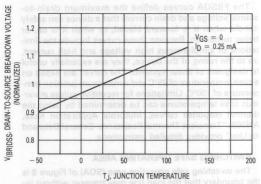


Figure 4. Breakdown Voltage Variation
With Temperature

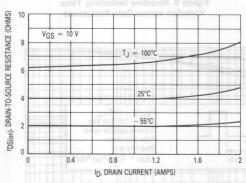


Figure 5. On-Resistance versus Drain Current

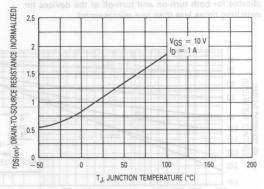


Figure 6. On-Resistance Variation
With Temperature

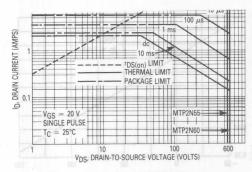


Figure 7. Maximum Rated Forward Biased Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

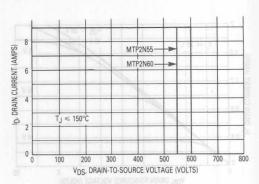


Figure 8. Maximum Rated Switching Safe Operating Area

The power averaged over a complete switching cycle must be less than:

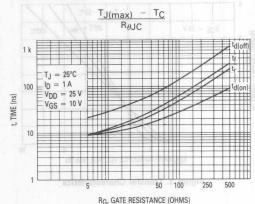


Figure 9. Resistive Switching Time Variation versus Gate Resistance

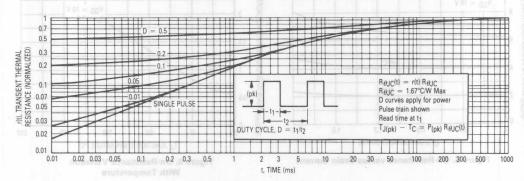


Figure 10. Thermal Response

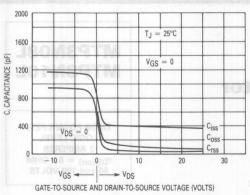


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

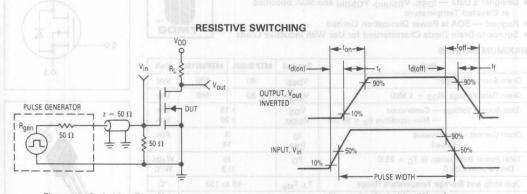
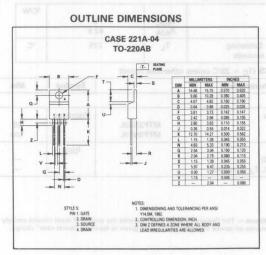


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

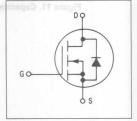
Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These Logic Level TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — V_{GS(th)} = 2 Volts max
 • Silicon Gate for Fast Switching Speeds — Switching Times
- Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTP3N08L

MTP3N10L

TMOS POWER FETS LOGIC LEVEL

3 AMPERES rDS(on) = 0.8 OHM 80 and 100 VOLTS



MAXIMUM RATINGS

Rating	Symbol	MTP3N08L	MTP3N10L	Unit
Drain-Source Voltage	V _{DSS}	80	100	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± ±.		Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	3 14		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	25 0.2		Watts W/°C
Operating and Storage Temperature Range	TJ, Tstq	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance	S M CH S M S M S M	an maumin	°C/W
Junction to Case	$R_{\theta}JC$	5 500	
Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL BAOS	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

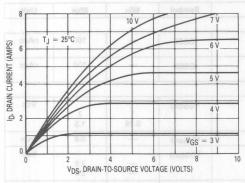
Char	Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS	2017 DES 101 DE 2017 D			ta		
Drain-Source Breakdown Voltage (VGS = 0, ID = 250 μ A)	100 100 100 100 100 100 100 100 100 100	MTP3N08L MTP3N10L	V _{(BR)DSS}	80 100	_	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, T	J = 125°C)	9 B B B B B B B B B B B B B B B B B B B	IDSS	=	1 50	μAdo

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

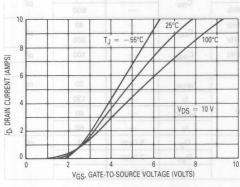
Characteristic			Min	Max	Unit
OFF CHARACTERISTICS (continued)		101		
Gate-Body Leakage Current, Forv (VGSF = 15 Vdc, VDS = 0)	vard	IGSSF	1	100	nAdo
Gate Body Leakage Current, Revo	IGSSR		100	nAdo	
ON CHARACTERISTICS				100	
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) (T, J = 100°C)			1 0.75	2 1.5	Vdc
Static Drain-Source On-Resistance	e (V _{GS} = 5 Vdc, I _D = 2 Adc)	rDS(on)	- 1	0.8	Ohm
Drain-Source On-Voltage (V _{GS} = (I _D = 3 Adc) (I _D = 2 Adc, T _J = 100°C)		VDS(on)	8 2000 PORTA	2.6 2.4	Vdc
Forward Transconductance (VDS	g _{FS}	ession 1 Chara	i-nO : t enu	mhos	
DYNAMIC CHARACTERISTICS	With				
Innut Conscitones	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	0.	-	225	
Input Capacitance	$V_{GS} = 15 \text{ V}, V_{DS} = 0, f = 1 \text{ MHz}$	C _{iss}	-	600	pF
Poverse Transfer Conscitence	$V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	28/5/2	4 + 1	40	pF
Reverse Transfer Capacitance	V _{GS} = 15 V, V _{DS} = 0, f = 1 MHz	C _{rss}	\3° 22 - = 1	360	
Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	Coss	1/4	100	pF
SWITCHING CHARACTERISTICS (T	J = 100°C)				
Turn-On Delay Time	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	td(on)	V±/1	20	ns
Rise Time	$(V_{DD} = 25 \text{ V}, I_{D} = 2 \text{ A},$	tr	777	130	
Turn-Off Delay Time	VGS = 5 V, R _{gen} = 50 ohms)	td(off)	1 + 79	40	
Fall Time	Mary Mary	tf	- 1	60	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Q_g	5 (typ)	8	nC
Gate-Source Charge	ID = 3 A, VGS = 5 Vdc)	Qgs	2 (typ)		
Gate-Drain Charge	See Figures 11 and 12.	Qgd	3 (typ)	STAD ZOV	
SOURCE DRAIN DIODE CHARACTE	RISTICS	politelysets	sension Charge	T E avenS	
Forward On-Voltage	$(I_S = 3 \text{ A, V}_{GS} = 0)$	V _{SD}	1.5 (typ)	1.8	Vdc
Forward Turn-On Time	See Figures 14 and 15.	ton	Limited	by stray ind	uctance
Reverse Recovery Time		t _{rr}	(typ)	_	ns
NTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		Ld	3.5 (typ) 4.5 (typ)	V 8 =	gg/ nH
Internal Source Inductance (Measured from the source lead	0.25" from package to source bond pad.)	L _S	7.5 (typ)	+	e e
Pulse Test: Pulse Width ≤ 300 µs, Duty	/ Cycle ≤ 2%.				-



GATE THRESHOLD VOLTAGE (NORMALIZED) $V_{DS} = V_{GS}$ $I_{D} = 1 \text{ mA}$ 0.9 0.8 - 50 50 100 125 150 T.J. JUNCTION TEMPERATURE (°C)

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Variation With Temperature



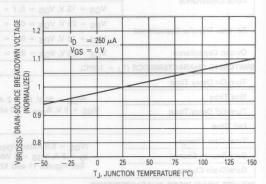
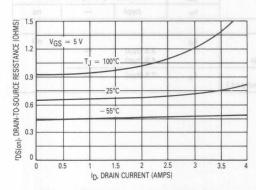


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation With Temperature



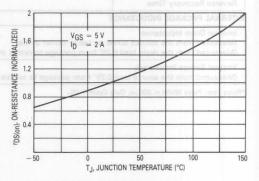


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

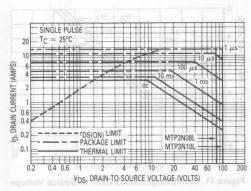


Figure 7. Maximum Rated Forward Biased Safe Operating Area

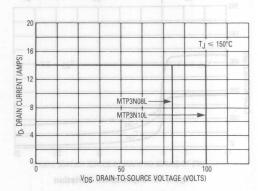


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{\mathsf{T}_{\mathsf{J}(\mathsf{max})} - \mathsf{T}_{\mathsf{C}}}{\mathsf{R}_{\theta}\mathsf{J}\mathsf{C}}$$

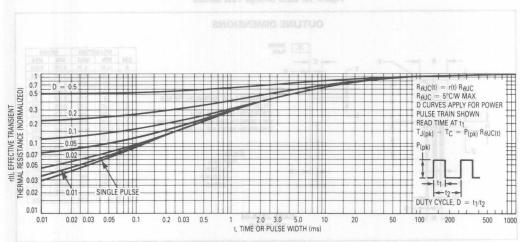


Figure 9. Thermal Response



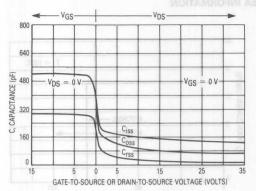
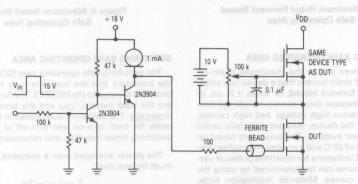


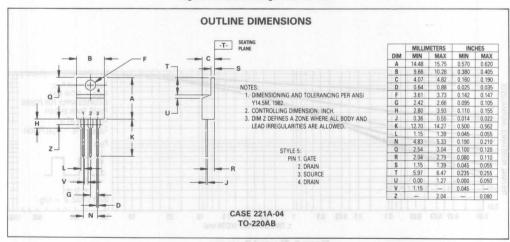
Figure 10. Capacitance Variation

Figure 11. Gate Charge versus Gate-to-Source Voltage



 $V_{in} = 15 V_{pk}$; PULSE WIDTH $\leq 100 \ \mu s$, DUTY CYCLE $\leq 10\%$

Figure 12. Gate Charge Test Circuit



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

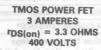
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

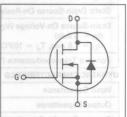
This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement V_{G(th)} = 4.5 Volts (max)





TMOS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	400	Vdc
Drain-Gate Voltage (R _{GS} = 1 MΩ)	VDGR	125 V 004 = 0.5 F	ggVdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu$	VGS VGSM	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed (QVT) 81	I _D	3 0 V bore 8 × 0 = 5	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D (V o	75 0.6	Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance		P	1.67	°C/W
Junction to Case		R _θ JC	1.67	
Junction to Ambient	TO-204	$R_{\theta JA}$	30	(805,000
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C



CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Drain-Source Breakdown Voltage			V(BR)DSS	400	150	Vdc
$(V_{GS} = 0, I_D = 0.25 \text{ mA})$			2.074	0.00 m	2 Table 10 1	
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0, TJ = 125°C) Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)			IDSS	177 <u>-</u> 1 1	0.2	mAdc
			IGSSF	-20	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)		IGSSR	_	100	nAdc	
N CHARACTERISTICS*		e, high speed	r high voltag	designed to	ower FET is	is TMOS Pa
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) $T_J = 100^{\circ}C$			VGS(th)	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 1.5 Adc)			rDS(on)		3.3	Ohms
Drain-Source On-Voltage ($V_{GS}=10~V$) ($I_{D}=3~Adc$) ($I_{D}=1.5~Adc,~T_{J}=100^{\circ}C$)			V _{DS(on)}	Us(an): *I re Discipation	12 10	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 1.5 A)		9FS	0.75	triementip	mhos	
NAMIC CHARACTERISTICS						
Input Capacitance		(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 11		_	500	pF
Output Capacitance				_	100	
Reverse Transfer Capacitance				_	50	
VITCHING CHARACTERISTICS* (T	$J = 100^{\circ}C$	Symbol Value			Rette	
Turn-On Delay Time	Vac		td(on)		40	ns
Rise Time	(V _{DD}	= 125 V, ID = 0.5 Rated ID	t _r	_0M1	60	in-Gate Volt
Turn-Off Delay Time	Say S	R _{gen} = 50 ohms) See Figures 9, 13 and 14		<u>auguni</u>	60	in-Source Ve
Fall Time	- Major	Ob T WSD A	tf	Gut annuada.	30	Supersul's ob
Total Gate Charge	()	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V)		16 (Typ)	20	nC
Gate-Source Charge				10 (Typ)	sipati u n @ 1	al Power Dis
Gate-Drain Charge	. W/C	See Figure 12	Q_{gd}	6 (Typ)	26°C	avode sistel
OURCE DRAIN DIODE CHARACTE	RISTICS*	J. Tsty -65 to 150	0	peratura Rang	Horaga Tem	d box golfane
Forward On-Voltage		(I _S = Rated I _D V _{GS} = 0)	V _{SD}	1 (Typ)	1.4	Vdc
Forward Turn-On Time	WIO		ton	Limited	by stray ind	uctance
Reverse Recovery Time			t _{rr}	300 (Typ)	-	ns
TERNAL PACKAGE INDUCTANCE	(TO-204)	go Augn	602-01		aribioiri	Anna I managaria
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L _d	5 (Typ)	front base f	nH _{scray}	
Internal Source Inductance (Measured from the source pin, 0.25" from the package			Ls	12.5 (Typ)	P -	

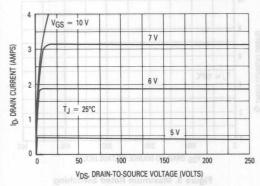


Figure 1. On-Region Characteristics

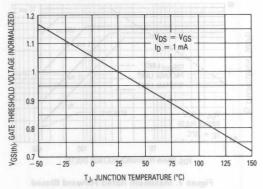


Figure 2. Gate-Threshold Voltage Variation With Temperature

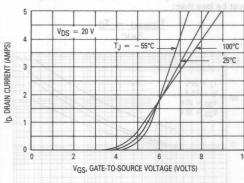


Figure 3. Transfer Characteristics

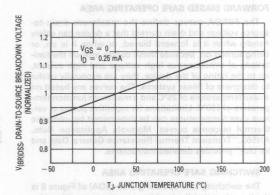


Figure 4. Breakdown Voltage Variation
With Temperature

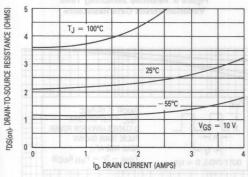


Figure 5. On-Resistance versus Drain Current

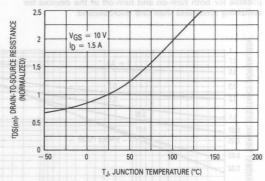


Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

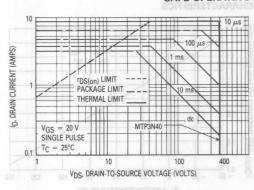


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

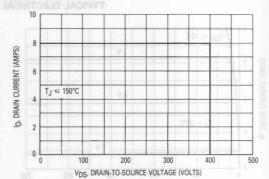


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

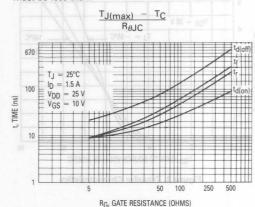


Figure 9. Resistive Switching Time Variation versus Gate Resistance

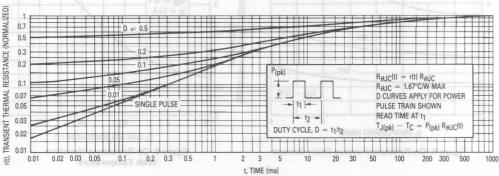


Figure 10. Thermal Response

5000 20

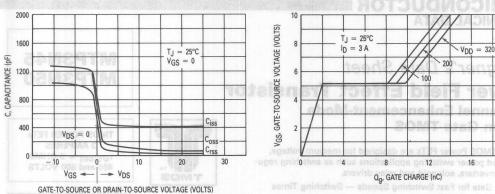


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus
Gate-to-Source Voltage

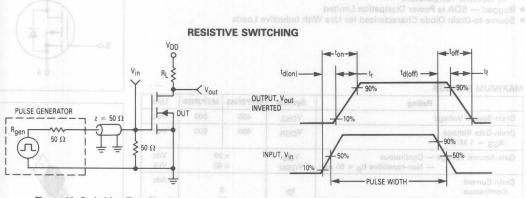
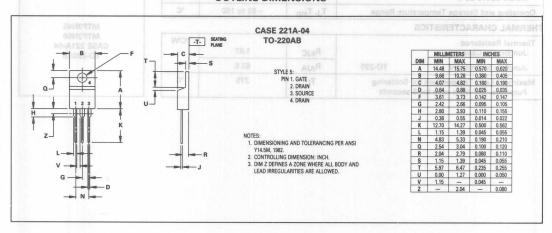


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

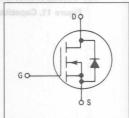
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS
3 AMPERES
rDS(on) = 3 OHMS
450 and 500 VOLTS



MAXIMUM RATINGS

Rating	Symbol	MTP3N45	MTP3N50	Unit
Drain-Source Voltage	V _{DSS}	450	500	Vdc
Drain-Gate Voltage (R _{GS} = 1 MΩ)	V _{DGR}	450	500	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current Continuous Pulsed	I _D	3 10		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	SNOIS!	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance		8A683		°C/W
Junction to Case		R _θ JC	1.67	0 pa
Junction to Ambient	TO-220	R _θ JA	62.5	3-0-1-0-
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL GAST AND S SOLUTION	275	°C



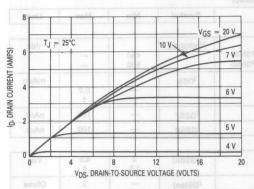
MTP3N45 MTP3N50 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Min	Max	Unit	
OFF CHARACTERISTICS	= 20 V/OS =	201				
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	MTP3N45 MTP3N50	V(BR)DSS	450 500	=	Vdc	
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0, TJ = 125°C)		IDSS		0.2	mAdd	
Gate-Body Leakage Current, Forwa	rd (V _{GSF} = 20 Vdc, V _{DS} = 0)	IGSSF	- 1	100	nAdd	
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)		IGSSR	- 1	100	nAdd	
ON CHARACTERISTICS*						
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C			2 1.5	4.5	Vdc	
Static Drain-Source On-Resistance	(V _{GS} = 10 Vdc, I _D = 1.5 Adc)	rDS(on)	_	3	Ohm:	
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 3 \text{ Adc}$) ($I_D = 1.5 \text{ Adc}$, $T_J = 100^{\circ}\text{C}$)			H-Region Ch	9 7	Vdc	
Forward Transconductance (V _{DS} = 10 V, I _D = 1.5 A)			1		mhos	
OYNAMIC CHARACTERISTICS		Sent Verd	[\ \presi - = [T			
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0,	Ciss	+ 1	500	pF	
Output Capacitance	f = 1 MHz)	Coss	11 + 1	150	V08 =	
Reverse Transfer Capacitance	See Figure 11	C _{rss}	111-	40		
SWITCHING CHARACTERISTICS* (T.	j = 100°C)		VNI			
Turn-On Delay Time		td(on)	1 1	25	ns	
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	tr	1/4	30		
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	4	90		
Fall Time		tf	-	50		
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Qg	16 (Typ)	20	nC	
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 V)	Qgs	10 (Typ)	Z Z		
Gate-Drain Charge	See Figure 12	Q_{gd}	10 (Typ)	TIME ISS		
SOURCE DRAIN DIODE CHARACTER	ISTICS*	etaristica	ensfer Chara	Igure 3. To	1	
Forward On-Voltage	(IS = Rated ID	V _{SD}	1.1 (Typ)	1.5	Vdc	
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	ductance	
Reverse Recovery Time	22,000	t _{rr}	500 (Typ)		ns	
Heverse Hecovery Time	(TO-220)			17.00		
NTERNAL PACKAGE INDUCTANCE	Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		II III		nH	
Internal Drain Inductance (Measured from the contact scre		Ld	3.5 (Typ) 4.5 (Typ)	= 17 -		

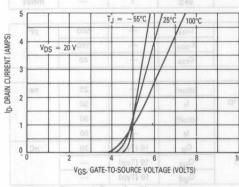
TYPICAL ELECTRICAL CHARACTERISTICS



(NORMALIZED) $V_{DS} = V_{GS}$ $I_D = 1 \text{ mA}$ THRESHOLD VOLTAGE 0.9 GATE 0.8 VGS(th), 0.7 25 50 75 100 125 - 50 - 25 TJ, JUNCTION TEMPERATURE (°C)

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



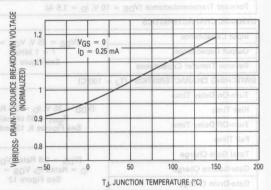
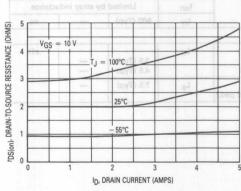


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation
With Temperature



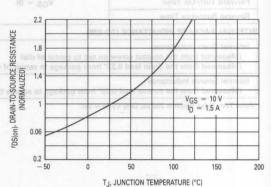


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

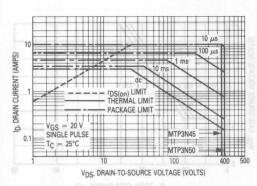


Figure 7. Maximum Rated Forward Biased Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

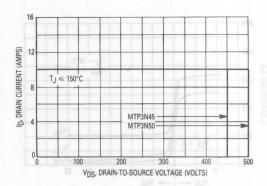


Figure 8. Maximum Rated Switching Safe Operating Area

The power averaged over a complete switching cycle must be less than:

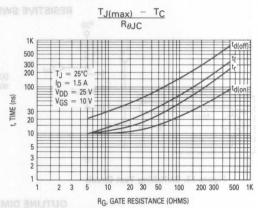
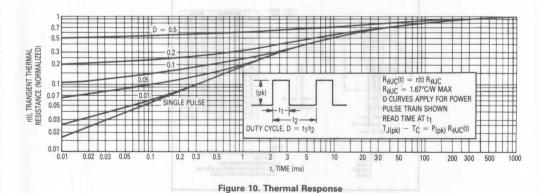
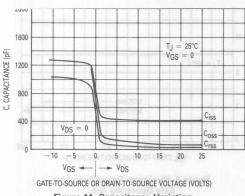


Figure 9. Resistive Switching Time Variation versus Gate Resistance



MOTOROLA TMOS POWER MOSFET DATA



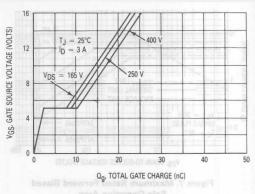
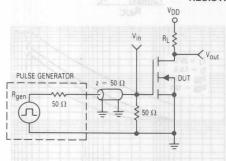


Figure 12. Gate Charge versus Gate-to-Source Voltage

Figure 11. Capacitance Variation

RESISTIVE SWITCHING



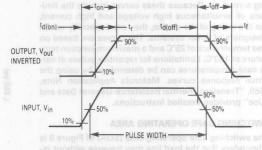
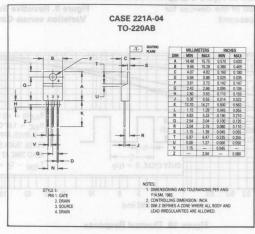


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MTP3N95 MTP3N100

MTP4N85

MTP4N90

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

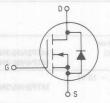
N-Channel Enhancement Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FETS 3 and 4 AMPERES rDS(on) = 4 OHMS 850, 900, 950 and 1000 VOLTS





MAXIMUM RATINGS

cories		M		MTP soneroubnoorn		neroubnoosne	Forward T
Rating	Symbol	4N85	4N90	3N95	3N100	Unit	
Drain-Source Voltage	V _{DSS}	850	900	950	1000	Vdc	
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	850	900	950	1000	Vdc	
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	(1812)		20 40 same	sedtanos anster Capacit	Vdc Vpk	
Drain Current Continuous Pulsed	I _D	4 3 18 16		3	Adc A		
Gate Current — Pulsed	IGM	(amda	08 = nan 1	.5		Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	.8 tins		75 6	amil yels	Watts W/°C	
Operating and Storage Temperature Range	TJ, T _{stq}	and the	-65	to 150	Charge	°C	

THERMAL CHARACTERISTICS (and 45) (above the population of the popu

Thermal Resistance Junction to Case	R_{θ} JC	1.67	Charge	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	62.5	10 300kg NIV	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	OS TL	(0 = ggV .gl bereR = gl)	agestoV-n	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Chara	cteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	ge MTP4N85 MTP4N90 MTP3N95 MTP3N100	V(BR)DSS	850 900 950 1000	's Data Fie <u>l</u> d I	Vdc 1900
Zero Gate Voltage Drain Currer (VDS = Rated VDSS, VGS = (VDS = 0.8 Rated VDSS, VGS	nt (0)	IDSS	JINBING SEMT	0.2	mAdc
Gate-Body Leakage Current, Fo (VGSF = 20 Vdc, VDS = 0)	rward	IGSSF	designed for h	100	nAdc
Gate Body Leakage Current, Re (VGSR = 20 Vdc, VDS = 0)	verse	IGSSR	and re fe y drive	100	nAdc
ON CHARACTERISTICS	BOW!			0°001 % bs	nes Specifi
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) (T _J = 100°C)	00	VGS(th)	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistar (VGS = 10 Vdc, I_D = 1.5 Add (VGS = 10 Vdc, I_D = 2 Adc)		rDS(on)	EU 107 besites	4 4	Ohm
Drain-Source On-Voltage (VGS (I _D = 3 Adc) (I _D = 1.5 Adc, T _J = 100°C) (I _D = 4 Adc) (I _D = 2 Adc, T _C = 100°C)	= 10 V) MTP3N95/3N100 MTP4N85/4N90	V _{DS} (on)	=	12 10 16 14	Vdc
Forward Transconductance (V _{DS} = 10 V, I _D = 1.5 A) (V _{DS} = 10 V, I _D = 2 A)	MTP3N95/3N100 MTP4N85/4N90	9fs	2 2	Ration	mhos
YNAMIC CHARACTERISTICS	000 000	SSGA		881	stlav sotupe:
Input Capacitance	008 008	C _{iss}	_	1500	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Coss	_	150	
Reverse Transfer Capacitance	04.5	C _{rss}	(sq 08 - g0 ps)	60	
WITCHING CHARACTERISTICS	$(T_J = 100^{\circ}C)$				Current
Turn-On Delay Time	87	td(on)	_	40	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r	_	40	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figs. 8 and 9.	td(off)	793	250	
Fall Time	8.0	tf	_	75	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Ωg	55 (typ)	85 85	nC nC
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 Vdc)	Qgs	30 (typ)	стенато	
Gate-Drain Charge	See Figs. 10 and 11.	Ω_{gd}	25 (typ)	a Junc do n to C	
SOURCE DRAIN DIODE CHARAC	TERISTICS	Reda	inaidm	A of notion to A	ngt Restatence
Forward On-Voltage	avs .	V _{SD}	1.1 (typ)	mpb (c.1.5) grm	Vdc
Forward Turn-On Time	(I _S = Rated I _D , V _{GS} = 0) See Figs. 16 and 17.	ton	200 (typ)	r 5 sec <u>o</u> nds	ns
Reverse Recovery Time	300	t _{rr}	1000 (typ)	_	ns

TYPICAL CHARACTERISTICS

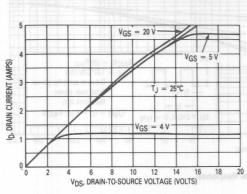
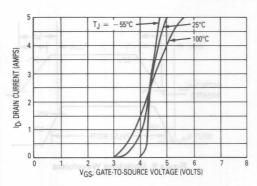


Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation with Temperature



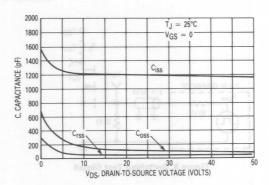
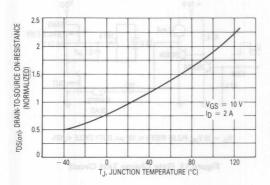


Figure 3. Transfer Characteristics

Figure 4. Capacitance Variation



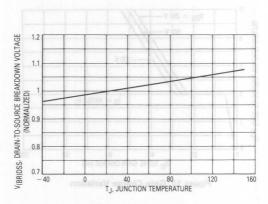


Figure 5. Normalized On-Resistance versus Temperature

Figure 6. Normalized Breakdown Voltage versus Temperature

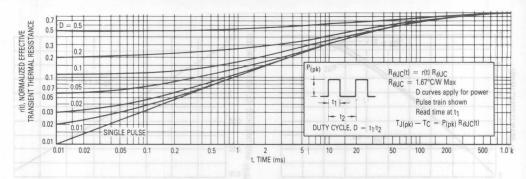


Figure 7. Thermal Response

RESISTIVE SWITCHING

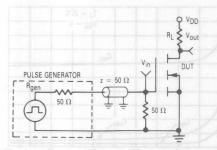


Figure 8. Switching Test Circuit

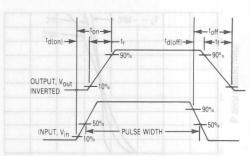


Figure 9. Switching Waveforms

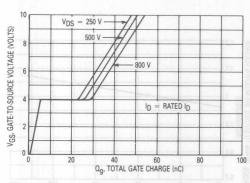


Figure 10. Gate Charge Variation

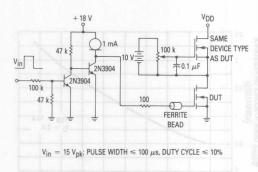


Figure 11. Gate Charge Test Circuit

SAFE OPERATING AREA INFORMATION

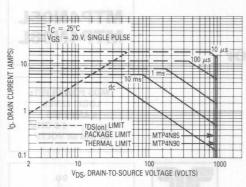


Figure 12. Maximum Rated Forward Biased Safe Operating Area

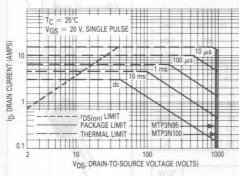


Figure 13. Maximum Rated Forward Biased Safe Operating Area

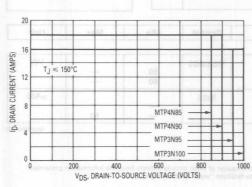


Figure 14. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 11 and 12 are based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

 $I_{DM} = I_{D}(25^{\circ}C) \left[\frac{T_{J}(max) - T_{C}}{P_{D} \cdot R_{\theta J}C \cdot r(t)} \right]$

where

I_D(25°C) = the dc drain current at T_C = 25°C from Figures 11 and 12

T_{J(max)} = rated maximum junction temperature

T_C = device case temperature

 P_D = rated power dissipation at $T_C = 25^{\circ}C$ $R_{\theta JC}$ = rated steady state thermal resistance r(t) = normalized thermal response from Figure 7

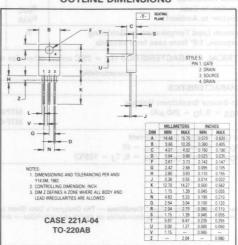
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 13 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 13 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

OUTLINE DIMENSIONS



MTP4N05L

MTP4N06L

TMOS POWER FETS LOGIC LEVEL

4 AMPERES rDS(on) = 0.6 OHM 50 and 60 VOLTS

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

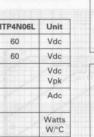
Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These Logic Level TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors - VGS(th) = 2 Volts max
- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MAXIMUM RATINGS

ring safe operating a gnits A) of Figure 13	Symbol	MTP4N05L	MTP4N06L	Unit
Drain-Source Voltage	VDSS	50	60	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	50	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 15 ± 20		Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	12	4	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C (xam)LT	PD	25 0.2		Watts W/°C
Operating and Storage Temperature Range	TJ, Tsta	-65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance AND AND SMLTUO Junction to Case Junction to Ambient	R_{θ} JC R_{θ} JA	5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS				3
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 250 μA) MTP4N05L	V(BR)DSS	50	1	Vdc
MTP4N06L		60	-	
Zero Gate Voltage Drain Current	IDSS			μAdc
$(V_{DS} = Rated V_{DSS}, V_{GS} = 0)$ $(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_{J} = 125^{\circ}C)$		MTP4NB	1 50	
100 101 M1 St 2 (100)		MIPHUS		(conti

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

CI	naracteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continue	d)			3'85 =	13
Gate-Body Leakage Current, For (VGSF = 15 Vdc, VDS = 0)	ward	IGSSF	-	100	nAdc
Gate Body Leakage Current, Rev (VGSR = 15 Vdc, VDS = 0)	verse	IGSSR		100	nAdc
ON CHARACTERISTICS	00 5			111	1
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) (T _J = 100°C)	50	V _{GS(th)}	1 0.75	2 1.5	Vdc
Static Drain-Source On-Resistan	ce (VGS = 5 Vdc, ID = 2 Adc)	rDS(on)	- 1	0.6	Ohm
Drain-Source On-Voltage (V _{GS} (I _D = 4 Adc) (I _D = 2 Adc, T _J = 100°C)		V _{DS(on)}	A A TO-SOUTHE FOUR	1.8	Vdc
Forward Transconductance (VD:	S = 10 V, I _D = 2 A)	g _{FS}	1	y it ganger.	mhos
DYNAMIC CHARACTERISTICS					
Innut Conneitone	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	_	-	225	
Input Capacitance	V _{GS} = 15 V, V _{DS} = 0, f = 1 MHz	Ciss	- 1	600	pF
Payerea Transfer Canacitanas	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	No.	\398= = 1T	40	-5
Reverse Transfer Capacitance	VGS = 15 V, V _{DS} = 0, f = 1 MHz	C _{rss}	1-1	360	pF
Output Capacitance	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	Coss	1	100	pF
SWITCHING CHARACTERISTICS (T _J = 100°C)				
Turn-On Delay Time		td(on)	7-11	20	ns
Rise Time	$(V_{DD} = 25 \text{ V}, I_{D} = 2 \text{ A},$	or = etr	-///	130	
Turn-Off Delay Time	VGS = 5 V, R _{gen} = 50 ohms)	td(off)	- N	40	
Fall Time	40 TO	tf	-	60	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Q_g	4 (typ)	8	nC
Gate-Source Charge	I _D = 4 A, V _{GS} = 5 Vdc)	Qgs	1.5 (typ)	CAD and	2
Gate-Drain Charge	See Figures 11 and 12.	Qgd	2.5 (typ)		
SOURCE DRAIN DIODE CHARACT	ERISTICS	CONTRIBUTE	etter reneritati	e ambia	
Forward On-Voltage	$(I_S = 4 \text{ A}, V_{GS} = 0)$	V _{SD}	1.2 (typ)	1.6	Vdc
Forward Turn-On Time	See Figures 14 and 15.	ton	Limited	by stray indu	uctance
Reverse Recovery Time		t _{rr}	250 (typ)		ns
NTERNAL PACKAGE INDUCTANO	E 81 8			Va - pol	
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L _d	3.5 (typ) 4.5 (typ)		nH
Internal Source Inductance (Measured from the source lead	0.25" from package to source bond pad.)	Ls	7.5 (typ)	-	
		*		THE STATE OF	

MOTOROLA TMOS POWER MOSFET DATA

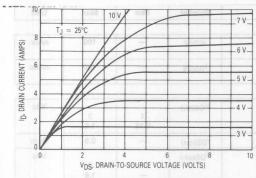


Figure 1. On-Region Characteristics

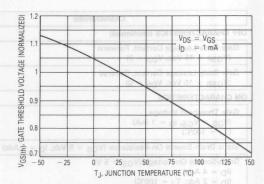


Figure 2. Gate-Threshold Variation
With Temperature

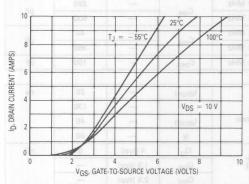


Figure 3. Transfer Characteristics

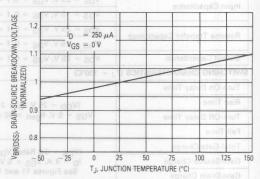


Figure 4. Breakdown Voltage Variation With Temperature

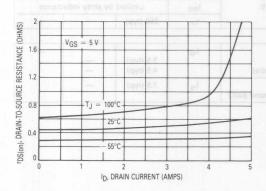


Figure 5. On-Resistance versus Drain Current

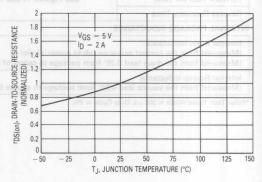


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

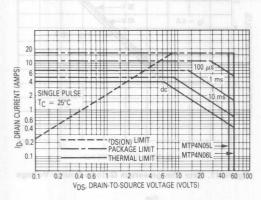


Figure 7. Maximum Rated Forward Biased Safe Operating Area

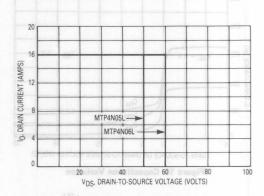


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{\mathsf{T}_{\mathsf{J}(\mathsf{max})} - \mathsf{T}_{\mathsf{C}}}{\mathsf{R}_{\theta}\mathsf{J}\mathsf{C}}$$

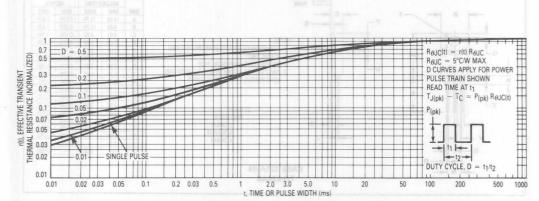


Figure 9. Thermal Response

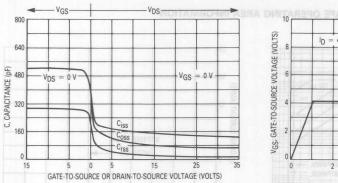
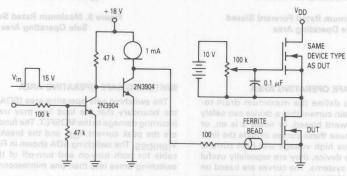


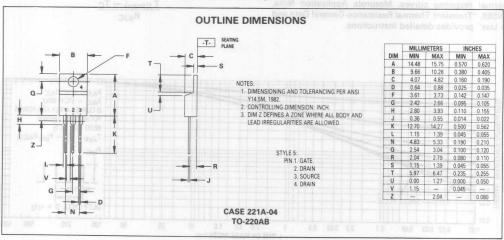
Figure 10. Capacitance Variation

Figure 11. Gate Charge versus Gate-to-Source Voltage



 $V_{in} = 15 V_{pk}$; PULSE WIDTH $\leq 100 \ \mu s$, DUTY CYCLE $\leq 10\%$

Figure 12. Gate Charge Test Circuit



TMOS POWER FET
4 AMPERES
rDS(on) = 0.8 OHM
80 VOLTS

MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

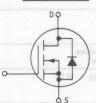
Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS



CASE 221A-04 TO-220AB

MAXIMUM RATINGS

	001	Rating	5804	Figure 1	Symbol	Value	Unit
Drain-Source Vo	ltage		8814		V _{DSS}	80	Vdc
Drain-Gate Volta (R _{GS} = 1 MΩ			(no)b [‡]		VDGR	Delay Time	Vdc no-mul
Gate-Source Vol		ntinuous n-repetitive (t _p	≤ 50 μs)	(b = 0.5 Rated lg = 50 ohms)	V _{GS} V _{GSM}	±20 ±40 erniT vels0	Vdc Vpk
Drain Current	30	-	H				Adc
Continuous Pulsed				Leagy bets 8.6	IDM	9 Charge 9	
Total Power Dis	sipation @	$T_C = 25^{\circ}C$	200	10 VGS = 10 VI	PD	res Charge 00	Watts
Derate above 25°C		2 (Typ)	580	Figure 12	986	0.4 egnario n	W/°C
Operating and S	torage Ter	nperature Rang	e		T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	R_{θ} JC R_{θ} JA	2.5 62.5	°C/W	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275 300/ATO 10 30/AXO	NTERNAL PA	

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

	acteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS					1
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)		V(BR)DSS	80	5VJ_C 1	Vdc
Zero Gate Voltage Drain Current	TOSTETIES	IDSS			μAdc
$(V_{DS} = Rated V_{DSS}, V_{GS} = 0)$ $(V_{DS} = Rated V_{DSS}, V_{GS} = 0)$	T _J = 125°C)	nt-Mode	nc <u>e</u> me	10 100	nanan
Gate-Body Leakage Current, Forwa (VGSF = 20 Vdc, VDS = 0)	ird	IGSSF	_60	100	nAdc
Gate-Body Leakage Current, Rever (VGSR = 20 Vdc, VDS = 0)	se s	IGSSR	designed no Nications su	100	nAdc
N CHARACTERISTICS*	a table a	de Gudeeluid	nan2 naidat	or Foot Sur	t are 2 or
Gate Threshold Voltage	qu silint gi	V _{GS(th)}		100°C	Vdc
$(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$ $T_{J} = 100^{\circ}\text{C}$	NA Specified	SS(th) and SC	1.5	4.5	ner's Di
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 2 Adc)	Inductive Loads	rDS(on)	Diss ip etion teracterized	A 8.0 WE	Ohm
Drain-Source On-Voltage (VGS = (ID = 4 Adc) (ID = 2 Adc, TJ = 100°C)	10 V)	V _{DS(on)}	=	3.6 3.2	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 2 A)		9FS	0.75	-	mhos
YNAMIC CHARACTERISTICS					
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0,	C _{iss}	_	200	pF
Output Capacitance	f = 1 MHz	Coss	_	150	AH MUN
Reverse Transfer Capacitance	See Figure 11	C _{rss}	INGSE	100	4
WITCHING CHARACTERISTICS* (T	j = 100°C)			85010	000000
Turn-On Delay Time	NOG*	td(on)	_	20	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	tr	ntinuotte	80	Source
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	n-rep <u>eti</u> tive ()	30	
Fall Time		tf	_	30	snemy) i
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Qg	3.75 (Typ)	10	nC
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 V)	Qgs	1.75 (Typ)	notetioies	Power D
Gate-Drain Charge	See Figure 12	Q _{gd}	2 (Typ)	58,67	rods star
OURCE DRAIN DIODE CHARACTER	ISTICS*	99	nperature Ran	Storage Ter	pus buite
Forward On-Voltage	(I _S = Rated I _D	V _{SD}	1.8 (Typ)	2.8	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	uctance
Reverse Recovery Time	ALDR	t _{rr}	250 (Typ)	notio —	ns
TERNAL PACKAGE INDUCTANCE		- 91	for S seconds	o Temperatu S' from pase	municipal
Internal Drain Inductance (Measured from the contact screw (Measured from the drain lead 0.2	Ld	3.5 (Typ) 4.5 (Typ)	=	nH	
Internal Source Inductance (Measured from the source lead 0.	25" from package to source bond pad.)	L _S	7.5 (Typ)	-	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

VITP4NO

3

TYPICAL ELECTRICAL CHARACTERISTICS

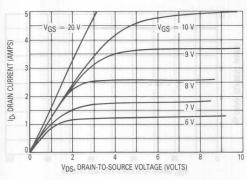


Figure 1. On-Region Characteristics

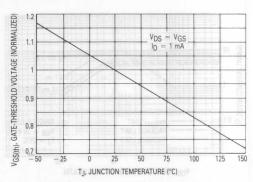


Figure 2. Gate-Threshold Voltage Variation With Temperature

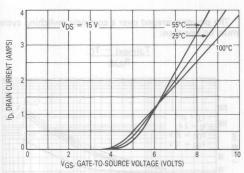


Figure 3. Transfer Characteristics

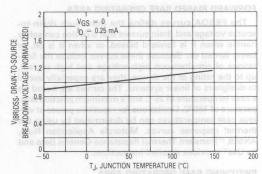


Figure 4. Breakdown Voltage Variation
With Temperature

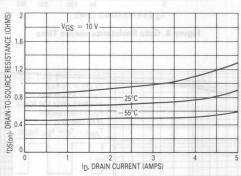


Figure 5. On-Resistance versus Drain Current

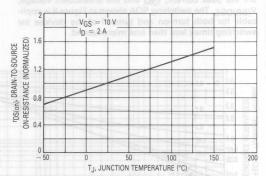


Figure 6. On-Resistance Variation With Temperature

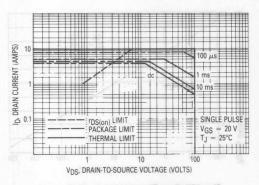


Figure 7. Maximum Rated Forward Biased Safe Operating Area

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

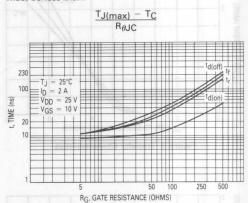


Figure 9. Gate Resistance versus Time

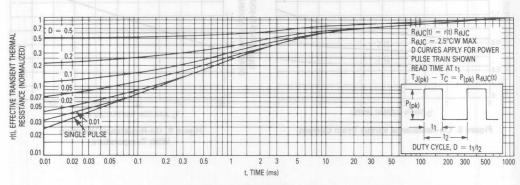
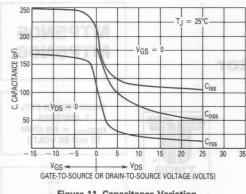


Figure 10. Thermal Response



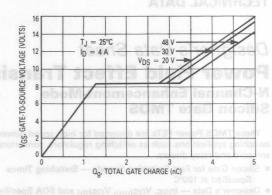


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

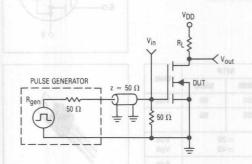


Figure 13. Switching Test Circuit

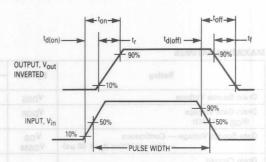
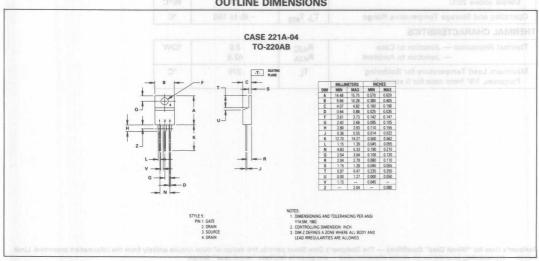


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

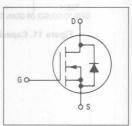
These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MTP5N05 MTP5N06

TMOS POWER FETS
5 AMPERES
rDS(on) = 0.6 OHM
50 and 60 VOLTS

TMOS



MAXIMUM RATINGS

Date:	Complete Vous	M			
Rating	Symbol	5N05 5N06		Unit	
Drain-Source Voltage	VDSS	50	60	Vdc	
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	50	60	Vdc	
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk	
Drain Current Continuous and available printed with a table? Pulsed	I _D		5 3iu	Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	50 0.4		Watts W/°C	
Operating and Storage Temperature Range	T _J , T _{stg}	- 65	to 150	°C	



Thermal Resistance — Junction to Case	$R_{\theta JC}$	2.5	°C/W
 Junction to Ambient 	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C



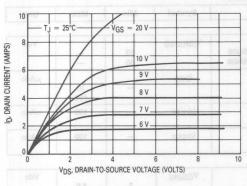
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Charact	eristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	HA E H		-V 02 = 20 V -	08	P
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	MTP5N05 MTP5N06	V(BR)DSS	50 60	1	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ	= 125°C)	IDSS	vs Vs	10 100	μAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		IGSSF	- V S	100	nAdo
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	i de	IGSSR		100	nAdo
ON CHARACTERISTICS*	10 8 - 50 - 25 0	8	0 0	3	0.
Gate Threshold Voltage (Vps = Vgs, Ip = 1 mA) TJ = 100°C		V _{GS(th)}	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 2.5 Adc)		rDS(on)	-	0.6	Ohm
Drain-Source On-Voltage ($V_{GS} = 10^{\circ}$) ($I_{D} = 5 \text{ Adc}$) ($I_{D} = 2.5 \text{ Adc}$, $T_{J} = 100^{\circ}$ C)	v) 0 = 20V	V _{DS(on)}	E	3.2	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 2.5 A)	81 MAL 188	9FS	0.75		mhos
YNAMIC CHARACTERISTICS	28	M. VIII.			
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0,	Ciss	- 1	200	pF
Output Capacitance	f = 1 MHz)	Coss		150	
Reverse Transfer Capacitance	See Figure 11	C _{rss}		100	
WITCHING CHARACTERISTICS* (TJ =	100°C)				
Turn-On Delay Time		td(on)	100	20	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	tr	1 3	80	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	BBATJE ¥ 308UØE	30	
Fall Time		tf		30	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Qg	3.75 (Typ)	10	nC
Gate-Source Charge	I_D = Rated I_D , V_{GS} = 10 V)	Qgs	1.75 (Typ)	_	
Gate-Drain Charge	See Figure 12	Q _{gd}	2 (Typ)	_	
OURCE DRAIN DIODE CHARACTERIST	TCS*				
Forward On-Voltage	(Is = Rated Ip	V _{SD}	1.4 (Typ)	2	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	uctance
Reverse Recovery Time		t _{rr}	250 (Typ)	-	ns
NTERNAL PACKAGE INDUCTANCE	에 없었				
Internal Drain Inductance (Measured from the contact screw on (Measured from the drain lead 0.25" f		L _d	3.5 (Typ) 4.5 (Typ)	=	nH
Internal Source Inductance	from package to source bond pad.)	L _S	7.5 (Typ)		

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

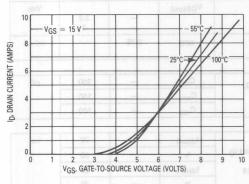
TYPICAL ELECTRICAL CHARACTERISTICS



VGS(th), GATE-THRESHOLD VOLTAGE (NORMALIZED) $V_{DS} = V_{GS}$ $I_{D} = 1 \text{ mA}$ 0.7 -50 25 50 75 100 125 TJ, JUNCTION TEMPERATURE (°C)

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation With Temperature



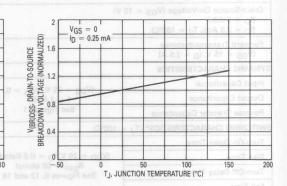
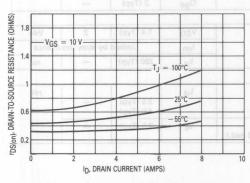


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation With Temperature



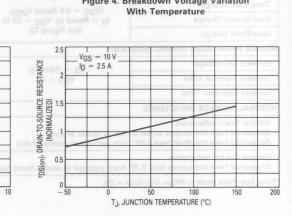


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

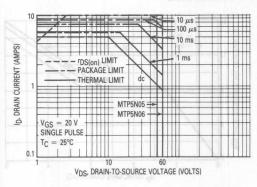


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

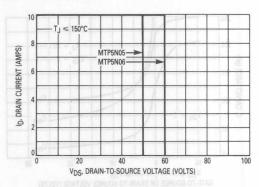


Figure 8. Maximum Rated Switching
Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

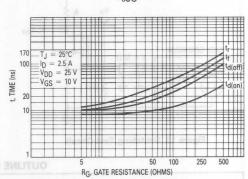


Figure 9. Resistive Switching Time Variation versus Gate Resistance

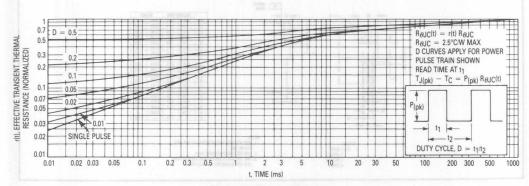


Figure 10. Thermal Response

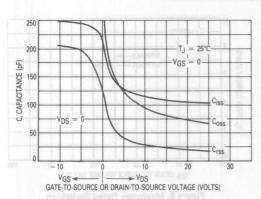


Figure 11. Capacitance Variation

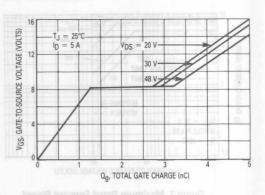


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

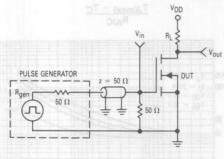


Figure 13. Switching Test Circuit

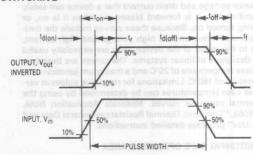
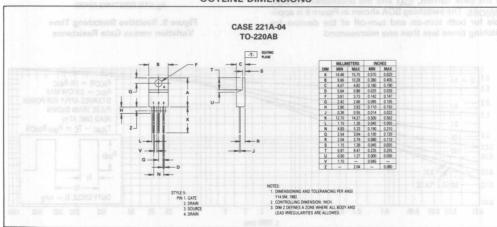


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

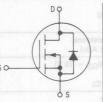
This TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times
 Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FET 5 AMPERES rDS(on) = 0.9 OHM 120 VOLTS





CASE 221A-04 TO-220AB

MAXIMUM RATINGS

001	Rating	3	e Figure 11	Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	120	Vdc	
Drain-Gate Voltage (R _{GS} = 1 MΩ)		(no)h ¹		VDGR	120 emit ysled	Vdc Vdc
Gate-Source Voltage — Co	ontinuous on-repetitive (t _p	≤ 50 μs)	= 50 ohms) res 8, 13 and 14	V _{GS} V _{GSM}	± 20 ± 40 miT ysloQ	Vdc Vpk
Drain Current	-	+3				Adc
Continuous Pulsed			0.8 Rated Vogs.	IDM	5 14	
Total Power Dissipation @	$T_C = 25^{\circ}C$	30 _{Cl}	5 D. VGS = 10 V)	PD	50	Watts
Derate above 25°C	(qyT) E	Ogd	St stoffitt		0.4 epsedO nie	W/°C
Operating and Storage Ter	mperature Rang	je		TJ, Tstg	-65 to 150	°C

THERMAL CHARACTERISTICS 14.1 deV all battell as all depends of the control of the

Thermal Resistance — Junction to Case	(0 = co)	R _θ JC	2.5	°C/W
— Junction to Ambient		$R_{\theta JA}$	62.5	Reverse Re
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL (055-01)	275	A DEMAND

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MOTOROLA SEMICONDUCTOR M

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Chara	cteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS			10	0.	
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	undalara.	V _{(BR)DSS}	120	N Z D	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, T,	IDSS	sweens	10 100	μAdc	
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		IGSSF	-501	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	erters, solenoid	IGSSR	vitching reg	100	nAdc
N CHARACTERISTICS*	JWIT	detiad one	non2 pointsti	and the first San	ates non
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) T _J = 100°C	OA Specified	VGS(th)	2 1.5	4.5	obV ed signer a D
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 2.5 Adc)	absol evituel	rDS(on)	r Dis al pation haraoterized	osboid nie	Ohm
Drain-Source On-Voltage ($V_{GS} = 10$ ($I_{D} = 5$ Adc) ($I_{D} = 2.5$ Adc, $T_{J} = 100^{\circ}$ C)	(V)	V _{DS(on)}	=	6.4 4.5	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 2.5 A)	0	9FS	0.75	_	mhos
YNAMIC CHARACTERISTICS					
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss	_	400	pF
Output Capacitance	f = 1 MHz)	Coss	_	200	A MUME
Reverse Transfer Capacitance	See Figure 11	C _{rss}	517624	100	
WITCHING CHARACTERISTICS* (TJ	= 100°C)			арыпоч	egypied-fil
Turn-On Delay Time	NOOV VOCA	td(on)	-	20	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r	aucomitoi	20	e-Source
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	oviti m par-no	M — 50	
Fall Time		tf	_	50	in Cument
Total Gate Charge	(VDS = 0.8 Rated VDSS,	Q_g	6.5 (Typ)	15	nC
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 V)	Qgs	3.5 (Typ)	ikajnatina (a	al Power
Gate-Drain Charge	See Figure 12	Q_{gd}	3 (Typ)	ne 25 -c	erate alogy
OURCE DRAIN DIODE CHARACTERIS	TICS* T T	egn	mpereture Rai		erering and
Forward On-Voltage	(I _S = Rated I _D	V _{SD}	1.5 (Typ)	ARA E ERIG	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	uctance
Reverse Recovery Time	ALSA	t _{rr} Inei	300 (Typ)	inp —	ns
NTERNAL PACKAGE INDUCTANCE (1	O-220)		ure for Solder	d Temperati	winnin Le
Internal Drain Inductance (Measured from the contact screw (Measured from the drain lead 0.2		Ld	3.5 (Typ) 4.5 (Typ)	=	nH
Internal Source Inductance (Measured from the source lead 0	.25" from package to source bond pad.	L _S	7.5 (Typ)	-	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

WTPBN12

3

TYPICAL ELECTRICAL CHARACTERISTICS

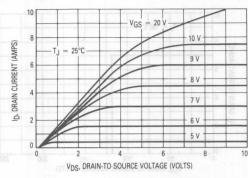


Figure 1. On-Region Characteristics

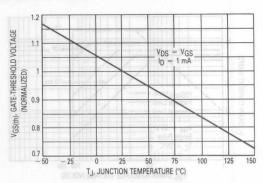


Figure 2. Gate-Threshold Voltage Variation
With Temperature

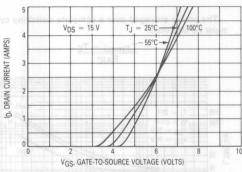


Figure 3. Transfer Characteristics

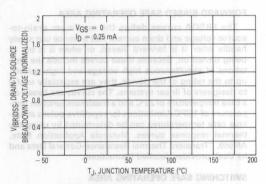


Figure 4. Breakdown Voltage Variation
With Temperature

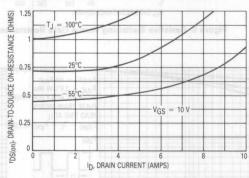


Figure 5. On-Resistance versus Drain Current

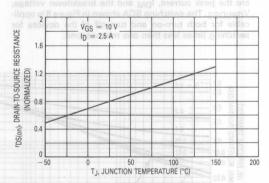


Figure 6. On-Resistance Variation
With Temperature

3

SAFE OPERATING AREA INFORMATION

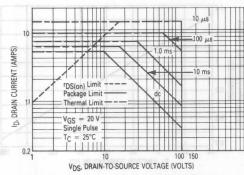


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

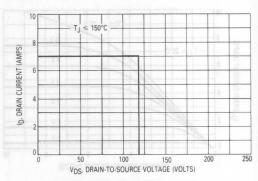


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

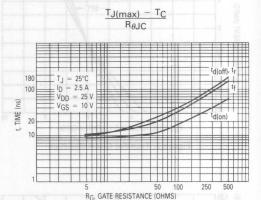


Figure 9. Resistive Switching versus Gate Resistance

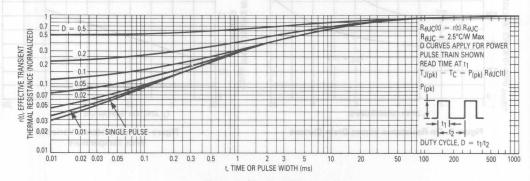
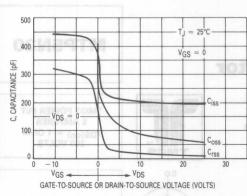


Figure 10. Thermal Response



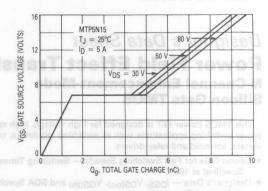
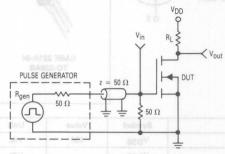


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING



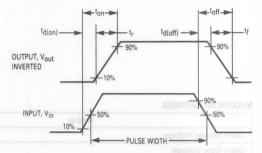
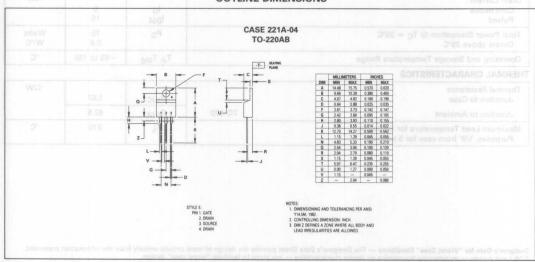


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MTP5N20

Designer's Data Sheet

Power Field Effect Transistor

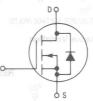
N-Channel Enhancement-Mode Silicon Gate TMOS

This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FET **5 AMPERES** rDS(on) = 1 OHM 200 VOLTS





CASE 221A-04 TO-220AB

MAXIMUM RATINGS

3

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	200	Vdc
Drain-Gate Voltage (R _{GS} = 1 MΩ) (A VOLTAGE AT CAUGIT SIGN	V _{DGR}	200	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current Continuous Pulsed	IDM	5 15	Adc
Total Power Dissipation @ T _C = 25°C BASS 36AS Derate above 25°C BASS OF	PD	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

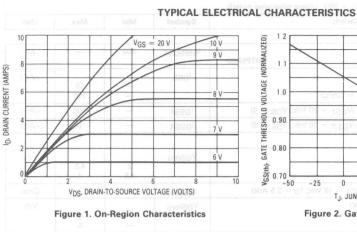
Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MOTOROLA TMOS POWER MOSFET DATA

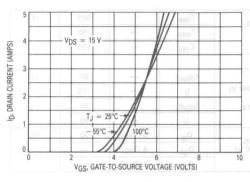
3-584

200 	10 100 100 100 4.5 4 1 6 5 —	Vdc μAdc nAdc nAdc Vdc Ohm Vdc pF
2 1.5 200 = 0.00	10 100 100 100 4.5 4 1	μAdc nAdc Ndc Ohm Vdc
1.5 1.5 - 0.001	100 100 100 100 4.5 4 1 1 6 5 - 500 150	nAdc nAdc Vdc Ohm Vdc
1.5 1.5 - 0.001	100 100 4.5 4 1 6 5 —	NAdc Vdc Ohm Vdc mhos
1.5 1.5 - 0.001	4.5 4 1 6 5 — 500 150	NAdc Vdc Ohm Vdc mhos
1.5 1.5 - 0.001	4.5 4 1 6 5 500 150	Vdc Ohm Vdc mhos
1.5 1.5 - 0.001	6 5 500 150	Ohm Vdc mhos
1.5 1.5 - 0.001	6 5 500 150	Vdc
Region Cha	500 150 100	Vdc
-	5 — 500 150	mhos
1.5	500 150 100	
1.5 ————————————————————————————————————	500 150 100	
+ + + + + + + + + + + + + + + + + + + +	150	pF
+ + + + + + + + + + + + + + + + + + + +	150	pF
+	100	
1 - 1		
		1
	20	ns
1 1	150	
W 1	50	
7/20	50	
9 (Typ)	20	nC
4 (Typ)	0-	0
5 (Typ)	Wast GATE	
1.2 (Typ)	2	Vdc
Limited	by stray inc	ductance
300 (Typ)	_	ns
	TIT	
		nH
3.5 (Typ)	-V 01 - 30V	-
	_ A = Q	-
7.5 (Typ)		
	3.5 (Typ) 4.5 (Typ) 7.5 (Typ)	3.5 (Typ) 4.5 (Typ)



1.0 VOS = VGS VO

Figure 2. Gate-Threshold Voltage Variation With Temperature



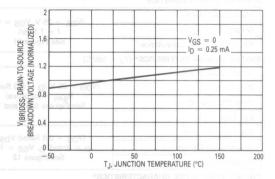
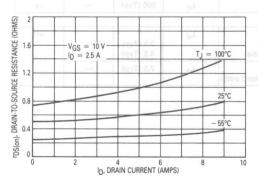


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation
With Temperature



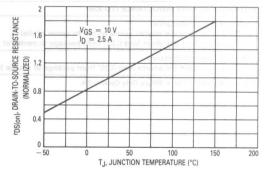


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

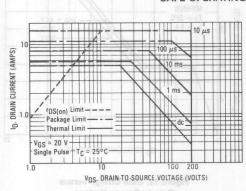


Figure 7. Maximum Rated Forward Biased Safe Operating Area

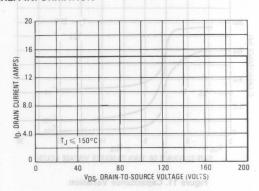


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

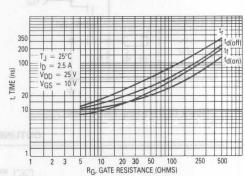


Figure 9. Resistive Switching Time Variation versus Gate Resistance

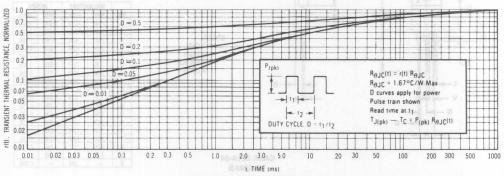
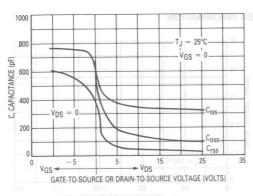


Figure 10. Thermal Response

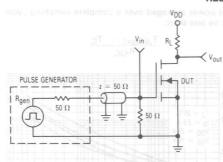


MTP5N20 V_{GS}, GATE SOURCE VOLTAGE (VOLTS) $T_J = 25^{\circ}C$ $I_D = 5 A$ $V_{DS} = 66 V$ - 160 V -100 V 12 Qg, TOTAL GATE CHARGE (nC)

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING





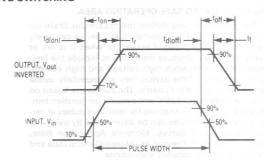
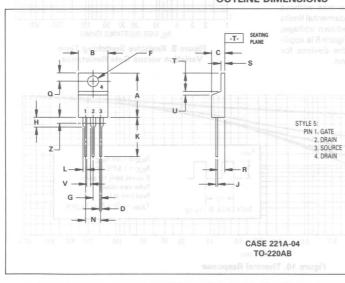


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



- 1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	14.48	15.75	0.570	0.620	
В	9.66	10.28	0.380	0.405	
C	4.07	4.82	0.160	0.190	
D	0.64	0.88	0.025	0.035	
F	3.61	3.73	0.142	0.147	
G	2.42	2.66	0.095	0.105	
H	2.80	3.93	0.110	0.155	
J	0.36	0.55	0.014	0.022	
K	12.70	14.27	0.500	0.562	
L	1.15	1.39	0.045	0.055	
N	4.83	5.33	0.190	0.210	
Q	2.54	3.04	0.100	0.120	
R	2.04	2.79	0.080	0.110	
S	1.15	1.39	0.045	0.055	
T	5.97	6.47	0.235	0.255	
U	0.00	1.27	0.000	0.050	
٧	1.15	-	0.045	-	
Z	-	2.04	_	0.080	

MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

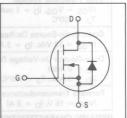
This TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FET 6 AMPERES rDS(on) = 0.6 OHM 100 VOLTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	100	Vdc
Drain-Gate Voltage $(R_{GS} = 1 M\Omega)$	VDGR	100	Vdc
	V _{GS} 50 μs) V _{GSM}	±20 ±40	Vdc Vpk
Drain Current Continuous Pulsed OB	I _D	6 12	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD PD	50 0.4	Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stg}	-65 to 150	°C



THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) Characteristic Symbol Min Max Unit OFF CHARACTERISTICS Drain-Source Breakdown Voltage 100 Vdc V(BR)DSS $(V_{GS} = 0, I_{D} = 0.25 \text{ mA})$ Zero Gate Voltage Drain Current μAdc IDSS $(V_{DS} = Rated V_{DSS}, V_{GS} = 0)$ 10 (VDS = Rated VDSS, VGS = 0, TJ = 125°C) 100 Gate-Body Leakage Current, Forward **IGSSF** 100 nAdc $(V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0)$ Gate-Body Leakage Current, Reverse IGSSR 100 nAdc $(V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0)$ ON CHARACTERISTICS* Vdc Gate Threshold Voltage VGS(th) 2 4.5 $(V_{DS} = V_{GS}, I_D = 1 \text{ mA})$ T_J = 100°C 1.5 4 Static Drain-Source On-Resistance rDS(on) 0.6 Ohm $(V_{GS} = 10 \text{ Vdc}, I_D = 3 \text{ Adc})$ Vdc Drain-Source On-Voltage (VGS = 10 V) V_{DS(on)} (ID = 6 Adc)4.2 $(I_D = 3 \text{ Adc}, T_J = 100^{\circ}\text{C})$ 3.6 mhos Forward Transconductance 9FS $(V_{DS} = 15 \text{ V}, I_{D} = 3 \text{ A})$ **DYNAMIC CHARACTERISTICS** Input Capacitance 400 pF Ciss $(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ **Output Capacitance** Coss 200 f = 1 MHzReverse Transfer Capacitance 100 Crss SWITCHING CHARACTERISTICS* (T1 = 100°C) Turn-On Delay Time 25 td(on) ns $(V_{DD} = 25 \text{ V}, I_D = 0.5 \text{ Rated } I_D$ Rise Time tr 25 R_{gen} = 50 ohms) Turn-Off Delay Time 50 See Figures 13 and 14 td(off) Fall Time tf 50 Total Gate Charge Q_g 6.5 (Typ) 15 nC (VDS = 0.8 Rated VDSS, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12 Qgs Gate-Source Charge 3.5 (Typ) _ Gate-Drain Charge 3 (Typ) Q_{gd} SOURCE DRAIN DIODE CHARACTERISTICS* Forward On-Voltage VSD 1.3 (Typ) 2.5 (IS = Rated ID Forward Turn-On Time $V_{GS} = 0$ Limited by stray inductance ton Reverse Recovery Time trr 250 (Typ) INTERNAL PACKAGE INDUCTANCE Internal Drain Inductance Ld (Measured from the contact screw on tab to center of die) 3.5 (Typ) (Measured from the drain lead 0.25" from package to center of die) 4.5 (Typ) Internal Source Inductance Ls 7.5 (Typ) (Measured from the source lead 0.25" from package to source bond pad.)

*Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

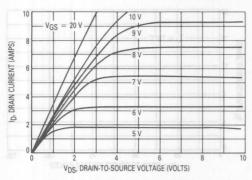


Figure 1. On-Region Characteristics

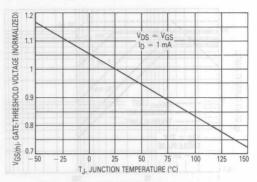


Figure 2. Gate-Threshold Voltage Variation With Temperature

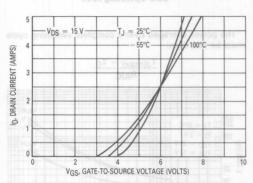


Figure 3. Transfer Characteristics

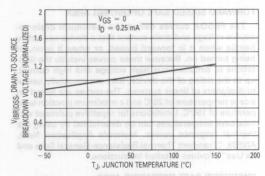


Figure 4. Breakdown Voltage versus Temperature

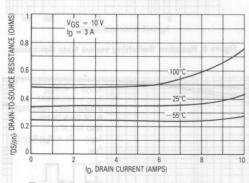


Figure 5. On-Resistance versus Drain Current

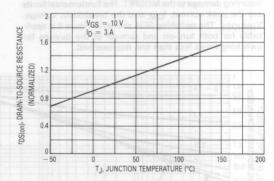


Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

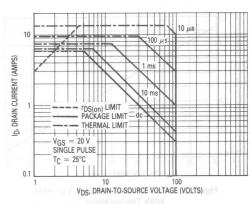


Figure 7. Maximum Rated Forward Biased Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

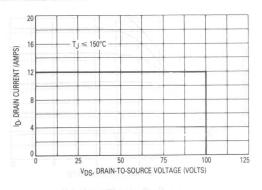


Figure 8. Maximum Rated Switching Safe Operating Area

The power averaged over a complete switching cycle must be less than:

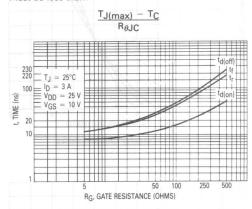


Figure 9. Resistive Switching versus Gate Resistance

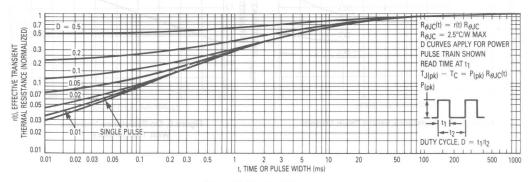
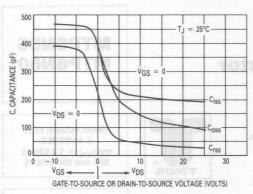


Figure 10. Thermal Response



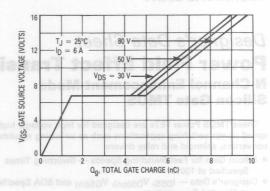


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

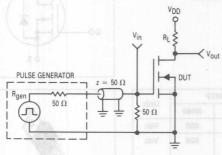


Figure 13. Switching Test Circuit

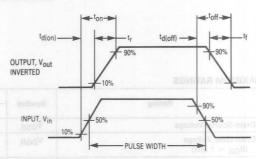
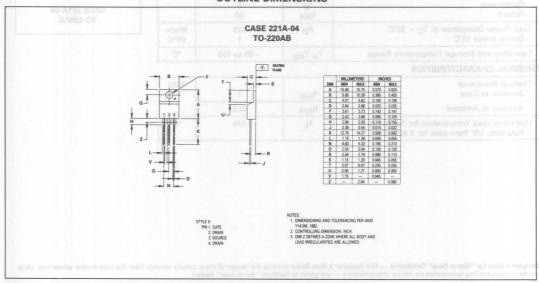


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

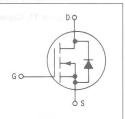
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- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS
6 AMPERES
rDS(on) = 1.2 OHMS
550 and 600 VOLTS



MAXIMUM RATINGS

Danie -		MTP		
Rating	Symbol	6N55	6N60	Unit
Drain-Source Voltage	V _{DSS}	550	600	Vdc
Drain-Gate Voltage (RGS = 1 MΩ)	V _{DGR}	550	600	Vdc
Gate-Source Voltage — Continuous — Non-repetitive (t _p ≤ 50 μs)	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current Continuous Pulsed	IDM	6 30		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C		125 1		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		R_{θ} JC	1	°C/W
Junction to Ambient		$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C

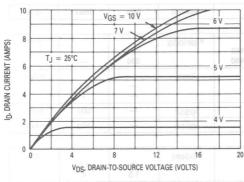


Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Chara	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS			K L VI		
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA) MTP6N55 MTP6N60		V _{(BR)DSS}	550 600	_ 0.92	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS =	0, T _J = 125°C)	IDSS	_	0.2	mAdd
Gate-Body Leakage Current, Forward	rd (V _{GSF} = 20 Vdc, V _{DS} = 0)	IGSSF	+ 1	500	nAdc
Gate-Body Leakage Current, Revers	e (V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR		500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$ $T_{J} = 100^{\circ}\text{C}$	O ST ST ST ST ST	V _{GS(th)}	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance	VGS = 10 Vdc, ID = 3 Adc)	rDS(on)	-Region Cha	0 1.2	Ohms
Drain-Source On-Voltage ($V_{GS} = 1$) ($I_D = 6$ Adc) ($I_D = 3$ Adc, $T_J = 100$ °C)	V _{DS(on)}	=	8 7.2	Vdc	
Forward Transconductance (VDS =	9FS	2		mhos	
YNAMIC CHARACTERISTICS	8 8		1100		
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss	14	1800	pF
Output Capacitance	f = 1 MHz)	Coss	V /\ - 1	350	
Reverse Transfer Capacitance	See Figure 11	C _{rss}	DX# 1	150	
WITCHING CHARACTERISTICS* (TJ	= 100°C)	3-00) era			
Turn-On Delay Time	NAME OF THE PARTY	t _{d(on)}	1 -\ 1	60	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	= gg t _r	+ ///	150	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	-	200	
Fall Time		tf	1 + 3	120	
Total Gate Charge	(Vps = 0.8 Rated Vpss,	Q_g	45 (Typ)	65	nC
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 V)	Qgs	22 (Typ)	VGS GATE	
Gate-Drain Charge	See Figure 12	Q_{gd}	23 (Typ)	igur a 3 . Tr	
OURCE DRAIN DIODE CHARACTERI	STICS*				
Forward On-Voltage	(Is = Rated In	V _{SD}	1.3 (Typ)	_	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	uctance
Reverse Recovery Time		t _{rr}	600 (Typ)	2000	ns
NTERNAL PACKAGE INDUCTANCE	V 01 = 20 V 02 5				
Internal Drain Inductance (Measured from the contact screw (Measured from the drain lead 0.25	Ld	3.5 (Typ) 4.5 (Typ)	-	nH	
Internal Source Inductance (Measured from the source lead 0.2	L _S	7.5 (Typ)	J'di		

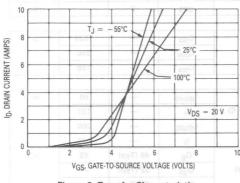
TYPICAL ELECTRICAL CHARACTERISTICS



1.1 VDS = VGS ID = 1 mA VDS = VGS ID = VGS ID = 1 mA VDS = VGS ID = VGS

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation With Temperature



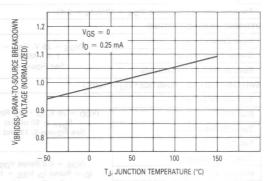
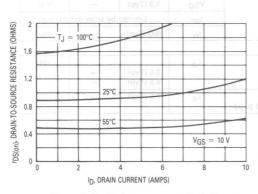


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation
With Temperature



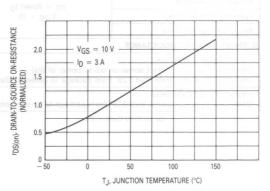


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

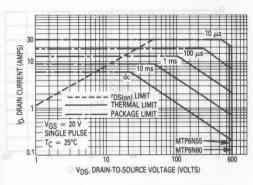


Figure 7. Maximum Rated Forward Biased Safe Operating Area

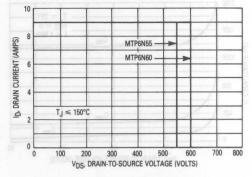


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

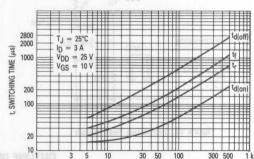
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SWITCHING SAFE OPERATING AREA

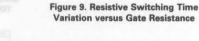
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The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$



RG, GATE RESISTANCE (OHMS)



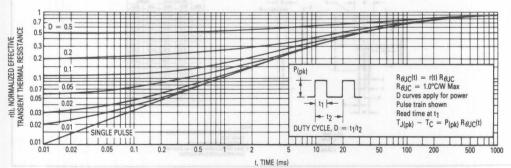
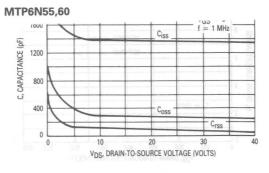


Figure 10. Thermal Response



VDS = 100 V 480 V 480 V Qg, TOTAL GATE CHARGE (nC)

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

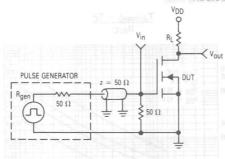
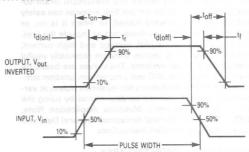
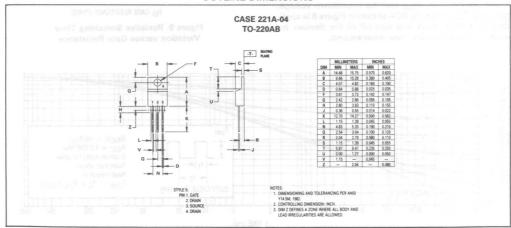


Figure 13. Switching Test Circuit



8 Stupiel Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

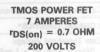
Power Field Effect Transistor

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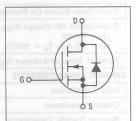
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- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS



MAXIMUM RATINGS

	Rating		Symbol	Value	Unit
Drain-Source Vol	tage	5116/12	VDSS	200	Vdc
Drain-Gate Voltage (RGS = 1 M Ω) Gate-Source Voltage — Continuous — Non-repetitive (tp \leq 50 μ s)		VDGR	200 ±20 ±40	Vdc	
		V _{GS} V _{GSM}		Vdc Vpk	
Drain Current Continuous Pulsed	4 (Typ) — b (Typ) —	ogd Ogd	I _D	7 mg/ 18	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C		PD	75 0.6	Watts W/°C	
Operating and Storage Temperature Range			TJ, Tstg	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance				°C/W
Junction to Case		$R_{\theta JC}$	1.67	
Junction to Ambient	TO-220	R_{θ} JA	62.5	o or dat no va
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C



CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) Characteristic Symbol Min OFF CHARACTERISTICS Drain-Source Breakdown Voltage Vdc V(BR)DSS 200 $(V_{GS} = 0, I_{D} = 0.25 \text{ mA})$ Zero Gate Voltage Drain Current μAdc DSS (VDS = Rated VDSS, VGS = 0) 10 $(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_{J} = 125^{\circ}C)$ 100 Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0) IGSSF 100 nAdc Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0) **IGSSR** 100 nAdc ON CHARACTERISTICS* VGS(th) Gate Threshold Voltage Vdc 2 $(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$ $T_{J} = 100^{\circ}\text{C}$ 45 1.5 4 0.7 Ohm Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 3.5 Adc) rDS(on) Drain-Source On-Voltage (VGS = 10 V) V_{DS}(on) Vdc 5.9 $(I_D = 7 Adc)$ $(I_D = 3.5 \text{ Adc, T}_J = 100^{\circ}\text{C})$ 5 1.5 Forward Transconductance ($V_{DS} = 15 \text{ V}, I_{D} = 3.5 \text{ A}$) mhos 9FS DYNAMIC CHARACTERISTICS 700 Input Capacitance Ciss pF $(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz})$ 300 **Output Capacitance** Coss See Figure 11 Crss 80 Reverse Transfer Capacitance SWITCHING CHARACTERISTICS* (TJ = 100°C) Turn-On Delay Time 50 td(on) $(V_{DD} = 25 \text{ V}, I_D = 0.5 \text{ Rated ID})$ Rise Time 150 R_{gen} = 50 ohms) See Figures 9, 13 and 14 Turn-Off Delay Time 100 td(off) Fall Time 50 tf **Total Gate Charge** 9 (Typ) Q_g 20 nC $(V_{DS} = 0.8 \text{ Rated } V_{DSS},$ $I_{D} = \text{Rated } I_{D}, V_{GS} = 10 \text{ V})$ See Figure 12 4 (Typ) Gate-Source Charge Q_{gs} Gate-Drain Charge Q_{gd} 5 (Typ) SOURCE DRAIN DIODE CHARACTERISTICS* Forward On-Voltage VSD 1.5 (Typ) 3 (IS = Rated ID Forward Turn-On Time Limited by stray inductance $V_{GS} = 0)$ ton Reverse Recovery Time 300 (Typ) t_{rr} INTERNAL PACKAGE INDUCTANCE (TO-220) Internal Drain Inductance Ld (Measured from the contact screw on tab to center of die) 3.5 (Typ) (Measured from the drain lead 0.25" from package to center of die) 4.5 (Typ) Internal Source Inductance 7.5 (Typ)

(Measured from the source lead 0.25" from package to source bond pad.)

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

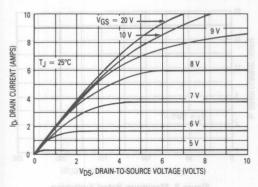


Figure 1. On-Region Characteristics

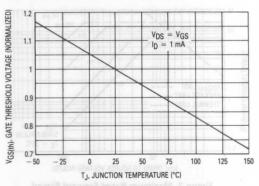


Figure 2. Gate-Threshold Voltage Variation With Temperature

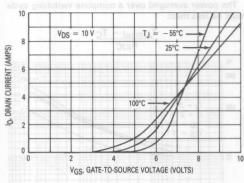


Figure 3. Transfer Characteristics

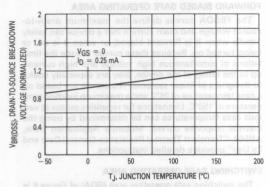


Figure 4. Breakdown Voltage Variation
With Temperature

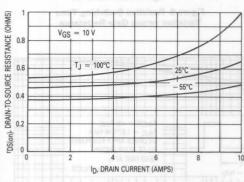


Figure 5. On-Resistance versus Drain Current

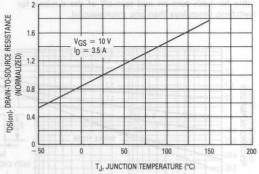


Figure 6. On-Resistance Variation
With Temperature

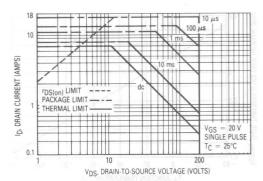


Figure 7. Maximum Rated Forward Biased Safe Operating Area

20 16 16 17 17 12 10 10 10 150 200 250 Vos. Drain-to-source voltage (volts)

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

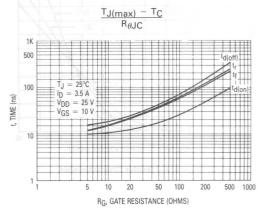


Figure 9. Resistive Switching Time Variation versus Gate Resistance

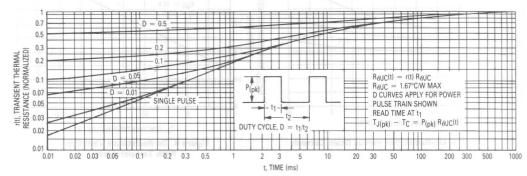
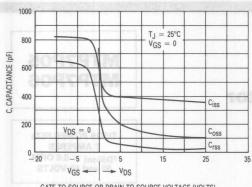
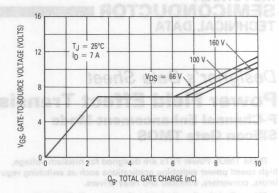


Figure 10. Thermal Response





GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

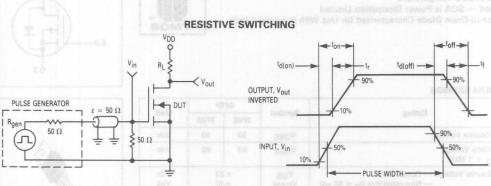
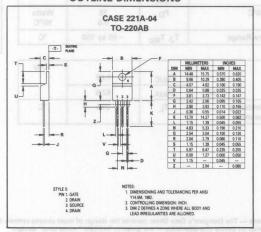


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

P-Channel Enhancement-Mode Silicon Gate TMOS

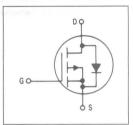
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MTP7P05 MTP7P06

TMOS POWER FETS 7 AMPERES rDS(on) = 0.6 OHM 50 and 60 VOLTS





MAXIMUM RATINGS

Pating	Completed.	MTP		TUC It-
Rating	Symbol	7P05	7P06	Unit
Drain-Source Voltage	V _{DSS}	50	60	Vdc
Drain-Gate Voltage (R _{GS} = 1 MΩ)	V _{DGR}	50	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive (t _p ≤ 50 μs)	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current Continuous Pulsed	IDM	7 [MHQ 21].JTUO		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C



Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Max	Unit
FF CHARACTERISTICS					1	201
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)		MTP7P05 MTP7P06	V(BR)DSS	50 60	-	Vdc
Zero Gate Voltage Drain Current (V _{DS} = Rated V _{DSS} , V _{GS} = 0) (V _{DS} = Rated V _{DSS} , V _{GS} = 0, 1	ГJ = 125°C)	W V	IDSS	72/	10 100	μAdc
Gate-Body Leakage Current, Forwa	rd (VGSF = 20 Vdc,	V _{DS} = 0)	IGSSF	7-73	100	nAdc
Gate-Body Leakage Current, Revers	se (VGSR = 20 Vdc,	$V_{DS} = 0$	IGSSR		100	nAdc
N CHARACTERISTICS*	150	à l			100	5
Gate Threshold Voltage (V _{DS} = V ₀ T _J = 100°C	GS, ID = 1 mA)	a Liv	VGS(th)	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 3.5 Adc)	RO DI	QI	rDS(on)	SOURCE VOLTA	0.6	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 7 Adc) (I _D = 3.5 Adc, T _J = 100°C)			V _{DS} (on)	Region Chy	4.2	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 3.5 A)			9FS	1.5		mhos
YNAMIC CHARACTERISTICS		W. FTT	1 XX X			20
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	Ciss		700	pF	
Output Capacitance		Coss	1-1-	400	81	
Reverse Transfer Capacitance	See Figure 11		C _{rss}	XV	150	
WITCHING CHARACTERISTICS* (TJ	= 100°C)	29		1/1		
Turn-On Delay Time		E &	td(on)	7	40	ns
Rise Time		D = 0.5 Rated ID	tr	1-1	120	
Turn-Off Delay Time		50 ohms) s 9, 13 and 14	td(off)	- \	80	
Fall Time			tf	- 1	70	
Total Gate Charge	(Vpc = 0.8	Rated V _{DSS} ,	Qg	12 (Typ)	16	nC
Gate-Source Charge	ID = Rated I	$V_{GS} = 10 V$	Qgs	7 (Typ)		0
Gate-Drain Charge	See F	igure 12	Qgd	5 (Typ)	DIND SOA	1
OURCE DRAIN DIODE CHARACTER	ISTICS*		zolsahesae	ranefer Charr	T,E mugP	
Forward On-Voltage	(le =	Rated I _D	V _{SD}	1.8 (Typ)	2.5	Vdc
Forward Turn-On Time	VGS	3 = 0)	ton	Limited	by stray ind	uctance
Reverse Recovery Time	221 3 22		t _{rr}	325 (Typ)		ns
NTERNAL PACKAGE INDUCTANCE	TO-220)	\$ /				209
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		Ld	3.5 (Typ) 4.5 (Typ)		nH	
(Measured from the drain lead 0	Internal Source Inductance (Measured from the source lead 0.25" from package to center of pad)					= (T

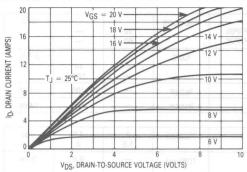


Figure 1. On-Region Characteristics

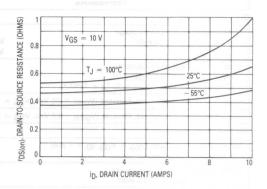


Figure 2. Gate-Threshold Voltage Variation With Temperature

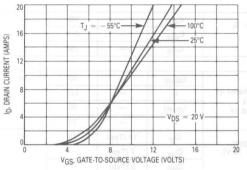


Figure 3. Transfer Characteristics

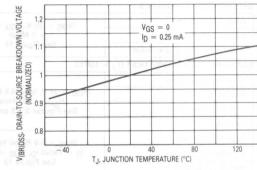


Figure 4. Breakdown Voltage Variation
With Temperature

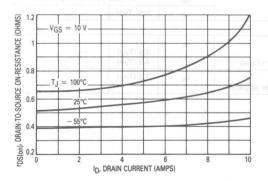


Figure 5. On-Resistance versus Drain Current

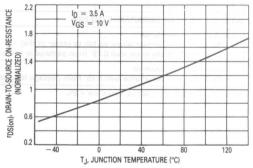


Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

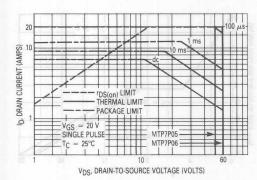


Figure 7. Maximum Rated Forward Biased Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V(\mbox{\footnotesize BR})\mbox{\footnotesize DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

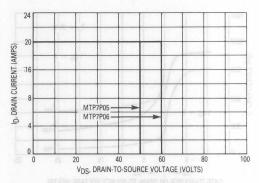


Figure 8. Maximum Rated Switching Safe Operating Area

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta}JC}$$

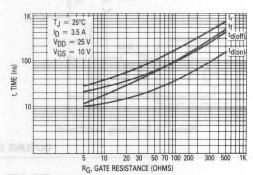


Figure 9. Resistive Switching Time Variation versus Gate Resistance

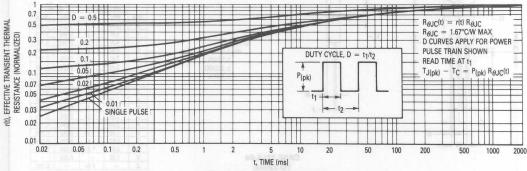


Figure 10. Thermal Response

TYPICAL CHARACTERISTICS

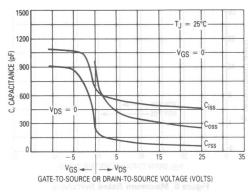
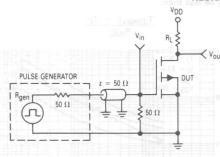


Figure 12. Capacitance Variation

Figure 13. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING





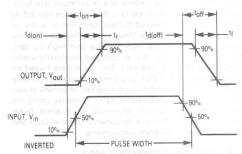
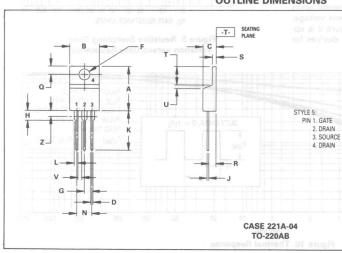


Figure 15. Switching Waveforms

OUTLINE DIMENSIONS



IM Z L		701-	uene	
EAD IF			HERE ALL E ALLOWE	
	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	14.48	15.75	0.570	0.620
В	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
Н	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
٧	1.15	_	0.045	_
Z	_	2.04	_	0.080

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

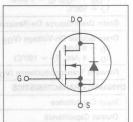
N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FETS 8 AMPERES rDS(on) = 0.5 OHM 80 and 100 VOLTS



MAXIMUM RATINGS

Det	0 1 1	MTM or MTP		Unit	
Rating	Symbol	8N08	8N10	Unit	
Drain-Source Voltage	V _{DSS}	80	100	Vdc	
Drain-Gate Voltage (RGS = 1 M Ω)	V _{DGR}	80 00	100	Vdc	
Gate-Source Voltage — Continuous — Non-repetitive (t _p ≤ 50 μs)	V _{GS} V _{GSM}		20 40	Vdc Vpk	
Drain Current	I _D		B i sea	Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75 0.6		Watts W/°C	
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150		°C	



CASE 221A-04 TO-220AB

THERMAL CHARACTERISTICS

Thermal Resistance				°C/W
Junction to Case		$R_{\theta JC}$	1.67	
Junction to Ambient	TO-220	$R_{\theta JA}$	62.5	on tab to ce
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Chara	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					,
Drain-Source Breakdown Voltage $(V_{GS} = 0, I_{D} = 0.25 \text{ mA})$	MTP8N08 MTP8N10	V _{(BR)DSS}	80 100	BU DIE	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS =	0, T _J = 125°C)	IDSS	osemen os-	0.2	mAdo
Gate-Body Leakage Current, Forwa	rd (VGSF = 20 Vdc, VDS = 0)	IGSSF	_	100	nAdc
Gate-Body Leakage Current, Revers	e (V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR	ទោញរម្នាច់ រប	100	nAdc
N CHARACTERISTICS*	-rigar grand	STATE OF SWEET	isla valisa huv	pays chart	
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C	TMOS	V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	V _{GS} = 10 Vdc, I _D = 4 Adc)	rDS(on)	D - Hillotor	0.5	Ohm
$ \begin{array}{ll} \mbox{Drain-Source On-Voltage (V}_{\mbox{GS}} = 1 \\ \mbox{(I}_{\mbox{D}} = 8 \mbox{ Adc)} \\ \mbox{(I}_{\mbox{D}} = 4 \mbox{ Adc, T}_{\mbox{J}} = 100^{\circ}\mbox{C)} \end{array} $	V _{DS(on)}	namplead Hassantan	4.8 4	Vdc	
Forward Transconductance (V _{DS} =	15 V, I _D = 4 A)	9FS	1.5	_	mhos
YNAMIC CHARACTERISTICS					
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz})$	C _{iss}	_	400	pF
Output Capacitance		Coss	_	350	
Reverse Transfer Capacitance	See Figure 11	C _{rss}		100	
WITCHING CHARACTERISTICS* (TJ	= 100°C)	Syn		gwasii	
Turn-On Delay Time	01046 8048	t _{d(on)}	_	50	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r		120	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	_	50	
Fall Time	and one are	tf	====	60	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Q_g	13 (Typ)	30	nC
Gate-Source Charge	shalp = Rated Ip, VGS = 10 V)	Qgs	6 (Typ)	_	
Gate-Drain Charge	See Figure 12	Q _{gd}	7 (Typ)	_	
OURCE DRAIN DIODE CHARACTERI	STICS*	g	25/36		
Forward On-Voltage	(Is = Rated In	V _{SD}	1.5 (Typ)	3	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	uctance
Reverse Recovery Time		t _{rr}	300 (Typ)	oma a .	ns
ITERNAL PACKAGE INDUCTANCE (TO-220)				
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		A Ld	3.5 (Typ) 4.5 (Typ)	_	nH
Internal Source Inductance (Measured from the source lead	0.25" from package to source bond pad.)	L _S	7.5 (Typ)	nol n 	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

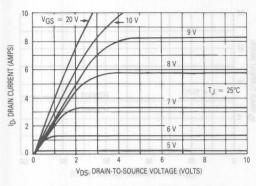


Figure 1. On-Region Characteristics

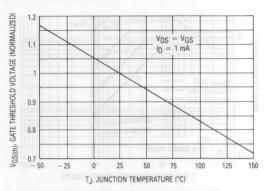


Figure 2. Gate-Threshold Voltage Variation With Temperature

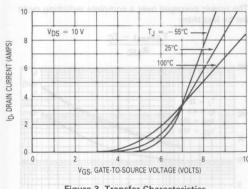


Figure 3. Transfer Characteristics

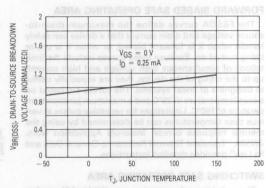


Figure 4. Breakdown Voltage Variation With Temperature

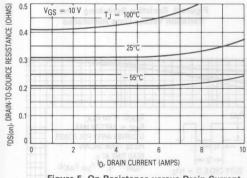


Figure 5. On-Resistance versus Drain Current

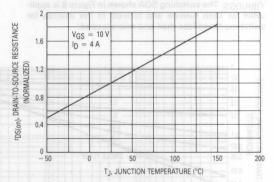


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

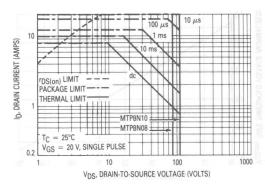


Figure 7. Maximum Rated Forward Biased Safe Operating Area

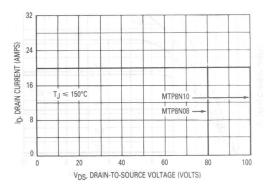


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

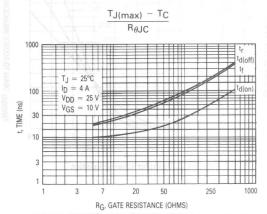


Figure 9. Resistive Switching Time Variation versus Gate Resistance

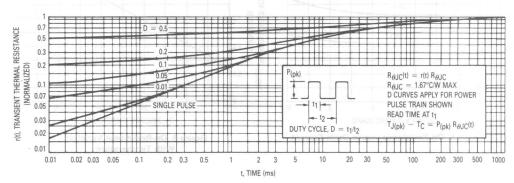
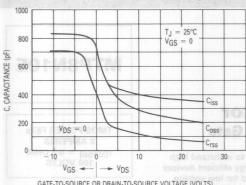


Figure 10. Thermal Response



VGS, GATE-TO-SOURCE VOLTAGE (VOLTS) $T_J = 25^{\circ}C$ 12 $I_D = 8 A$ 48 V 30 V VDS = 20 1 12 Q_g, TOTAL GATE CHARGE (nC)

GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

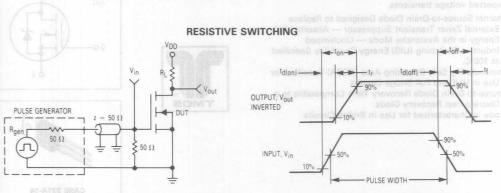
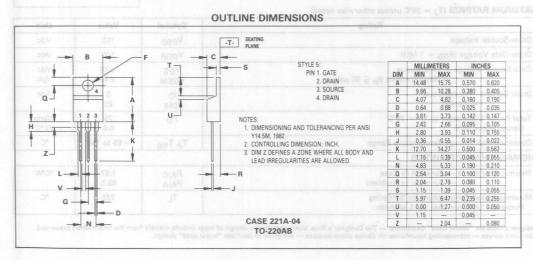


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

TMOS IV

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate

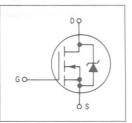
This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace
 External Zener Transient Suppressor Absorbs High
 Energy in the Avalanche Mode Unclamped
 Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits



MTP8N10E

TMOS POWER FETS 8 AMPERES rDS(on) = 0.5 OHM 100 VOLTS





MAXIMUM RATINGS (T.J = 25°C unless otherwise noted)

Rating		Value	Unit
Drain-Source Voltage	V _{DSS}	100	Vdc
Drain-Gate Voltage (R _{GS} = 1 MΩ)	VDGR	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50~\mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	IDM	8 20	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	R_{θ} JC R_{θ} JA	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

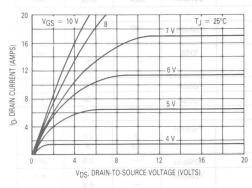
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Min	Max	Unit
OFF CHARACTERISTICS	T 2 12 12 12 12 12 12 12 12 12 12 12 12 1			NIN DE	
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)			100		Vdc
Zero Gate Voltage Drain Current $(V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0)$ $(V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0,\ T_{J}$	= 125°C)	IDSS		10 100	μΑ
Gate-Body Leakage Current, Forward	(V _{GSF} = 20 Vdc, V _{DS} = 0)	IGSSF	++	100	nAdc
Gate-Body Leakage Current, Reverse	(V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR		100	nAdc
ON CHARACTERISTICS*					-7/1
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = 1 \text{ mA})$ $T_J = 100^{\circ}C$	8.6	V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V	GS = 10 Vdc, I _D = 4 Adc)	rDS(on)	1 - 8	0.5	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 8 Adc) (I _D = 4 Adc, T _J = 100°C)			10-SOURCE VOL	4.8	Vdc
Forward Transconductance (VDS =	9 _{FS}	4	_	mhos	
DRAIN-TO-SOURCE AVALANCHE CHAI	RACTERISTICS				
Unclamped Drain-to-Source Avalanche Energy See Figures 14 and 15 (ID = 20 A, VDD = 25 V, TC = 25°C, Single Pulse, Non-repetitive) (ID = 8 A, VDD = 25 V, TC = 25°C, P.W. \leq 200 μ s, Duty Cycle \leq 1%) (ID = 3.2 A, VDD = 25 V, TC = 100°C, P.W. \leq 200 μ s, Duty Cycle \leq 1%)		W _{DSR}		80 170 70	mJ
DYNAMIC CHARACTERISTICS	5 6	50-1/1	0 8s = 1		
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss		600	pF
Output Capacitance	f = 1 MHz	Coss	N + 1	400	
Reverse Transfer Capacitance	See Figure 16	Crss	M+	100	
SWITCHING CHARACTERISTICS* (TJ =	= 100°C)				
Turn-On Delay Time		td(on)	-	50	ns
Rise Time	$(V_{DD} = 25 \text{ V}, I_{D} = 4 \text{ A})$	t _r	+///	80	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figure 9	td(off)	+ 1	100	
Fall Time	0 02- 01	tf		80	
Total Gate Charge	(VDS = 0.8 Rated VDSS,	Q_g	15 (Typ)	30	nC
Gate-Source Charge	ID = Rated ID, VGS = 10 V)	Q_{gs}	7.5 (Typ)	igus a 3. Tr	17
Gate-Drain Charge	See Figures 17 and 18	Q_{gd}	7.5 (Typ)	_	
SOURCE DRAIN DIODE CHARACTERIS	TICS*				
Forward On-Voltage	(Is = 4 A	V _{SD}	1.4 (Typ)	1.7	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray inc	ductance
Reverse Recovery Time	vor = aav	t _{rr}	70 (Typ)		ns
NTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw (Measured from the drain lead 0.2)	Ld	3.5 (Typ) 4.5 (Typ)	1991 = LT	nH	
Internal Source Inductance (Measured from the source lead 0.				123	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

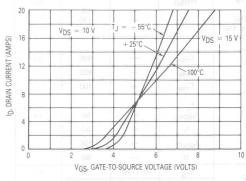
TYPICAL ELECTRICAL CHARACTERISTICS



VGS(th), GATE THRESHOLD VOLTAGE (NORMALIZED) 1.2 $V_{DS} = V_{GS}$ $I_D = 1 \text{ mA}$ 1.1 0.9 0.8 0.7 50 - 25 25 50 75 100 125 150 TJ, JUNCTION TEMPERATURE (°C)

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation With Temperature



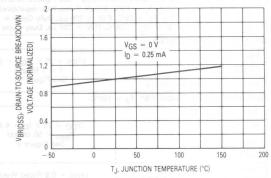
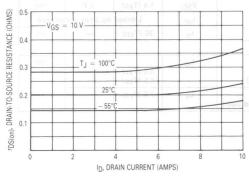


Figure 3. Transfer Characteristics





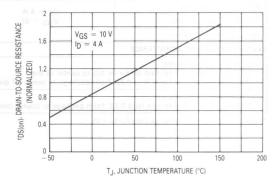


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

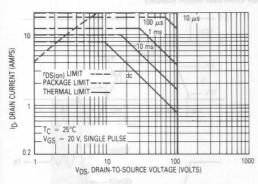


Figure 7. Maximum Rated Forward Biased Safe Operating Area

Figure 8. Maximum Rated Switching
Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

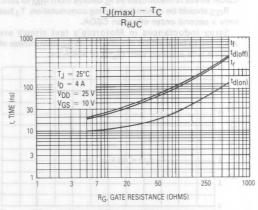


Figure 9. Resistive Switching Time Variation versus Gate Resistance

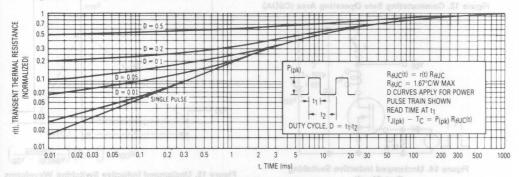


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of IFM and peak VDS for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so $dl_{\rm S}/dt$ is specified with a maximum value. Higher values of $dl_{\rm S}/dt$ require an appropriate derating of $l_{\rm FM}$, peak Vps or both. Ultimately $dl_{\rm S}/dt$ is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during $t_{\rm TF}$ as the diode goes from conduction to reverse blocking.

V_{DS(pk)} is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

 V_R is specified at 80% of $V_{\left(BR\right)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

RGS should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dl_{S}/dt of 400 A/ μ s.

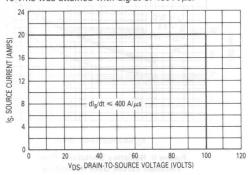


Figure 12. Commutating Safe Operating Area (CSOA)

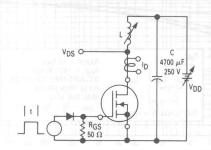


Figure 14. Unclamped Inductive Switching
Test Circuit

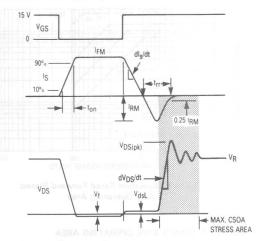


Figure 11. Commutating Waveforms

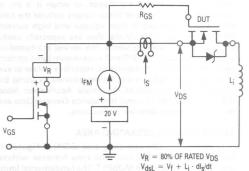


Figure 13. Commutating Safe Operating Area
Test Circuit

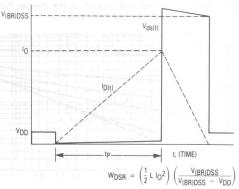
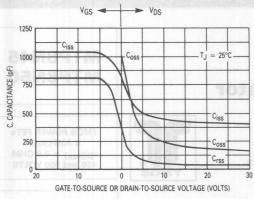


Figure 15. Unclamped Inductive Switching Waveforms



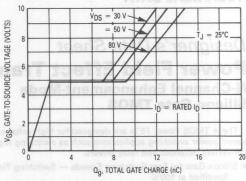
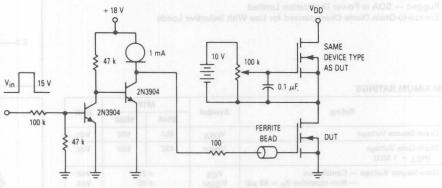


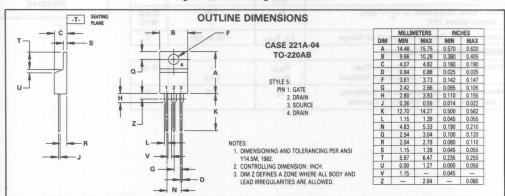
Figure 16. Capacitance Variation

Figure 17. Gate Charge versus Gate-To-Source Voltage



 $V_{in} = 15 V_{pk}$; PULSE WIDTH $\leq 100 \mu s$, DUTY CYCLE $\leq 10\%$

Figure 18. Gate Charge Test Circuit



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

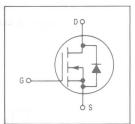
N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads







MAXIMUM RATINGS

P. et .	0 1 1	MTP		N.,	
Rating	Symbol	8N45 8N50		Unit	
Drain-Source Voltage	V _{DSS}	450	500	Vdc	
Drain-Gate Voltage (RGS = 1 M Ω)	V _{DGR}	450	500	Vdc	
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± ±	20 40	Vdc Vpk	
Continuous	ID D IDM	SEWOTH &	В	Adc	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	ю зиці	²⁵	Watt:	
Operating and Storage Temperature Range	T _J , T _{stg}	- 65	to 150	°C	

THERMAL CHARACTERISTICS

THE THINKS OF PARTY OF ETHIC 1100			
Thermal Resistance — Junction to Case — Junction to Ambient	R_{θ} JC R_{θ} JA	1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TAO 7 TL HARG S	275	°C

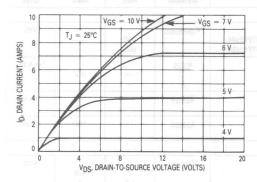


Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Char	Symbol	Min	Max	Unit	
FF CHARACTERISTICS	1 1 9 1 1	T ISS	welver - nov		10
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	MTP8N45 MTP8N50	V _(BR) DSS	450 500	70 <u>= 2</u> 8°C	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = Rated\ V_{DSS},\ V_{GS} = 0$) ($V_{DS} = 0.8\ Rated\ V_{DSS},\ V_{GS} = 0$)	0, T _J = 125°C)	IDSS		0.2	mAdd
Gate-Body Leakage Current, Forwa (VGSF = 20 Vdc, VDS = 0)	rd 000 9	IGSSF	-	100	nAdo
Gate-Body Leakage Current, Reversion (VGSR = 20 Vdc, VDS = 0)	Se 08.0	IGSSR		100	nAdd
N CHARACTERISTICS*	\$ 0.70				3
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C	(a	VGS(th)	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 4 Adc)	Figure 2. Gat	rDS(on)	Dn-Rogion C	0.8	Ohm
Drain-Source On-Voltage ($V_{GS} = 1$) ($I_D = 8$ Adc) ($I_D = 4$ Adc, $T_J = 100$ °C)	V _{DS(on)}	=	7.2 6.4	Vdc	
Forward Transconductance (V _{DS} = 10 V, I _D = 4 A)	1.2 V _{CS} = 0	9FS	4	V0S = 20 V	mhos
YNAMIC CHARACTERISTICS	8.0 = 0	1 1///			
Input Capacitance	$V_{DS} = 25 \text{ V, } V_{GS} = 0,$	Ciss		1600	pF
Output Capacitance	f = 1 MHz)	Coss	1-1	350	
Reverse Transfer Capacitance	See Figure 11	C _{rss}	N-L	150	
WITCHING CHARACTERISTICS* (TJ	= 100°C)				
Turn-On Delay Time	Valley	td(on)		60	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	tr	17/1	150	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	-1-25-3	200	
Fall Time C7 SRUTARSMST WORDS	W 47	and t _f spans	Y STRUCK OT ST	120	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Q_g	40 (Typ)	60	nC
Gate-Source Charge	ID = Rated ID, VGS = 10 V)	Qgs	20 (Typ)	Higure 3.	
Gate-Drain Charge	See Figure 12	Q _{gd}	20 (Typ)	_	
OURCE DRAIN DIODE CHARACTER	ISTICS*				
Forward On-Voltage	VIV = SAV (IS = Rated ID	V _{SD}	1.1 (Typ)	2	Vdc
Forward Turn-On Time	$V_{GS} = 0$	ton	Limited	by stray indu	uctance
Reverse Recovery Time		t _{rr}	600 (Typ)	0-001 = LT	ns
NTERNAL PACKAGE INDUCTANCE	- 8				
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		Ld	3.5 (Typ) 4.5 (Typ)	ores =	nH
Internal Source Inductance	Ls	7.5 (Typ)			

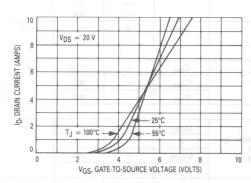
TYPICAL ELECTRICAL CHARACTERISTICS



1.1 VDS = VGS ID = 1 mA ID

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation With Temperature



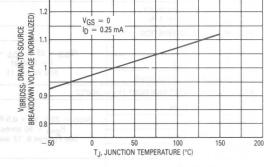
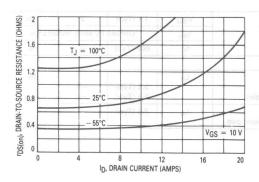


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation With Temperature



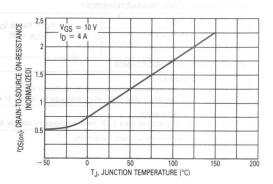


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

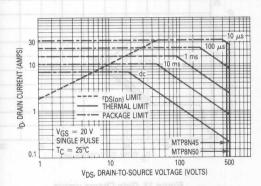


Figure 7. Maximum Rated Forward Biased Safe Operating Area

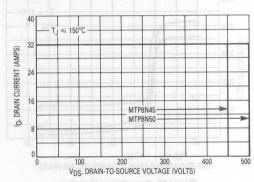


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

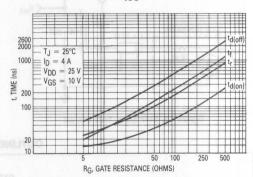


Figure 9. Resistive Switching Time Variation versus Gate Resistance

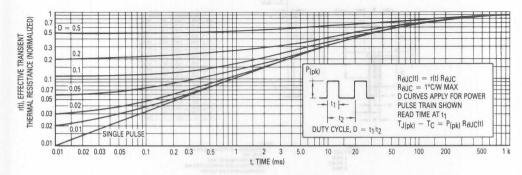


Figure 10. Thermal Response

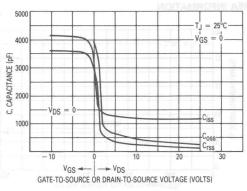


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus
Gate-to-Source Voltage

RESISTIVE SWITCHING

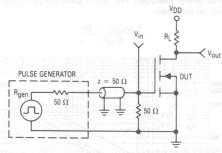


Figure 13. Switching Test Circuit

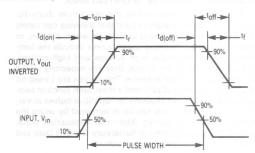
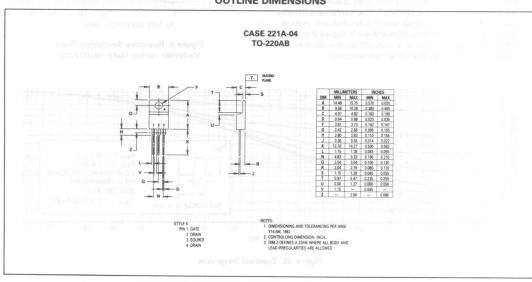


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

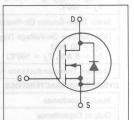
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTP10N05 MTP10N06

TMOS POWER FETS 10 AMPERES rDS(on) = 0.28 OHM 50 and 60 VOLTS



MAXIMUM RATINGS

Rating			MTP		1001 =	
an 08	ating	(2015)	Symbol	10N05	10N06	Unit
Drain-Source Voltage		1	V _{DSS}	50	60	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)		(No)67	VDGR	50	60	Vdc
Gate-Source Voltage —	Continuous Non-repetitive (t	₀ ≤ 50 μs)	V _{GS} V _{GSM}		20 40	Vdc Vpk
Drain Current Continuous Pulsed	(qyT) X	Oge Ogd	I _D	10 28		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C		PD	75 0.6		Watts W/°C	
Operating and Storage Temperature Range		T _J , T _{stg}	-65	to 150	°C	

THERMAL CHARACTERISTICS

Thermal Resistance				°C/W
Junction to Case		$R_{\theta JC}$	1.67	
Junction to Ambient	TO-220	$R_{\theta JA}$	62.5	of fail no w
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C



MTP10N05 MTP10N06 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

(Characteristic			Min	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Volta (VGS = 0, I _D = 0.25 mA)	MTI	P10N05 P10N06	V _(BR) DSS	50 60	0	Vdc
Zero Gate Voltage Drain Currer (VDS = Rated VDSS, VGS = (VDS = Rated VDSS, VGS =	0)	1	IDSS	em <u>a</u> on.	10 100	μAdc
Gate-Body Leakage Current, Fo	orward (VGSF = 20 Vdc, VDS = 0))	IGSSF	-0.41	100	nAdc
Gate-Body Leakage Current, Re	everse (VGSR = 20 Vdc, VDS = 0)	IGSSR	malesta in an a	100	nAdc
N CHARACTERISTICS*	210	ashugan pr	ch as switchin	plications su	12111	
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C			VGS(th)	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resista	nce ($V_{GS} = 10 \text{ Vdc}$, $I_D = 5 \text{ Adc}$)	Nosq2 AC	rDS(on)	Viln al adV	0.28	Ohm
Drain-Source On-Voltage (VGS = 10 V) (ID = 10 Adc) (ID = 5 Adc, T_J = 100°C)			V _{DS(on)}	Dasigation	3.4 2.8	Vdc
Forward Transconductance ($V_{DS} = 15 \text{ V}, I_{D} = 5 \text{ A}$)			9FS	2.5	_	mhos
YNAMIC CHARACTERISTICS					v	
Input Capacitance	(V _{DS} = 25 V, V _{GS}	= 0.	C _{iss}	_	400	pF
Output Capacitance	f = 1 MHz)	-,	Coss		350	
Reverse Transfer Capacitance	See Figure 11		C _{rss}	_	100	H U!
WITCHING CHARACTERISTICS	(T _J = 100°C)	Continue			eriorai\)	
Turn-On Delay Time	tordes torde		td(on)	_	50	ns
Rise Time	$(V_{DD} = 25 \text{ V}, I_{D} = 0.5 \text{ I})$		t _r	_	120	
Turn-Off Delay Time	R _{gen} = 50 ohms See Figures 9, 13 an	nd 14	td(off)	_	50	
Fall Time			tf	_	60	
Total Gate Charge	(V _{DS} = 0.8 Rated V	nee.	Q_g	13 (Typ)	26	nC
Gate-Source Charge	ID = Rated ID, VGS =		Qgs	6 (Typ)	_	
Gate-Drain Charge	See Figure 12		Q_{gd}	7 (Typ)	_	10.00
OURCE DRAIN DIODE CHARAC	TERISTICS*	MO				
Forward On-Voltage	(Is = Rated ID	0.	V _{SD}	1.7 (Typ)	3	Vdc
Forward Turn-On Time	V _{GS} = 0)			Limited	by stray ind	uctance
Reverse Recovery Time			t _{rr}	300 (Typ)	213 37	ns
NTERNAL PACKAGE INDUCTAN	ICE WAS					
	screw on tab to center of die) ad 0.25" from package to center o	f die) ALAR	L _d	3.5 (Typ) 4.5 (Typ)	_	nH
,	au ole moni puonago to conter o			(17)		1

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

Internal Source Inductance

(Measured from the source lead 0.25" from package to source bond pad.)

Ls

7.5 (Typ)

3

TYPICAL ELECTRICAL CHARACTERISTICS

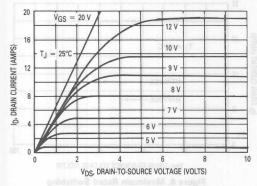


Figure 1. On-Region Characteristics

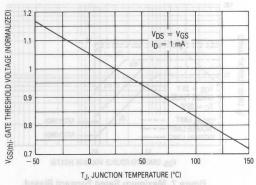


Figure 2. Gate-Threshold Voltage Variation With Temperature

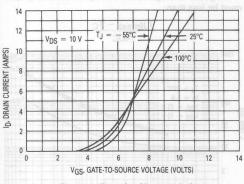


Figure 3. Transfer Characteristics

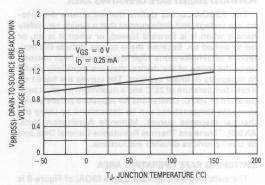


Figure 4. Breakdown Voltage Variation
With Temperature

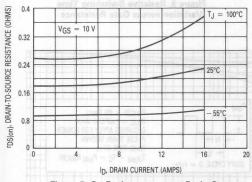


Figure 5. On-Resistance versus Drain Current

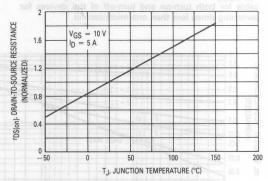


Figure 6. On-Resistance Variation
With Temperature

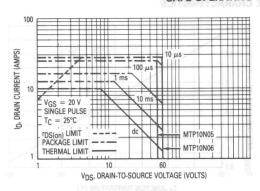


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

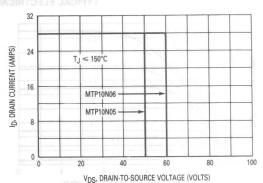


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

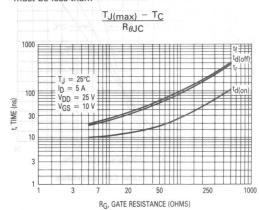


Figure 9. Resistive Switching Time Variation versus Gate Resistance

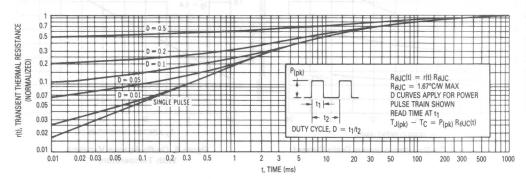
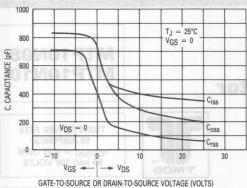


Figure 10. Thermal Response



GATE-TO-SOURCE VOLTAGE (VOLTS) T_J = 25°C $I_D = 10 A$ 48 V = 20 V 28 104 12 Qq, TOTAL GATE CHARGE (nC)

Figure 11. Capacitance Variation

Figure 12 Gate Charge versus Gate-to-Source Voltage

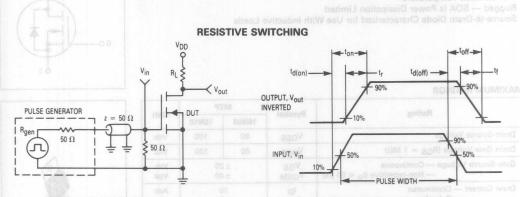
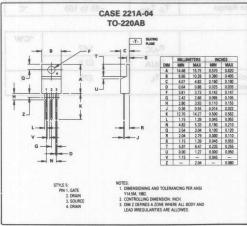


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

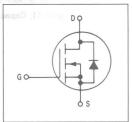
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS 10 AMPERES rDS(on) = 0.33 OHM 80 and 100 VOLTS



MAXIMUM RATINGS

	GETREV	MTP		
Rating	Symbol	10N08	10N10	Unit
Drain-Source Voltage	V _{DSS}	80	100	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	80	100	Vdc
	V _{GS} V _{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	I _D I _{DM}	10 25		Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	- 65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		$R_{\theta JC}$	1,67	°C/W
Junction to Ambient	TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C



MTP10N08 MTP10N10 CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Cha	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS		- 007		2.88	= (1
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	MTP10N08 MTP10N10	V _{(BR)DSS}	80 100	7=	Vdc
Zero Gate Voltage Drain Current $(V_{DS} = Rated V_{DSS}, V_{GS} = 0)$ $(V_{DS} = Rated V_{DSS}, V_{GS} = 0,$	IDSS		10 100	μAdc	
Gate-Body Leakage Current, Forwa	ard (VGSF = 20 Vdc, VDS = 0)	IGSSF	- 1	100	nAdc
Gate-Body Leakage Current, Rever	se (VGSR = 20 Vdc, VDS = 0)	IGSSR		100	nAdc
ON CHARACTERISTICS*	F0 #8				IN.
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C	0 & − 08 − ≪ 08) SMUL _E T	VGS(th)	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance	(V _{GS} = 10 Vdc, I _D = 5 Adc)	rDS(on)	n-Region G	0.33	Ohm
Drain-Source On-Voltage (VGS = $(I_D = 10 \text{ Adc})$ $(I_D = 5 \text{ Adc}, T_J = 100^{\circ}\text{C})$	V _{DS} (on)	=	4 3.3	Vdc	
Forward Transconductance (V _{DS}	9FS	2.5		mhos	
YNAMIC CHARACTERISTICS	0 = pay 2 2 2 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	7// 25	00		
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz})$	Ciss	-	600	geV pF
Output Capacitance		Coss	-	400	13
Reverse Transfer Capacitance	See Figure 11	C _{rss}	- 1	80	
WITCHING CHARACTERISTICS* (T.	J = 100°C)				
Turn-On Delay Time	3 8 8	td(on)		50	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	tr	1/2	150	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	1	100	
Fall Time		tf		50	السار
Total Gate Charge	(VDS = 0.8 Rated VDSS,	Q_g	13 (Typ)	30	nC
Gate-Source Charge	ID = Rated ID, VGS = 10 V)	Qgs	6 (Typ)	_	
Gate-Drain Charge	See Figure 12	Qgd	7 (Typ)	Figure 3, T	
OURCE DRAIN DIODE CHARACTER	IISTICS*				
Forward On-Voltage	(Is = Rated Ip	V _{SD}	1.7 (Typ)	3	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	luctance
Reverse Recovery Time		t _{rr}	700 (Typ)		ns
NTERNAL PACKAGE INDUCTANCE	A 0 = m 8.1 \$			Max	4
Internal Drain Inductance (Measured from the contact scre (Measured from the drain lead (ew on tab to center of die) .25" from package to center of die)	L _d	3.5 (Typ) 4.5 (Typ)		nH 8
Internal Source Inductance (Measured from the source lead	0.25" from package to source bond pa	L _S	7.5 (Typ)	_	1

*Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

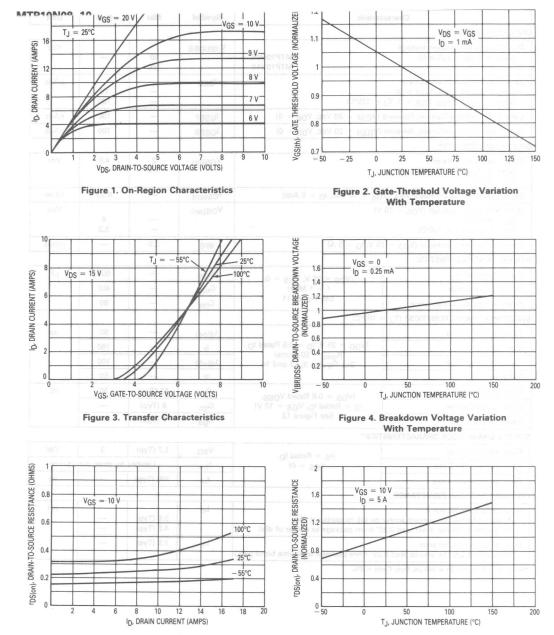


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

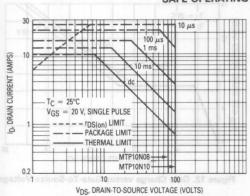


Figure 7. Maximum Rated Forward Biased Safe Operating Area

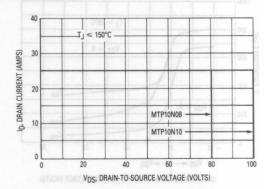


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

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SWITCHING SAFE OPERATING AREA

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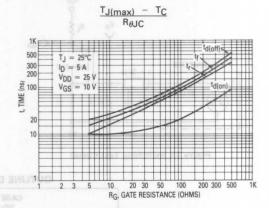


Figure 9. Resistive Switching Time versus Gate Resistance

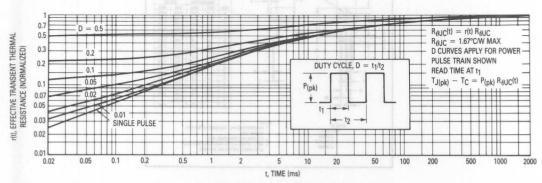
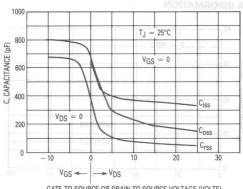


Figure 10. Thermal Response



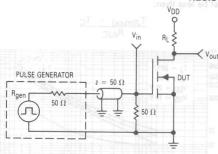
 $T_{\rm J}=25^{\circ}{\rm C}$ VGS, GATE SOURCE VOLTAGE (VOLTS) ID = 10 A 50 V VDS = 30 V Qq, TOTAL GATE CHARGE (nC)

GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 12. Gate Charge versus Gate-To-Source Voltage

Figure 11. Capacitance Variation

RESISTIVE SWITCHING





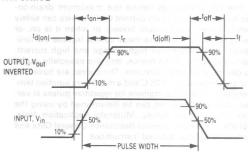
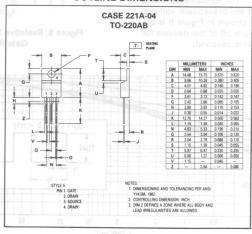


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

TMOS IV

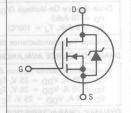
Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits



TMOS POWER FETS 10 AMPERES rDS(on) = 0.25 OHM 100 VOLTS





TMOS

CASE 221A-04 TO-220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	gag ^O		Symbol	Value	Unit
Drain-Source Voltage	Dgd		V _{DSS}	100	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)			V _{DGR}	100	Vdc
	50 μs)	(IS = Rated ID	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous (447) 05 — Pulsed	79.7		ID IDM	10 25	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PJ F	center of dia)	P _D	75 0.6	Watts W/°C
Operating and Storage Temperature Range		ickage to center of die)	TJ, Tstg	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Character	istic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)		V _{(BR)DSS}	100	n 5	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ = 125°C)			=	10 100	μΑ
Gate-Body Leakage Current, Forward (V	GSF = 20 Vdc, V _{DS} = 0)	IGSSF	77 b	100	nAdc
Gate-Body Leakage Current, Reverse (Vo	GSR = 20 Vdc, V _{DS} = 0)	IGSSR		100	nAdo
ON CHARACTERISTICS*	2120 11031110 20	MANAGE THE	HIND CHILD	KSGTPN YET	
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_{D} = 1 \text{ mA})$ $T_{J} = 100^{\circ}\text{C}$	VGS(th)	2 1.5	4.5 4	Vdc	
Static Drain-Source On-Resistance (VGS	rDS(on)	ni entitons in	0.25	Ohm	
Drain-Source On-Voltage (V _{GS} = 10 V) and about an attack applied (I _D = 10 Adc) (I _D = 5 Adc, T _J = 100°C)			articularly v ing a rs a arr tents -	2.7 2.4	Vdc
Forward Transconductance (V _{DS} = 15)	9FS	s0 s4d0 n	E 0	mho	
RAIN-TO-SOURCE AVALANCHE CHARAC	CTERISTICS night adv	ssor — Abso	end Suppre	ana sa	-90
$ \begin{array}{lll} \mbox{Unclamped Drain-to-Source Avalanche} \\ \mbox{(ID} = 25 \mbox{ A, V}_{\mbox{DD}} = 25 \mbox{ V, T}_{\mbox{C}} = 25 \mbox{°C,} \\ \mbox{(ID} = 10 \mbox{ A, V}_{\mbox{DD}} = 25 \mbox{ V, T}_{\mbox{C}} = 25 \mbox{°C,} \\ \mbox{(ID} = 4 \mbox{ A, V}_{\mbox{DD}} = 25 \mbox{ V, T}_{\mbox{C}} = 100 \mbox{°C,} \\ \end{array} $	Single Pulse, Non-repetitive) P.W. ≤ 200 μs, Duty Cycle ≤ 1%)	WDSR	UIS) <u>E</u> nerg	60 100 40	mJ
DYNAMIC CHARACTERISTICS	WT E of eld	учерто Сетрану	T. ynewnas S		
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0,	C _{iss}	appid y	600	pF
Output Capacitance	f = 1 MHz) See Figure 16	Coss	6 nt (121) 101	400	
Reverse Transfer Capacitance		C _{rss}	_	100	
SWITCHING CHARACTERISTICS* (TJ = 1	00°C)				
Turn-On Delay Time	05.77	^t d(on)	_	50	ns
Rise Time	$(V_{DD} = 25 \text{ V, } I_{D} = 5 \text{ A} $ $R_{gen} = 50 \text{ ohms})$	t _r		80	_
Turn-Off Delay Time	See Figure 9	td(off)		100	
Fall Time		tf		80	
Total Gate Charge	(VDS = 0.8 Rated VDSS,	on seQgenro	15 (Typ)	30	nC
Gate-Source Charge	ID = Rated ID, VGS = 10 V) See Figures 17 and 18	Qgs	8 (Typ)	_	
Gate-Drain Charge		Q _{gd}	7 (Typ)		1-17
SOURCE DRAIN DIODE CHARACTERISTIC	S*		(ON)	= 257	
Forward On-Voltage	(IS = Rated ID	V _{SD}	1.4 (Typ)	1.7	Vdd
Forward Turn-On Time	$V_{GS} = 0$	ton	Limited	by stray inc	ductance
Reverse Recovery Time		t _{rr}	70 (Typ)	uema	ns
NTERNAL PACKAGE INDUCTANCE				TIOSILLA	
Internal Drain Inductance (Measured from the contact screw on (Measured from the drain lead 0.25" f		L _d	3.5 (Typ) 4.5 (Typ)	12 45 45 45 45 45 45 45 45 45 45 45 45 45	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)		L _S	7.5 (Typ)	(2015)	

TYPICAL ELECTRICAL CHARACTERISTICS

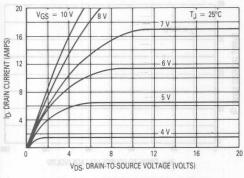


Figure 1. On-Region Characteristics

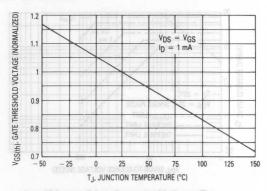


Figure 2. Gate-Threshold Voltage Variation
With Temperature

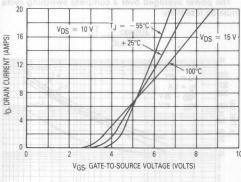


Figure 3. Transfer Characteristics

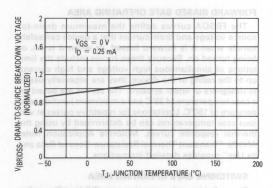


Figure 4. Breakdown Voltage Variation With Temperature

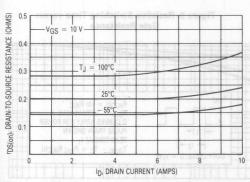


Figure 5. On-Resistance versus Drain Current

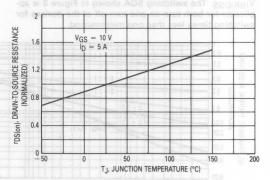


Figure 6. On-Resistance Variation With Temperature

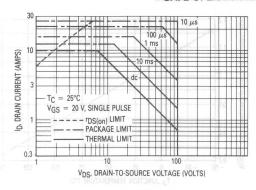


Figure 7. Maximum Rated Forward Biased Safe Operating Area

40 T_J ≤ 150°C 10 0 20 40 60 80 100 V_{DS}, DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

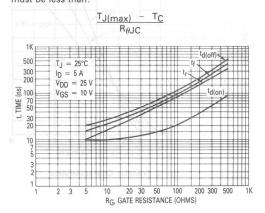


Figure 9. Resistive Switching Time versus
Gate Resistance

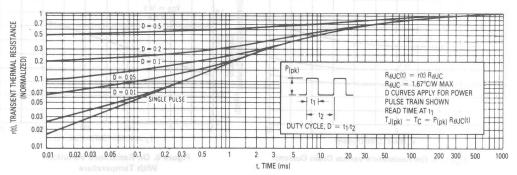


Figure 10. Thermal Response

3

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of IFM and peak VDS for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so $dl_{\rm S}/dt$ is specified with a maximum value. Higher values of $dl_{\rm S}/dt$ require an appropriate derating of $l_{\rm FM}$, peak $V_{\rm DS}$ or both. Ultimately $dl_{\rm S}/dt$ is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during $t_{\rm TF}$ as the diode goes from conduction to reverse blocking.

V_{DS(pk)} is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

 V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

RGS should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dl_{s}/dt of 400 A/ μ s.

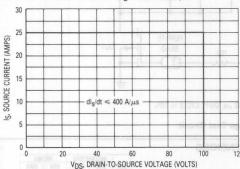


Figure 12. Commutating Safe Operating Area (CSOA)

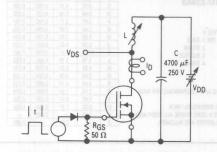


Figure 14. Unclamped Inductive Switching Test Circuit

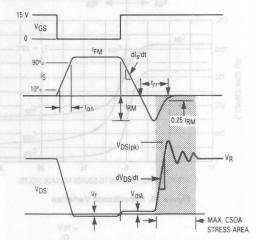


Figure 11. Commutating Waveforms

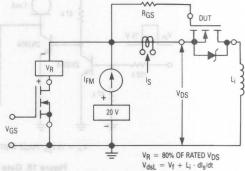


Figure 13. Commutating Safe Operating Area

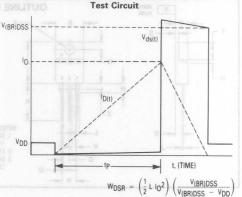


Figure 15. Unclamped Inductive Switching Waveforms

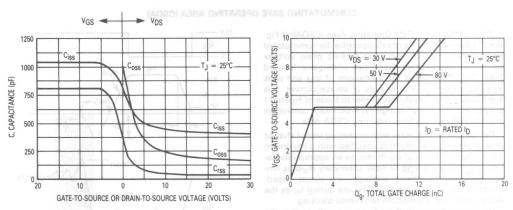


Figure 16. Capacitance Variation

Figure 17. Gate Charge versus Gate-To-Source Voltage

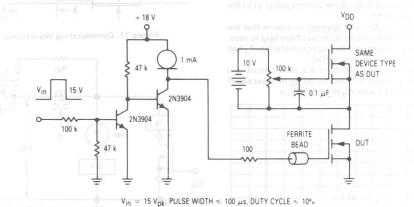
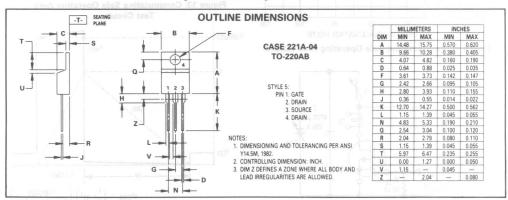


Figure 18. Gate Charge Test Circuit



MOTOROLA SEMICONDUCTOR **TECHNICAL DATA**

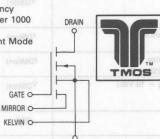
Advance Information

Power Field Effect Transistor

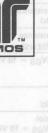
N-Channel Enhancement-Mode **Silicon Gate TMOS** with Current Sensing Capability

This TMOS Power FET with current sensing capability is designed for all power control applications where it is desirable to sense current such as in power supplies and motor controls. This device allows current sensing with minimum power

- "Lossless" Current Sensing for Maximum Efficiency - Sense Current is Reduced by a Factor of Over 1000
- Ideal for Short Circuit/Overload Protection
- Simplifies Many Circuits When Used With Current Mode Integrated Circuits Such as the MC34129
- Kelvin Source Contact to Maximize Accuracy • Rugged — SOA is Power Dissipation Limited
- Low rDS(on) 0.25 Ohms Maximum NOTES:
- Handling precautions to protect against electrostatic
- 1. Hambling precautions to protect against electrostatic discharge is mandatory.
 2. Do not use the mirror FET independent of the power FET.
 3. It is recommended that the mirror terminal (M) be shorted
- to the source terminal (S) when current sensing is not required.



SOURCE



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	VDSS	100	Vdc
Drain-to-Gate Voltage (R _{GS} = 1 MΩ)	VDGR	100	Vdc
Gate-to-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	±20 ±40	Vdc Vpk
Drain-to-Mirror Voltage	V _{DMS}	100	Vdc
Gate-to-Mirror Voltage	V _{GM}	±20	Vdc
Drain Current — Continuous — Pulsed	I _D	10 25	Adc
Sense Current — Continuous — Pulsed	IMM	6	mA
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	75 0.6	Watts W/°C
Operating and Storage Temperature Range	TJ, Tstg	-55 to 150	°C

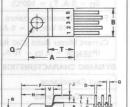
THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case Junction-to-Ambient	R _θ JC R _θ JA	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

MTP10N10M

TMOS SENSEFET 10 AMPERES rDS(on) = 0.25 OHM 100 VOLTS





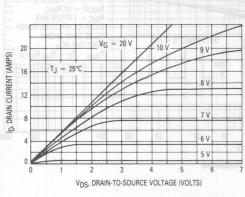
	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	15.49	15.88	0.610	0.625
В	9.91	10.41	0.390	0.410
C	4.32	4.57	0.170	0.180
D	0.71	0.81	0.028	0.032
F	20.83	21.59	0.820	0.850
G	1.45	1.96	0.057	0.077
H	12.70	13.69	0.500	0.539
J	0.38	0.64	0.015	0.025
K	21.46	23.50	0.845	0.925
L	8.00	8.38	0.315	0.330
P	4.32	4.70	0.170	0.185
Q	3.53	3.73	0.139	0.147
R	0.89	1.40	0.035	0.055
T	9.02	9.40	0.355	0.370
٧	4.70	5.46	0.185	0.215

CASE 314B-01

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Charact	teristics	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown V (VGS = 0, ID = 0.25 mA)	oltage	V _{(BR)DSS}	100	ımatıi	stril a	Vdc
Drain-to-Mirror Breakdown Voltage (VGS = 0, I _D = 0.25 mA)		V _(BR) DMS	100	ME b	eH	Vdc
Zero Gate Voltage Drain Curro $(V_{DS} = 100 \text{ V}, V_{GS} = 0)$ $(V_{DS} = 100 \text{ V}, V_{GS} = 0, T_{C})$		IDSS @	oW-tne	means 20h	0.2	mAdc
Gate-Body Leakage Current — (VGSF = 20 Vdc, VDS = 0)		IGSSF	ida q a0	ensing	100	nAdc
Gate-Body Leakage Current — (VGSR = 20 Vdc, VDS = 0)	Reverse Tewaq IIIa tal ben				T3 100	nAdc
N CHARACTERISTICS*	n minimum power	trive gnianes on	allowis curre	This device	.eleur	avern bria
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mAdd (T _J = 100°C)	DRAIN STATE CONTROL	VGS(th)	0 1.5 al	sing gr Ma aduc <u>—</u> by a	4.5 4	Vdc
Static Drain-to-Source On-Res (VGS = 10 Vdc, ID = 5 Add		rDS(on)	rectron d With Curte	0.16	0.25	Ohms
Static Drain-to-Mirror On-Resistance (VGS = 10 V, I _D = 10 A, R _{SENSE} = 0)		rDM(on)	Accuracy	288	Tiach	Ohms
Drain-to-Source On-Voltage (V _{GS} = 10 Vdc) (I _D = 10 A) (I _D = 5 A, T _J = 100°C)		VDS(on)	m — ostatio—	mis Maximii 1.9 1. agai nt electr	2.7	Vdc
Forward Transconductance (VGS = 10 Vdc, ID = 5 Adc)		9FS	5 2.5 word	ent to macrosor or commat the	Mary a	mhos
Current Mirror Ratio (Cell Ratio) (RSENSE = 0, ID = 10 A, VGS = 10 V)		n	1750	1800	1850	_
YNAMIC CHARACTERISTICS		*		-	2007	14 14 15
Input Capacitance	Value Unit	C _{iss}	_	police	500	pF
Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0$ f = 1 MHz	Coss	_	_	300	
Transfer Capacitance	See Figure 6	C _{rss}	_	_	100	1 145
WITCHING CHARACTERISTICS	S*					
Turn-On Delay Time	±20 Vdc	88 td(on)	_	гиошийпо0	50	ns
Rise Time	V _{DD} = 25 V, I _D = 5 A	t _r	sea oc - gn :	Mullade Incopt	150	
Turn-Off Delay Time	R _{gen} = 50 Ohms	t _d (off)			100	
Fall Time		tf			50	
Total Gate Charge	768 57 35	Og	_	16	25	nC
Gate-Source Charge	V _{DS} = 80 V, I _D = 10 A V _{GS} = 10 V	Qgs	_	7	onni i m	
Gate-Drain Charge See Figure 4		Mana Ogd	_	9	he <u>ulu</u> r.	
OURCE-DRAIN DIODE CHARA	CTERISTICS*	G ^q	-	Tg = 25°C	ne notraces	0.00
Forward On-Voltage	5 197 6.0	V _{SD}	_	2		Vdc
Forward Turn-On Time	I _S = 10 A	ton	991	20	= गवपुर छि	ns
Reverse Recovery Time		t _{rr}		700	arna <u>tu</u> rk i	et a gerial





GATE THRESHOLD VOLTAGE (NORMALIZED) 1.2 $V_{DS} = V_{GS}$ $I_{D} = 1 \text{ mA}$ 1.1 0.9 0.8 VGS(th), 25 50 75 100 125 TJ, JUNCTION TEMPERATURE (°C)

Figure 1. On-Region Characteristics Figure 2. Gate Threshold Voltage Variation with Temperature

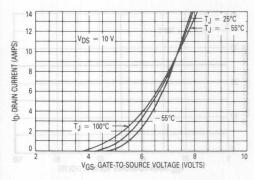


Figure 3. Transfer Characteristics

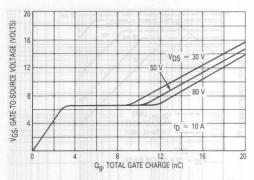


Figure 4. Stored Charge Variation

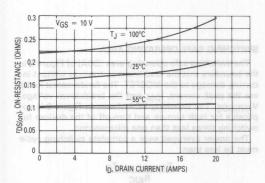


Figure 5. On-Resistance versus Drain Current

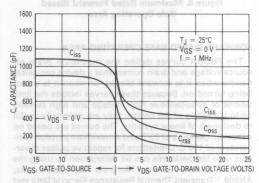


Figure 6. Capacitance Variation

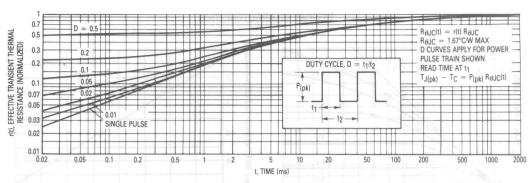


Figure 7. Thermal Response

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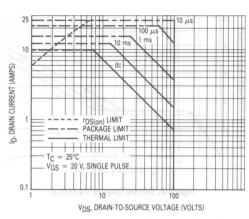


Figure 8. Maximum Rated Forward Biased
Safe Operating Area

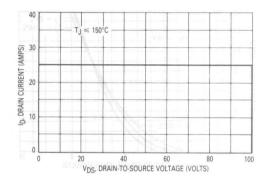


Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.



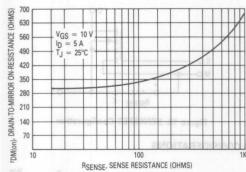


Figure 10. Drain-to-Mirror On-Resistance versus Sense Resistance

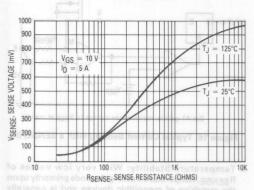


Figure 12. Sense Voltage versus Sense Resistance

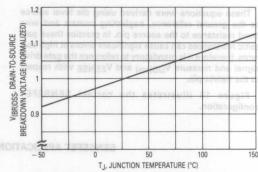


Figure 11. Normalized Drain-To-Source Breakdown
Voltage versus Temperature

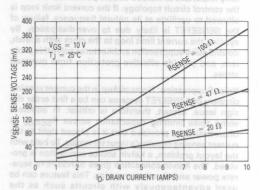


Figure 13. Drain Current versus Sense Voltage

USING SENSEFETS

In practical applications, less sense current will flow than that calculated by using the current mirror ratio, n. Shown in Figure 1 is a model of the SENSEFET. It is seen that RSENSE decreases the voltage across rDM(on) and decreases the sense current. An additional decrease in sense current occurs due to the decreased voltage across

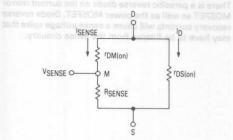


Figure 14. SENSEFET Model

the mirror transistors. For this reason, a modified current mirror ratio, n' must be calculated. The equation to calculate n' is derived from the MOSFET square law model in the linear region,

$$n' = \frac{n}{1 - \frac{V_{SE}(V_{GS} - V_{T} - 1/2 \ V_{SE})}{V_{DS(on)}(V_{GS} - V_{T} - 1/2 \ V_{DS(on)})}}$$

$$n' \approx \frac{n}{1 - V_{SE}/V_{DS(on)}}$$
(1)

(for VSE, VDS(on) < < VGS - VT).

Where, $V_{GS} = Gate\text{-to-Source Voltage},$ $V_{T} = Gate\text{-to-Source Threshold Voltage}$

and V_{SE} = Sense Voltage = $\frac{R_{SENSE} I_D}{n'}$. (2)

Hence, n' can be calculated from equation (1) and the result used in equation (2) to find the value of RSENSE. The value of RSENSE should be kept below 100 Ω for most accurate results.

as the ground reference, neglecting contact and wire bond resistance to the source pin. In practice these parasitic resistances can cause significant errors at high currents, therefore it is mandatory to reference the gate drive signal and measure VDS(on) and VSENSE with respect to the Kelvin pin.

Figure 15 illustrates the correct SENSEFET configuration.

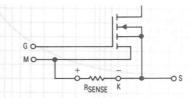


Figure 15. SENSEFET Configuration

SENSEFET APPLICATIONS CONSIDERATIONS

- Double Pulse Suppression: In PWM circuits it is critically important to include double pulse suppression in the control circuit topology. If the current limit loop is allowed to oscillate at its natural frequency, failure of the SENSEFET is likely due to over-dissipation. By syncing the current limit loop to the clock with a latch, double pulse suppression architectures solve this problem, and provide effective protection from overload stress.
- Noise Suppression: Noise pickup in the current sensing circuitry of SENSEFET systems can be a first order design issue. Layout, therefore is critical. In addition, some spike limiting capacitance across RSENSE is often desirable, provided that it is placed right at the current sensing circuitry's input terminals. To help with the layout problem, a Kelvin source connection is provided. The Kelvin connection gives SENSEFETs separate power and signal source pins. This feature can be used advantageously with circuits such as the MC34129 current mode controller and MC33034 brushless dc motor drive, which also have dual grounds.
- Ground Loop Errors: Lossless current sensing is a technique that looks for 100 mV signals in a loop that may carry tens or even hundreds of amps. The potential for ground loop error in this kind of situation is a first order design consideration. In particular, current flowing from the SENSEFET's source into a non-zero ground impedance can easily create voltage drops which are significant with respect to SENSEFET signal levels. Here again, the Kelvin connection is a useful tool. Tying the current limit circuitry's voltage reference to the Kelvin terminal as shown in Figure 16 eliminates errors that can be developed by high currents flowing in a power ground.

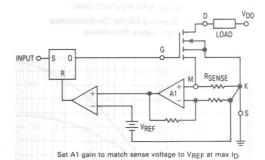


Figure 16. Typical Current Sensing with a SENSEFET

- Temperature Stability: With very low values of RSENSE, temperature tracking depends primarily upon the matching of monolithic devices and is generally within a few percent for a 100°C change in temperature. As RSENSE is increased, however, temperature coefficient becomes less dependent upon matching and more a function of the power section's on-voltage. In the limit where RSENSE is very large, sense voltage approximates VDS(on) and tracks its temperature coefficient. It is not unusual to see VSENSE change less than 5% for a 100°C change in temperature provided that RSENSE is less than 10% of rDM(on). On the other hand, changes of 50% are not unusual when RSENSE exceeds rDM(on).
- There is a parasitic reverse diode on the current mirror MOSFET as well as the power MOSFET. Diode reverse recovery currents will cause a sense voltage spike that may have to be filtered from the sense circuitry.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

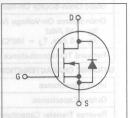
This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTP10N15

TMOS POWER FET 10 AMPERES rDS(on) = 0.3 OHM 150 VOLTS



MAXIMUM RATINGS

Rati	ting	Inotisi	Symbol	Value	Unit
Drain-Source Voltage		- 1	V _{DSS}	2.0 = (150) = (0	Vdc
Drain-Gate Voltage (R _{GS} = 1 MΩ)		(Holb)	VDGR	150	Vdc
Gate-Source Voltage — C	Continuous Non-repetitive (t	p ≤ 50 <i>μ</i> s)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current	(qyT) 8	Ogs	(V 0) =	gaV .gl berefi = g	Adc
Continuous Pulsed		bgO	IDM	10 28	La Court de
Total Power Dissipation (Derate above 25°C	@ T _C = 25°C	asy	PD	75 0.6	Watts W/°C
Operating and Storage T	emperature Ran	ge no	TJ, Tstg	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance				°C/W
Junction to Case		$R_{\theta JC}$	1.67	
Junction to Ambient (qvT) 3	TO-220	$R_{\theta JA}$	62.5	of did no w
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C



CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Cha	racteris	tic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)		MTF	P10N15	V _{(BR)DSS}	150	$G \in \mathcal{M}$	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ = 125°C)		IDSS	rid D meons	10 100	μAdo		
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		IGSSF	201	100	nAdo		
Gate-Body Leakage Current, Reve	rse (V _G	SR = 20 Vdc, V _{DS} = 0)	IGSSR	-	100	nAdd
ON CHARACTERISTICS*	183	THE STATE	rokage, ne ried reduit	tori as switch	e enotitalita	na pii falla.	
Gate Threshold Voltage (V _{DS} = \ T _J = 100°C	/GS, ID	= 1 mA)	van Tirace	V _{GS(th)}	1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	(VGS	= 10 Vdc, I _D = 5 Adc)		rDS(on)	_	0.3	Ohm
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 10 \text{ Adc}$) ($I_D = 5 \text{ Adc}$, $T_J = 100^{\circ}\text{C}$)		V _{DS(on)}	- VDS(on)- ire r Dis ci patio	3 2.5	Vdc		
Forward Transconductance (V _{DS}	= 15 V,	I _D = 5 A)	VIIDUBNI A	9FS	2.5) GD 112 17 E	mhos
YNAMIC CHARACTERISTICS							
Input Capacitance		$(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz})$		Ciss	_	800	pF
Output Capacitance				Coss	_	500	
Reverse Transfer Capacitance		See Figure 11		C _{rss}	_	100	
WITCHING CHARACTERISTICS* (T	J = 10	O°C)					
Turn-On Delay Time	tint		Symbol	[†] d(on)	_ 8	50	ns
Rise Time	olik V	$V_{DD} = 25 \text{ V, } I_{D} = 0.5 \text{ F}$	Rated ID	t _r	_	180	77 117
Turn-Off Delay Time	Villa	R _{gen} = 50 ohms See Figures 9, 13 and	d 14	td(off)	_	200	1 to /
Fall Time	- 904	00.4		tf	- Augustina	100	
Total Gate Charge	Vek	(VDS = 0.8 Rated VD	199, 180 V	Qg	15 (Typ)	м 30	nC
Gate-Source Charge	obio.	ID = Rated ID, VGS =		Qgs	8 (Typ)	_	11000
Gate-Drain Charge		See Figure 12	O.	Q_{gd}	7 (Typ)	_	Silnereite
OURCE DRAIN DIODE CHARACTE	RISTICS	76	MU		7000		
Forward On-Voltage	WCC.	(Is = Rated In	0.1	V _{SD}	1.2 (Typ)	2.5	Vdc
Forward Turn-On Time	3	VGS = 0)	TJ. Tstg	t _{on}	Limited	by stray ind	uctance
Reverse Recovery Time		1		t _{rr}	325 (Typ)	BIASTS AAV	ns
NTERNAL PACKAGE INDUCTANCE	*CAW					301151	LaP Er
Internal Drain Inductance (Measured from the contact scr (Measured from the drain lead			die)	L _d	3.5 (Typ) 4.5 (Typ)	11 <u>5</u> (0.00)	nH
Internal Source Inductance (Measured from the source lead	1 0 25" f	rom package to source	hand nad)	L _S	7.5 (Typ)	526 T	re myl

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

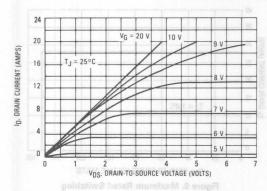


Figure 1. On-Region Characteristics

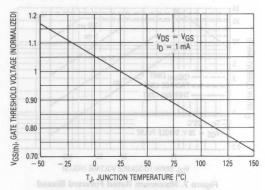


Figure 2. Gate-Threshold Voltage Variation With Temperature

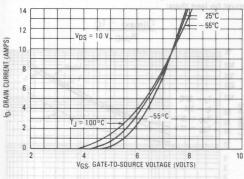


Figure 3. Transfer Characteristics

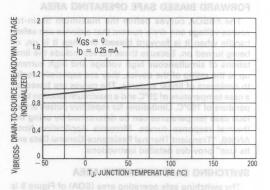


Figure 4. Breakdown Voltage Variation
With Temperature

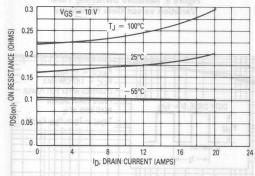


Figure 5. On-Resistance versus Drain Current

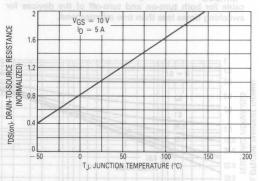


Figure 6. On-Resistance Variation
With Temperature

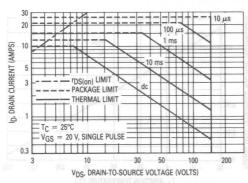


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

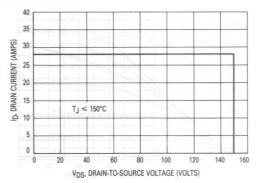


Figure 8. Maximum Rated Switching
Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

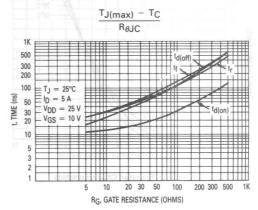


Figure 9. Resistive Switching Time Variation versus Gate Resistance

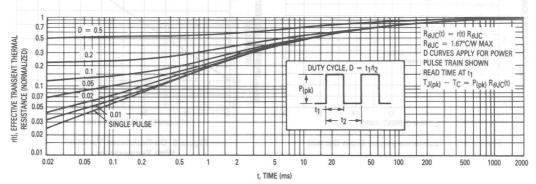
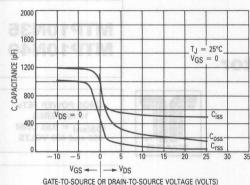


Figure 10. Thermal Response



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

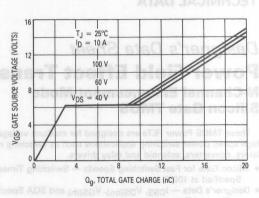


Figure 12. Gate Charge versus Gate-to-Source Voltage

Figure 11. Capacitance Variation

RESISTIVE SWITCHING

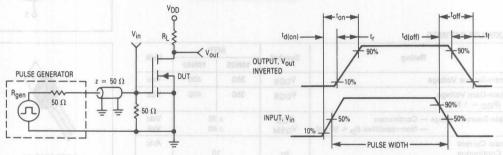
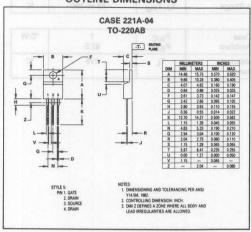


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

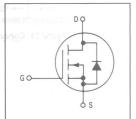
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data I_{DSS}, V_{DS(on)}, V_{GS(th)} and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FETS 10 AMPERES rDS(on) = 0.55 OHM 350 and 400 VOLTS



MAXIMUM RATINGS

100-100	Symbol	M		
Rating		10N35	10N40	Unit
Drain-Source Voltage	V _{DSS}	350	400	Vdc
Drain-Gate Voltage (R _{GS} = 1 MΩ)	V _{DGR}	350	400	Vdc
Gate-Source Voltage — Continuous — Non-repetitive (t _p ≤ 50 μs)	V _{GS} V _{GSM}		20 40	Vdc Vpk
Drain Current Continuous Pulsed Continuous Pulsed Continuous	I _D		0	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		25 1	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	- 65 1	to 150	°C

THERMAL CHARACTERISTICS

THE STATE OF EACH OF E			
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C



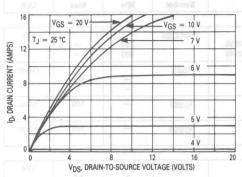
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

	cteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS		vint - acv	100	- 20 V = 2a	/ 0
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	MTP10N35 MTP10N40	V(BR)DSS	350 400	7 - 20	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS =), T _J = 125°C)	IDSS		0.2	mAdo
Gate-Body Leakage Current, Forwar (VGSF = 20 Vdc, VDS = 0)	d Santa	IGSSF	-	100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	08.0 14	IGSSR		100	nAdc
ON CHARACTERISTICS*	0 85 08 00 00	61	8 17		interest to \$1.0
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C		VGS(th)	2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, I _D = 5 Adc)		rDS(on)	-	0.55	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 10 Adc) (I _D = 5 Adc, T _J = 100°C)		V _{DS} (on)	#\\\ <u>-</u>	6 4.75	Vdc
Forward Transconductance (V _{DS} = 10 V, I _D = 5 A)		9FS	4		mhos
DYNAMIC CHARACTERISTICS	18 77				8
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0,	Ciss		1600	pF
Output Capacitance	f = 1 MHz)	Coss	T	350	0
Reverse Transfer Capacitance	See Figure 11	C _{rss}	1 - W	150	
WITCHING CHARACTERISTICS* (TJ	= 100°C)				
Turn-On Delay Time	La	td(on)	-	60	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r 30A	TO-SOLLECE VOL	150	1
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	nation Phase	200	
Fall Time		tf	-	120	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Q_g	40 (Typ)	60	nC
Gate-Source Charge	In = Rated In, VGS = 10 V)	Qgs	20 (Typ)		
Gate-Drain Charge	See Figure 12	Qgd	20 (Typ)	—0°e01	= 17
SOURCE DRAIN DIODE CHARACTERIS	STICS*				
Forward On-Voltage	(Is = Rated Ip	VSD	1.1 (Typ)	2	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray inc	luctance
Reverse Recovery Time	1 8 8	t _{rr}	600 (Typ)	1-	ns
NTERNAL PACKAGE INDUCTANCE	A = 2				
Internal Drain Inductance (Measured from the contact screw (Measured from the drain lead 0.25		L _d	3.5 (Typ) 4.5 (Typ)		nH
Internal Source Inductance	5" from package to source bond pad.)	L _S	7.5 (Typ)		100

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

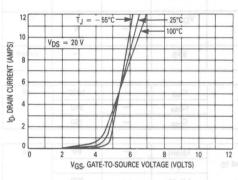
TYPICAL ELECTRICAL CHARACTERISTICS



(3) 1.2 VDS = VGS | 1.1 VDS = VGS | 1.1 VDS = 1 mA | 1.1

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation
With Temperature



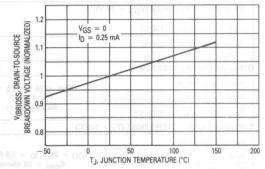
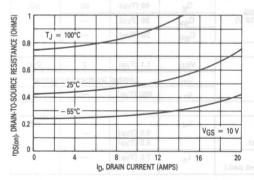


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation
With Temperature



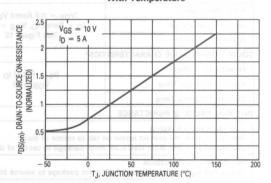


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

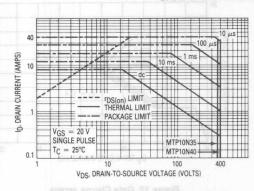


Figure 7. Maximum Rated Forward Biased Safe Operating Area

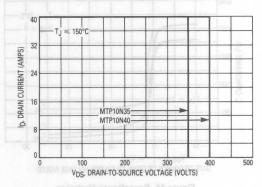


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

$$T_{J(max)} - T_{C}$$
 $R_{\theta JC}$

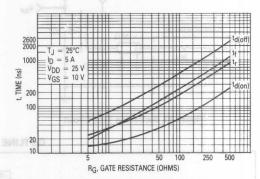


Figure 9. Resistive Switching Time Variation versus Gate Resistance

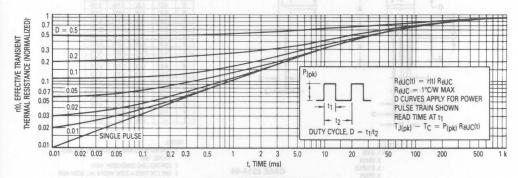
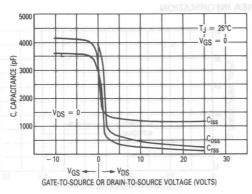


Figure 10. Thermal Response



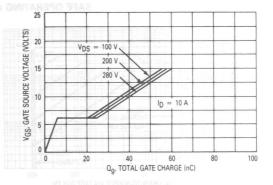
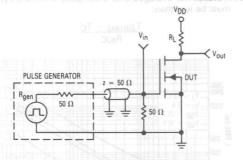


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING



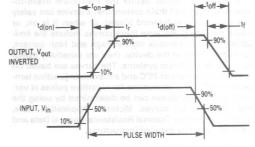
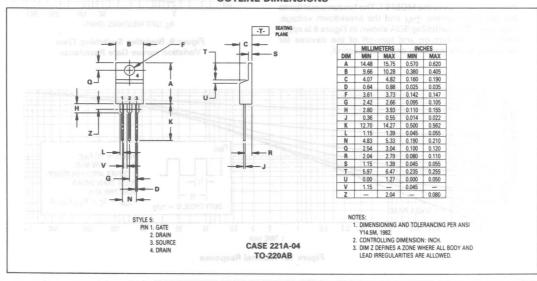


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MTP12N08L

TMOS POWER FETs LOGIC LEVEL 12 AMPERES

rDS(on) = 0.18 OHM 80 and 100 VOLTS

Designer's Data Sheet

■ SEMICONDUCTOR TECHNICAL DATA

Power Field Effect Transistor N-Channel Enhancement-Mode

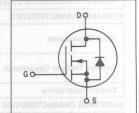
Silicon Gate TMOS

These Logic Level TMOS Power FETs are designed for high labA 0 = glabV 0 = ggV est speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — VGS(th) = 2 Volts max
- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



Symbol Min



MAXIMUM RATINGS

MOTOROLA

Day Rating	Symbol	MTP12N08L	MTP12N10L	Unit
Drain-Source Voltage	VDSS	80	100 aa	Vdc
Drain-Gate Voltage (R _{GS} = 1 MΩ)	VDGR	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 2 and Voss		Vdc Vpk
Drain Current — Continuous — Pulsed (9/4) 5.11 bp.9	I _D	0.1 109109 1 1 16	2	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD		5 .6	Watts W/°C
Operating and Storage Temperature Range	TJ, Tstg	-65	to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	R _O JC R _O JA	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL sib	275	℃



TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic

Ollaractoristic		Cyllibor	Statement of the	Ivida	Oine
FF CHARACTERISTICS					
Drain-Source Breakdown Voltage (VGS = 0, I_D = 250 μ A)	MTP12N08L MTP12N10L	V(BR)DSS	80 100	_	Vdc
Zero Gate Voltage Drain Current (Vps = Rated Vpss, Vgs = 0) (Vps = Rated Vpss, Vgs = 0, Tj = 125°C)		IDSS	Ξ	1 50	μAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

CI	naracteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued	1)		-		
Gate-Body Leakage Current, Forward (VGSF = 15 Vdc, VDS = 0)		IGSSF	12 etel	100	nAdo
Gate Body Leakage Current, Reverse (VGSR = 15 Vdc, VDS = 0)		IGSSR	44 61	100	nAdo
ON CHARACTERISTICS		15.05	D 0 100 010 0	E 10.1	
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) (T _{.1} = 100°C)		V _{GS(th)}	1 0.75	2 1.5	Vdc
Static Drain-Source On-Resistance (VGS = 5 Vdc, ID = 6 Adc) Highly roll ber		rDS(on)	ER nework 20	0.18	Ohm
Drain-Source On-Voltage (V _{GS} = 5 V) (I _D = 12 Adc) (I _D = 6 Adc, T _J = 100°C)		V _{DS(on)}	oplications : relay <u>d</u> river it to i nt erfec	2.4 1.6	Vdc
Forward Transconductance (VDS	; = 10 V, I _D = 6 A)	g _{FS}	188 5	889 NC	mhos
DYNAMIC CHARACTERISTICS	Assert Chine	direct spe	pdo Bureoum	100 100 7	
1.00	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	Vesting and	s Vi ja (on)-	800	pF
Input Capacitance	V _{GS} = 15 V, V _{DS} = 0, f = 1 MHz	C _{iss}	enu	2600	
Bayerea Transfer Consider	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	W self tot b	Characterize	350	
Reverse Transfer Capacitance	$V_{GS} = 15 \text{ V}, V_{DS} = 0, f = 1 \text{ MHz}$	C _{rss}	_	1600	pF
Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	Coss	_	100	pF
SWITCHING CHARACTERISTICS (T	J = 100°C)				
Turn-On Delay Time		[†] d(on)	_	50	ns
Rise Time	$(V_{DD} = 25 \text{ V}, I_{D} = 6 \text{ A},$	t _r	_ Bt	150	
Turn-Off Delay Time	V _{GS} = 5 V, R _{gen} = 50 ohms)	td(off)	_	130	
Fall Time	APA ABI GB MGCA	tf	<u>(C</u> ilyl I	150	
Total Gate Charge	$(V_{DS} = 0.8 \text{ Rated } V_{DSS},$	Qg	15 (typ)	25	nC
Gate-Source Charge	I _D = 12 A, V _{GS} = 5 Vdc)	Qgs	3.7 (typ)	_	
Gate-Drain Charge	See Figures 11 and 12.	Qgd	11.3 (typ)	t eat	
SOURCE DRAIN DIODE CHARACT	ERISTICS		To = 20°C	g) note and	183
Forward On-Voltage	(Is = Rated ID, VGS = 0)	V _{SD}	1 (typ)	1.25	Vdc
Forward Turn-On Time	or total an or girt u.T	ton	Limited	by stray indu	ctance
Reverse Recovery Time		t _{rr}	325 (typ)	MATELIAN.	ns
NTERNAL PACKAGE INDUCTANC	E WAD!				- 14
Internal Drain Inductance (Measured from the contact scre (Measured from the drain lead 0	w on tab to center of die) .25" from package to center of die)	Ld	3.5 (typ) 4.5 (typ)	Th owner	nH
Internal Source Inductance	0.25" from package to source bond pad.)	Ls	7.5 (typ)	3CF7 : : : -	

^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

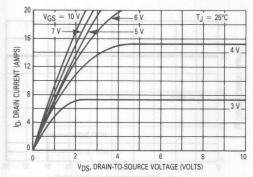


Figure 1. On-Region Characteristics

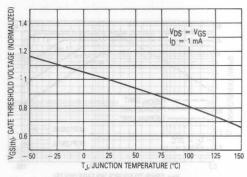


Figure 2. Gate-Threshold Voltage Variation
With Temperature

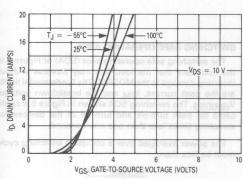


Figure 3. Transfer Characteristics

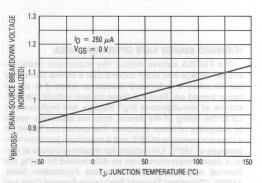


Figure 4. Breakdown Voltage Variation With Temperature

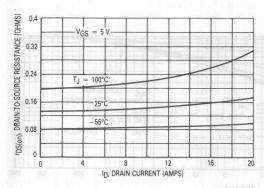


Figure 5. On-Resistance Variation With Drain Current

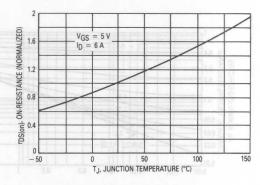


Figure 6. On-Resistance Variation
With Temperature

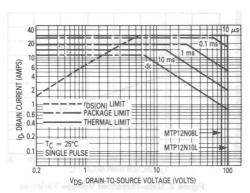


Figure 7. Maximum Rated Forward Biased Safe Operating Area

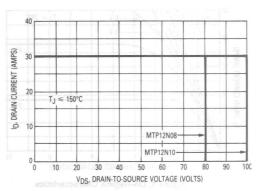


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

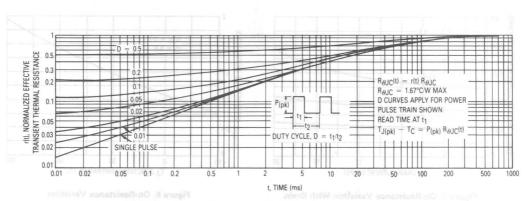


Figure 9. Thermal Response

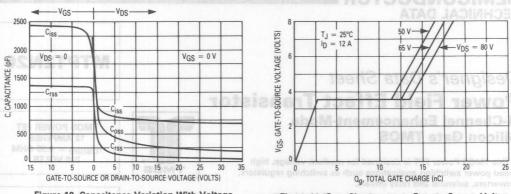
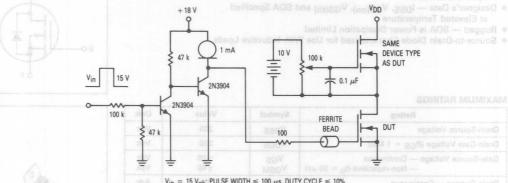


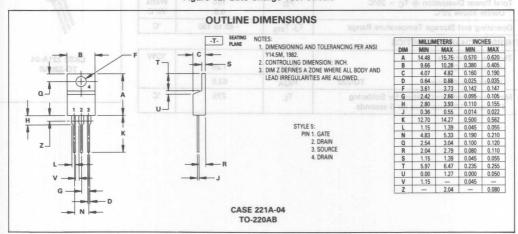
Figure 10. Capacitance Variation With Voltage

Figure 11. Gate Charge versus Gate-to-Source Voltage



 $V_{in} = 15 V_{pk}$; PULSE WIDTH $\leq 100 \mu s$, DUTY CYCLE $\leq 10\%$

Figure 12. Gate Charge Test Circuit



Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

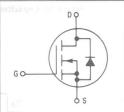
This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TMOS POWER FET
12 AMPERES
rDS(on) = 0.35 OHM
200 VOLTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage TUG (A38)	VDSS	200	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	200	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	IDM	40 40	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	100 0.8	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		$R_{\theta JC}$	1.25	°C/W
Canalian to Case		116JC	1.20	
Junction to Ambient	TO-220	$R_{\theta JA}$	62.5	1
Maximum Lead Temperature f Purposes, 1/8" from case for		TL	275	°C



CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Figure 6. On-Resistence Variation

Cha	racteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS			20 V - 6 - 10	= 20V	
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	tr og	V(BR)DSS	200	7020	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0,	T _J = 125°C)	IDSS		10 100	μAdd
Gate-Body Leakage Current, Forw	ard (V _{GSF} = 20 Vdc, V _{DS} = 0)	IGSSF	-	100	nAdd
Gate-Body Leakage Current, Reve	rse (V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR	+	100	nAdd
ON CHARACTERISTICS*	\$D 150				
Gate Threshold Voltage (VDS = VGS, ID = 1 mA)		VGS(th)	2 1.5	4.5	Vdc
T _J = 100°C Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 6 Adc)		rDS(on)	KON SOUTHON OT	0.35	Ohm
The state of the s		V _{DS(on)}	-Ringion Chi	5 4.2	Vdc
Forward Transconductance (VDS	= 15 V, I _D = 6 A)	9FS	4.5	_	mho
DYNAMIC CHARACTERISTICS		VIV			-
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0,	Ciss	198 (1-	1000	pF
Output Capacitance	f = 1 MHz) See Figure 11	Coss	++1	400	
Reverse Transfer Capacitance		C _{rss}	198 4	100	
SWITCHING CHARACTERISTICS* (1	$J = 100^{\circ}C$	1 134			
Turn-On Delay Time	3 10001	td(on)	+	50	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r	-	250	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	1 + 1	100	
Fall Time	30 8	tf	10/-	120	
Total Gate Charge	(VDS = 0.8 Rated VDSS,	Qg	24 (Typ)	50	nC
Gate-Source Charge	I_D = Rated I_D , V_{GS} = 10 V)	Qgs	13 (Typ)	2	
Gate-Drain Charge	See Figure 12	Q _{gd}	11 (Typ)	VGS GATE-I	
SOURCE DRAIN DIODE CHARACTE	RISTICS*	ectoristics	ransfer Charr	Figure 3. To	
Forward On-Voltage	(IS = Rated ID	V _{SD}	1.5 (Typ)	3	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	uctance
Reverse Recovery Time	25	t _{rr}	300 (Typ)		ns
NTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		Ld	3.5 (Typ) 4.5 (Typ)	A 01 = 50 A	nH
Internal Source Inductance		L _s	7.5 (Typ)		

TYPICAL ELECTRICAL CHARACTERISTICS

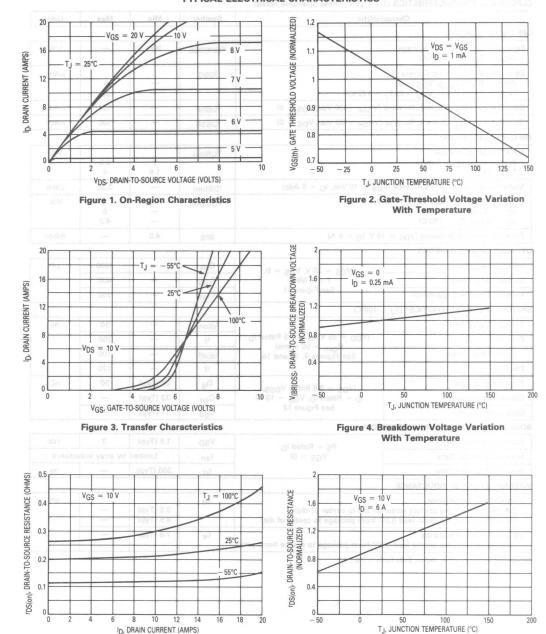
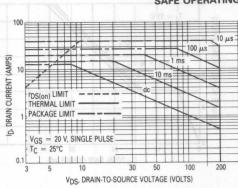


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature



Safe Operating Area

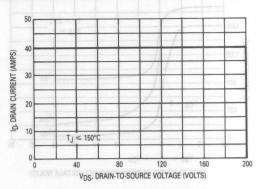


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

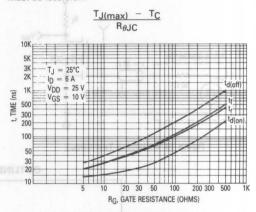
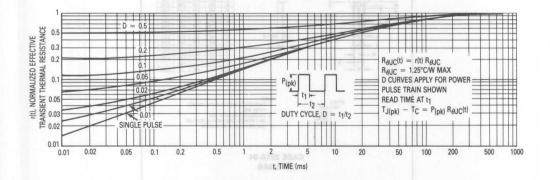
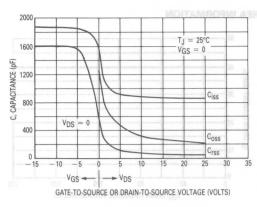


Figure 9. Resistive Switching Time Variation versus Gate Resistance



MOTOROLA TMOS POWER MOSFET DATA

Figure 10. Thermal Response



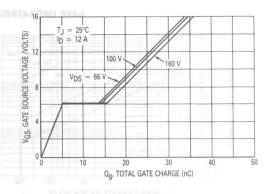
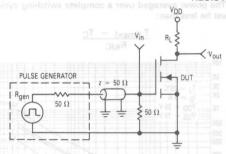


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING





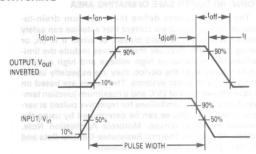
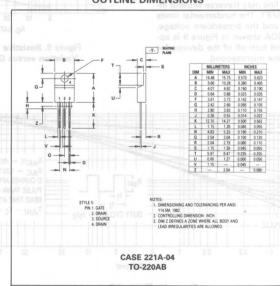


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA ■ SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

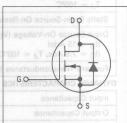
N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified GLABY OF A SOUTH S
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

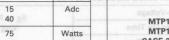
MTP15N05 MTP15N06

TMOS POWER FETs 15 AMPERES rDS(on) = 0.16 OHM 50 and 60 VOLTS



MAXIMUM RATINGS

200	(flo)b1	0 1 1	ns ar a M	TP Tesa	11.74
Rating	12	Symbol	15N05	15N06	Unit
Drain-Source Voltage	C _g	VDSS	50	60	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	Qgs	VDGR	= 850° G	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)		V _{GS} V _{GSM}		20 40	Vdc Vpk
Drain Current — Continuous — Pulsed		I _D		5	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	no)	PD		'5 .6	Watts W/°C
Operating and Storage Temperature Range		T _J , T _{stg}	- 65	to 150	°C



THERMAL CHARACTERISTICS

Thermal Resistance		(alb to	ackage to center	°C/W
Junction to Case		$R_{\theta JC}$	1.67	
Junction to Ambient	TO-220	R _θ JA	62.5	0.25° from
Maximum Lead Temperature f Purposes, 1/8" from case for		TL	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



MTP15N05 MTP15N06 CASE 221A-04 TO-220AB

Chara	acteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (VGS = 0, I _D = 0.25 mA)	MTP15N05 MTP15N06	V(BR)DSS	50 60	0 <u>+</u> 1 te	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, T	J = 125°C)	IDSS	d Eff	10 100	μAdc
Gate-Body Leakage Current, Forward	rd (V _{GSF} = 20 Vdc, V _{DS} = 0)	IGSSF	20h	100	nAdc
Gate-Body Leakage Current, Revers	e (V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR	_	100	nAdc
ON CHARACTERISTICS*	inge, mgn	ich as switchi	s are uesign	DE DESCRIPTION	201100
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C			nevi2 yele eq2 1.5 eq2 phidoin	4.5	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 7.5 Adc)			VDStonte	0.16	Ohm
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 15 \text{ Adc}$) ($I_D = 7.5 \text{ Adc}$, $T_J = 100^{\circ}\text{C}$)			ire ir Dis <u>ci</u> patio hara <u>ct</u> erice	2.9	Vdc
Forward Transconductance (VDS =	15 V, I _D = 7.5 A)	9FS	3.5	_	mhos
DYNAMIC CHARACTERISTICS		-			
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0,	C _{iss}	_	700	pF
Output Capacitance	f = 1 MHz)	Coss	_	400	
Reverse Transfer Capacitance	See Figure 11	C _{rss}	_	200	
SWITCHING CHARACTERISTICS* (TJ	= 100°C)				
Turn-On Delay Time		td(on)	_	50	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r	_	150	AXIMETERS
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	_	200	
Fall Time	Symbol 15Nos 15Nos	tf	_	100	
Total Gate Charge	(VDS = 0.8 Rated VDSS,	Qg	17 (Typ)	35	nC
Gate-Source Charge	ID = Rated ID, VGS = 10 V)	Qgs	8 (Typ)	- 857 - 4111	, en o-risid
Gate-Drain Charge See Figure 12		Q _{gd}	9 (Typ)	60 - - 0 0	Bate St.
OURCE DRAIN DIODE CHARACTERI	STICS* MEDV	(sr/ 05 > 0	n evilleger-n	OM	
Forward On-Voltage	(Is = Rated Ip	V _{SD}	1.8 (Typ)	2.5	Vdc
Forward Turn-On Time	$V_{GS} = 0$	ton	Limited	by stray ind	uctance

 t_{rr}

 L_{d}

Ls

320 (Typ)

3.5 (Typ) 4.5 (Typ)

7.5 (Typ)

ns

nH

(Measured from the source lead 0.25" from package to source bond pad.) *Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

(Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)

Reverse Recovery Time

Internal Source Inductance

INTERNAL PACKAGE INDUCTANCE
Internal Drain Inductance

3

TYPICAL ELECTRICAL CHARACTERISTICS

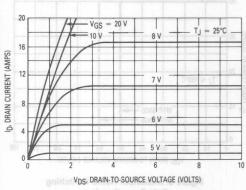


Figure 1. On-Region Characteristics

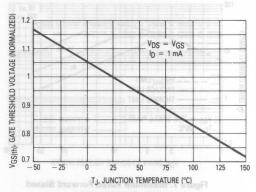


Figure 2. Gate-Threshold Voltage Variation With Temperature

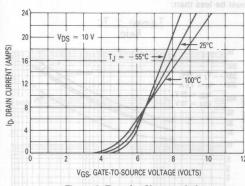


Figure 3. Transfer Characteristics

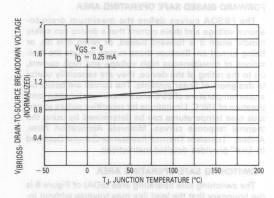


Figure 4. Breakdown Voltage Variation With Temperature

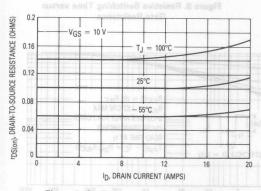


Figure 5. On-Resistance versus Drain Current

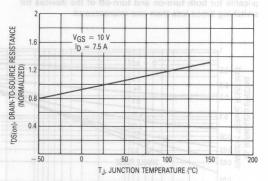


Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

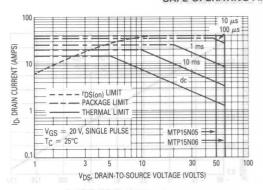


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

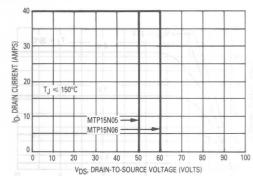


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V(\mbox{\footnotesize BR})_{\mbox{\footnotesize DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

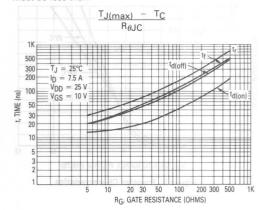


Figure 9. Resistive Switching Time versus

Gate Resistance

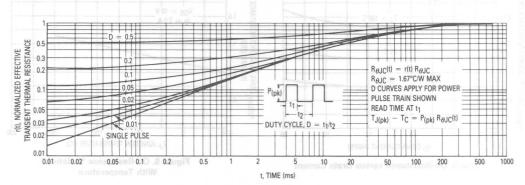
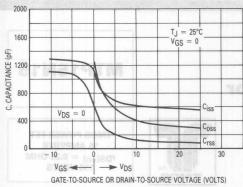


Figure 10. Thermal Response



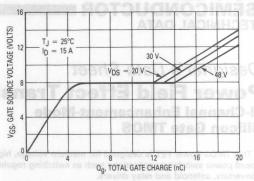


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-To-Source Voltage

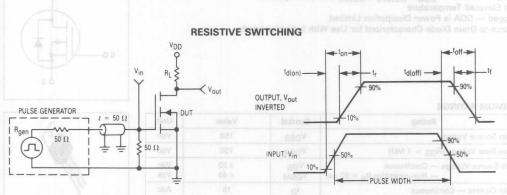
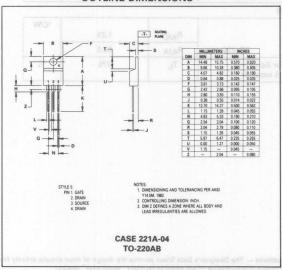


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



Designer's Data Sheet

Power Field Effect Transistor

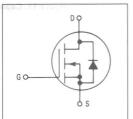
N-Channel Enhancement-Mode Silicon Gate TMOS

This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FET 15 AMPERES rDS(on) = 0.25 OHM 150 VOLTS



MAXIMUM RATINGS

3

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	150	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	VDGR	150	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \mu s$)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed W grantof W At an USA	I _D	15 48	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	100 0.8	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C



Thermal Resistance Junction to Case		$R_{\theta JC}$	1.25	°C/W
Junction to Ambient	TO-220	R _θ JA	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C



TO-220AB

ELECTRICAL	CHARACTERISTICS	(T _C	=	25°C unless otherwise noted)	PICA

Chara	cteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS				1/ 20V	Vos = znv
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	III BU	V(BR)DSS	150	7	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, T	J = 125°C)	IDSS	Y5 =	10 100	μAdd
Gate-Body Leakage Current, Forwar	d (VGSF = 20 Vdc, VDS = 0)	IGSSF		100	nAdd
Gate-Body Leakage Current, Revers	Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)			100	nAdd
ON CHARACTERISTICS*	80 4		V.9		1
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C	VGS(th)	2 1.5	4.5	Vdc	
Static Drain-Source On-Resistance	V _{GS} = 10 Vdc, I _D = 7.5 Adc)	rDS(on)	NEOUR CE VOLTA	0.25	Ohm
Drain-Source On-Voltage ($V_{GS} = 1$ ($I_D = 15 \text{ Adc}$) ($I_D = 7.5 \text{ Adc}$, $T_J = 100^{\circ}\text{C}$)	V _{DS(on)}	legio <u>n</u> Char	4.5 3.75	Vdc	
Forward Transconductance (VDS =	9FS	5.5	_	mho	
YNAMIC CHARACTERISTICS	143				
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss	_ 2632	1000	pF
Output Capacitance	f = 1 MHz)	Coss	1 -1	500	
Reverse Transfer Capacitance	See Figure 11	C _{rss}		100	
WITCHING CHARACTERISTICS* (TJ	= 100°C)				
Turn-On Delay Time	THE STATE OF THE S	td(on)		50	ns
Rise Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D	t _r		250	y
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 9, 13 and 14	td(off)	W-	100	
Fall Time	10 8	tf	11/-	120	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Qg	23 (Typ)	45	nC
Gate-Source Charge	ID = Rated ID, VGS = 10 V)	Qgs	11 (Typ)	A	-
Gate-Drain Charge	See Figure 12	Qgd	12 (Typ)	Vag. GATE-TO	
OURCE DRAIN DIODE CHARACTERI	STICS*				
Forward On-Voltage	(Is = Rated ID	V _{SD}	1.2 (Typ)	2.5	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray ind	ductance
Reverse Recovery Time		t _{rr}	300 (Typ)	-	ns
NTERNAL PACKAGE INDUCTANCE		TITI			
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L _d	3.5 (Typ) 4.5 (Typ)	V 01	Hn 204
Internal Source Inductance (Measured from the source lead	0.25" from package to source bond pad.	L _S	7.5 (Typ)	1	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS OF SOMESTOANANCE AND ANALYSIS

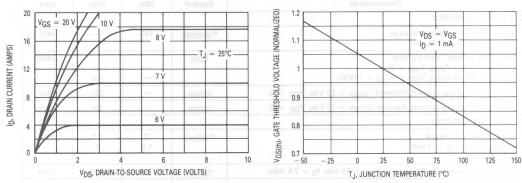


Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation With Temperature

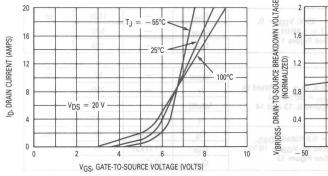


Figure 3. Transfer Characteristics

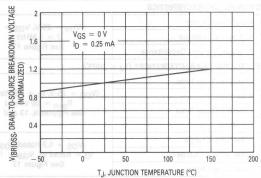


Figure 4. Breakdown Voltage Variation
With Temperature

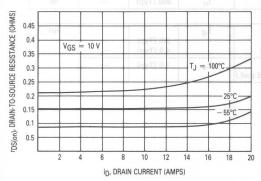


Figure 5. On-Resistance versus Drain Current

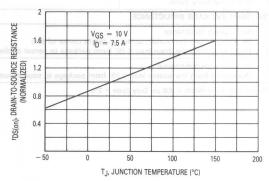


Figure 6. On-Resistance Variation With Temperature

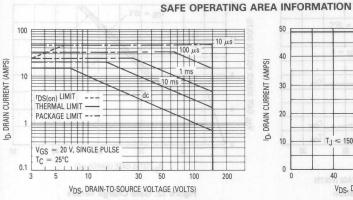


Figure 7. Maximum Rated Forward Biased Safe Operating Area

50 40 40 80 120 160 200 VDS, DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{\rm (BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

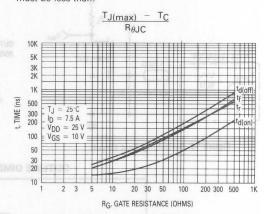


Figure 9. Resistive Switching Time Variation versus Gate Resistance

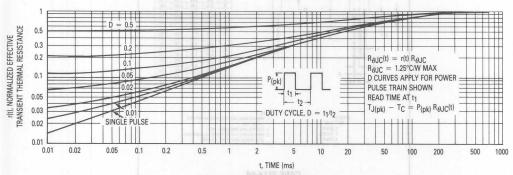


Figure 10. Thermal Response

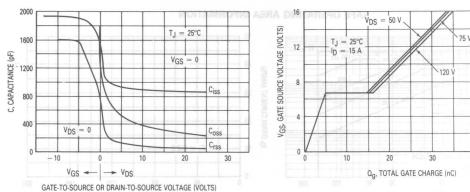


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-to-Source Voltage

40

RESISTIVE SWITCHING

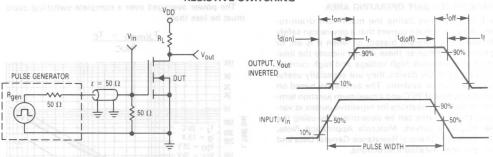
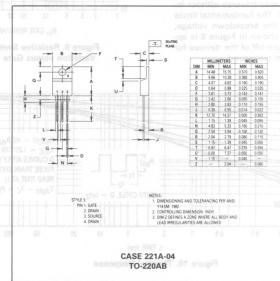


Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS OF TO LACE BOTTO



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Advance Information

Power Field Effect Transistor

P-Channel Enhancement-Mode Silicon Gate TMOS

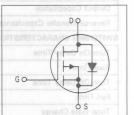
This TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS

TMOS POWER FET 20 AMPERES rDS(on) = 0.2 OHM 60 VOLTS



MAXIMUM RATINGS

Rating (gvT) 05	Symbol	Value	Unit
Drain-Source Voltage (gy/T) 01	VDSS	See Fi 00 12	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	V _{DGR}	60	Vdc
Gate-Source Voltage Continuous Non-repetitive (t _p ≤ 50 μs)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	20 72	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	125 0.8	Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stg}	-65 to 150	°C



THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	R_{θ} JC	1.25	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ARACTERISTICS				
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA)	V _{(BR)DSS}	60	_	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ = 125°C)	IDSS	=		μAdd
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	IGSSF	_	100	nAdd
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	_	100	nAdd

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

	Characteristic		Symbol	Min	Max	Unit	
ON CHARACTERISTICS*						1	
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C		s circle a const	V _{GS(th)}	2 1.5	4.5		Vdc
Static Drain-Source On-Resis	tance (VGS = 10) Vdc, I _D = 10 Adc)	rDS(on)	I I mad the	0.2	Ohm	
Drain-Source On-Voltage (V _{(ID} = 20 Adc) (ID = 10 Adc, T _J = 100°C	V _{DS(on)}	ncemel IOS_	4.2	Vdc			
Forward Transconductance (V _{DS} = 15 V, I _D	= 10 A)	9FS	5	i.T.C.	mhos	
OYNAMIC CHARACTERISTICS	47 年 日	anverters,	g regulators, co	nidatiwe za d	alla PON Ja	nges gode	
Input Capacitance	P.F.154	V _{DS} = 25 V, V _{GS} = 0,	Ciss	_	1400	pF	
Output Capacitance	,	f = 1 MHz	Coss	Hade Builds	700	151	
Reverse Transfer Capacitano	e	See Figure 11	C _{rss}	W.JawaselV	300	3	
WITCHING CHARACTERISTIC	S* (T _J = 100°C)		1931112	971	dalacimo	1. lo . le 3	
Turn-On Delay Time		au item de	td(on)	horaclessu :	60	ns	
Rise Time	(V _[$D_D = 25 \text{ V, } I_D = 10 \text{ Amp,}$	t _r	-	350	11.60	
Turn-Off Delay Time	S	R _{gen} = 50 ohms) ee Figures 9, 13 and 14	td(off)	_	150		
Fall Time		or rigardo o, ro aria ri	tf		160	1	
Total Gate Charge	0	// 0.0 Pered //		30 (Typ)	60	nC	
Gate-Source Charge		/DS = 0.8 Rated V _{DSS} , = 20 Amp, V _{GS} = 10 V)	Ω_{g}	20 (Typ)	gnitali		
Gate-Drain Charge	Vde	See Figure 12	Qqd	10 (Typ)	<u> </u>	100112	
SOURCE DRAIN DIODE CHARA	ACTERISTICS*	00	Pagy		1.0	u h h	
Forward On-Voltage			V _{SD}	4 (Typ)	4.2	Vdc	
Forward Turn-On Time	sav	$(I_S = 20 \text{ Amp}, V_{GS} = 0)$	ton	100 (Typ)	_	ns	
Reverse Recovery Time	8qV	VGS - 07	Masy trr	120 (Typ)	11, <u>—</u> 180 µ	ns	
NTERNAL PACKAGE INDUCTA	NCE (TO-220)	08	al a	81	io infinaçõe	in nakati	
Internal Drain Inductance (Measured from the conta (Measured from the drain			og Ld	3.5 (Typ) 4.5 (Typ)	Mra <u>r</u> icas	nH	
Internal Source Inductance (Measured from the source	e lead 0.25" from	package to center of pad)	gall La se	7.5 (Typ)	187 1 <u>58</u> 1 2 21977 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Pulse Test: Pulse Width ≤ 300 μs.	Duty Cycle ≤ 2%.	1.25	Rate	easO nt noite	nut - use	graph states	

3

TYPICAL ELECTRICAL CHARACTERISTICS

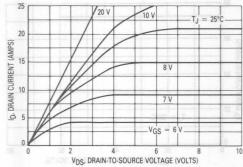


Figure 1. On-Region Characteristics

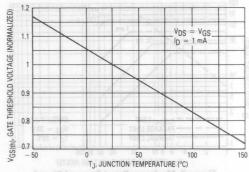


Figure 2. Gate-Threshold Variation
With Temperature

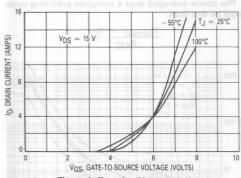


Figure 3. Transfer Characteristics

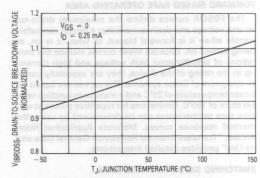


Figure 4. Breakdown Voltage Variation
With Temperature

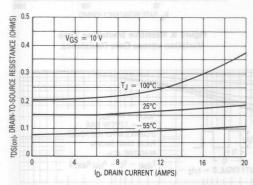


Figure 5. On-Resistance versus Drain Current

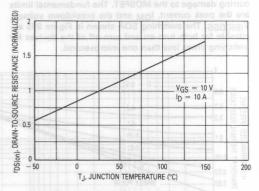


Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

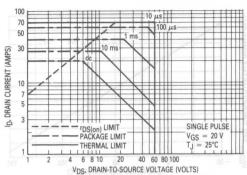


Figure 7. Maximum Rated Forward Biased Safe Operating Area

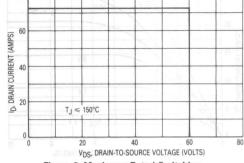


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

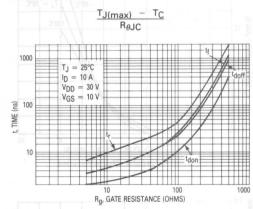


Figure 9. Resistive Switching Time Variation versus Gate Resistance

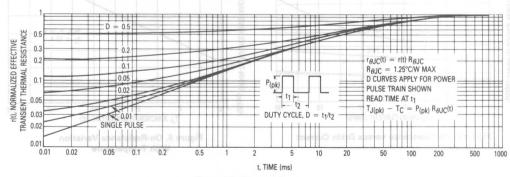


Figure 10. Thermal Response

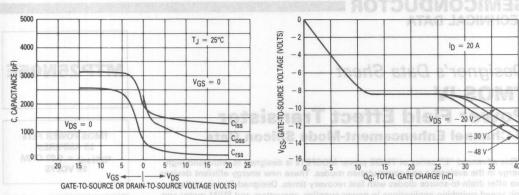


Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-To-Source Voltage

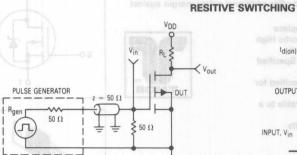


Figure 13. Switching Test Circuit

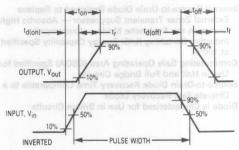


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS | SALTING | SALT

CASE 221A-04 TO-220AB

Designer's Data Sheet

TMOS IV

Power Field Effect Transistor

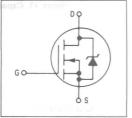
N-Channel Enhancement-Mode Silicon Gate

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits



TMOS POWER FETS
25 AMPERES
rDS(on) = 0.07 OHM
50 VOLTS





h.P. assumini

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	50	Vdo
Drain-Gate Voltage (R _{GS} = 1 M Ω)	VDGR	50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$)	V _G S V _G SM	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	25 80	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	100 0.8	Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	76		$R_{ heta JC}$ $R_{ heta JA}$	1.25 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	DISCONDING STORES AND TOLERAND AND TOLERAND SAND NO.	2120 1 001 2120 1 001	TL	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T _C = 25°C unless otherwise noted)	
---	--

	cteristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS					
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)		V(BR)DSS	50	NE VOI	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ	- 125°C)	IDSS	A8 -	10 100	μΑ
Gate-Body Leakage Current, Forward		loope		100	nAdc
		IGSSF	44	100	nAdc
Gate-Body Leakage Current, Reverse	(vGSR = 20 vdc, vDS = 0)	IGSSR	T	100	HAGE
IN CHARACTERISTICS*	1 2	V _{GS(th)}			7.11
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μA, T _J = 100°C)			1.5	3.5	Vdc
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 16 Adc)		rDS(on)	-	0.07	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 25 Adc) (I _D = 12.5 Adc, T _J = 100°C)			10 3014 E VOL	2	Vdc
Forward Transconductance (VDS =		9 _{FS}	9 9	-nO tř stut	mhos
PRAIN-TO-SOURCE AVALANCHE CHA	RACTERISTICS				
Unclamped Drain-to-Source Avalanche Energy See Figures 14 and 15 ($ID = 80 \text{ A}, V_{DD} = 25 \text{ V}, T_{C} = 25^{\circ}\text{C}, \text{ Single Pulse, Non-repetitive}$) ($ID = 25 \text{ A}, V_{DD} = 25 \text{ V}, T_{C} = 25^{\circ}\text{C}, \text{ P.W.} \le 200 \ \mu\text{s}, \text{ Duty Cycle} \le 1\%$) ($ID = 10 \text{ A}, V_{DD} = 25 \text{ V}, T_{C} = 100^{\circ}\text{C}, \text{ P.W.} \le 200 \ \mu\text{s}, \text{ Duty Cycle} \le 1\%$)			- # = 1	90 200 90	mJ
DYNAMIC CHARACTERISTICS	0 = 20V	1/1		Wat	
Input Capacitance	da = 0	C _{iss}		1600	pF
Output Capacitance	$V_{DS} = 25 \text{ V, } V_{GS} = 0,$ f = 1 MHz)	Coss	- 1	800	
Reverse Transfer Capacitance	See Figure 16	C _{rss}		200	
WITCHING CHARACTERISTICS* (TJ	= 100°C)				
Turn-On Delay Time	1 2 2	t _{d(on)}		25	ns
Rise Time	(V _{DD} = 25 V, I _D = 16 A	tr		35	
Turn-Off Delay Time	R _{gen} = 15 ohms) See Figure 9	td(off)	117	45	
Fall Time	Social Sales	tf	7-33	35	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Ωg	26 (Typ)	30	nC
Gate-Source Charge	$I_D = Rated I_D, V_{GS} = 10 V$	Qgs	14 (Typ)	DING SOL	
Gate-Drain Charge	See Figures 17 and 18	Qgd	12 (Typ)	gure_3. In	
SOURCE DRAIN DIODE CHARACTERIS	STICS*				
Forward On-Voltage		V _{SD}	1.3 (Typ)	1.5	Vdc
Forward Turn-On Time	(I _S = 25 A V _{GS} = 0)	ton		by stray inc	ductance
Reverse Recovery Time		t _{rr}	160 (Typ)		ns
NTERNAL PACKAGE INDUCTANCE	11 - 201 31 5				204
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)			3.5 (Typ) 4.5 (Typ)		nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)		L _S	7.5 (Typ)	1-1	
	1.25 from package to source bond pad.)	F			

TYPICAL ELECTRICAL CHARACTERISTICS - 371 SOFTERETOARAND LEURY DE LE

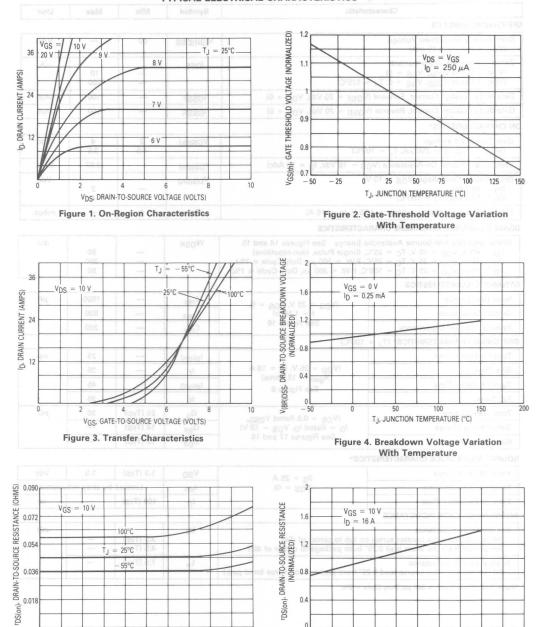


Figure 5. On-Resistance versus Drain Current

ID, DRAIN CURRENT (AMPS)

24

12

0

Figure 6. On-Resistance Variation With Temperature

TJ, JUNCTION TEMPERATURE (°C)

100

50

150

200

0.4

0 _

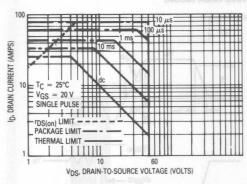


Figure 7. Maximum Rated Forward Biased Safe Operating Area



The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

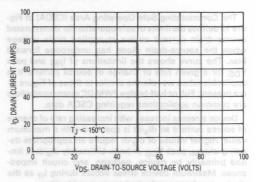


Figure 8. Maximum Rated Switching Safe Operating Area

The power averaged over a complete switching cycle must be less than:

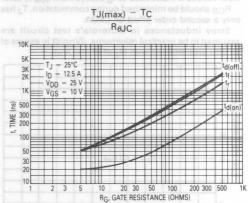


Figure 9. Resistive Switching Time Variation versus Gate Resistance

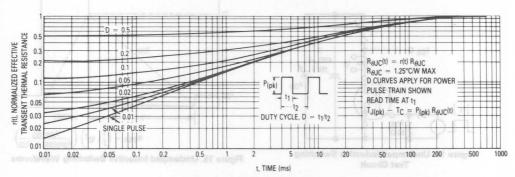


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of IFM and peak VDS for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so $dl_{\rm S}/dt$ is specified with a maximum value. Higher values of $dl_{\rm S}/dt$ require an appropriate derating of $l_{\rm FM}$, peak $V_{\rm DS}$ or both. Ultimately $dl_{\rm S}/dt$ is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during $t_{\rm rr}$ as the diode goes from conduction to reverse blocking.

V_{DS(pk)} is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of V_{(BR)DSS} to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

RGS should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dl_{S}/dt of 400 A/ μ s.

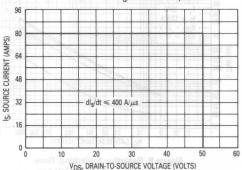


Figure 12. Commutating Safe Operating Area (CSOA)

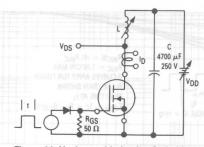


Figure 14. Unclamped Inductive Switching Test Circuit

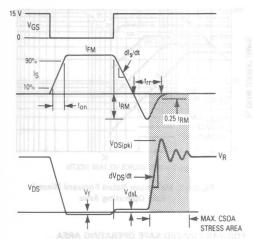


Figure 11. Commutating Waveforms

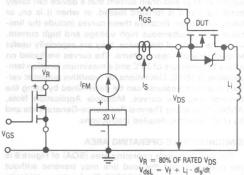


Figure 13. Commutating Safe Operating Area Test Circuit

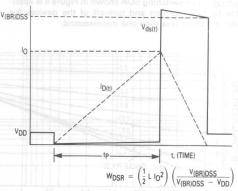
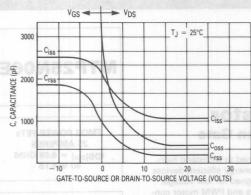


Figure 15. Unclamped Inductive Switching Waveforms



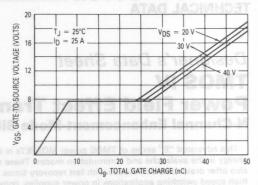


Figure 16. Capacitance Variation

Figure 17. Gate Charge versus Gate-to-Source Voltage

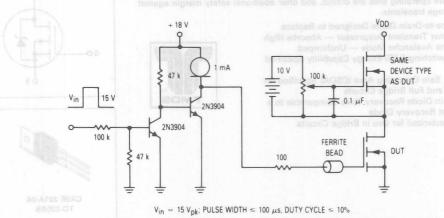
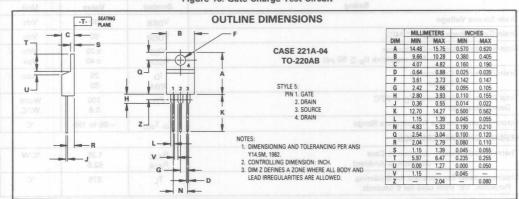


Figure 18. Gate Charge Test Circuit



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

TMOS IV

Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate

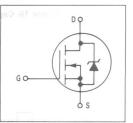
This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- · Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits





TMOS POWER FETs 25 AMPERES rDS(on) = 0.08 OHM 60 VOLTS





CASE 221A-04 TO-220AB

MAXIMUM RATINGS (T.I = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage &MOIZMANNO 3MLTTUO	V _{DSS}	60	Vdc
Drain-Gate Voltage (R _{GS} = 1 MΩ)	VDGR	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive (t _p ≤ 50 μs)	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	I _D	25 80	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	100 0.8	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C

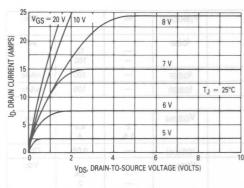
Thermal Resistance — Junction to Case — Junction to Ambient	R _θ JC R _θ JA	1.25 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T _C = 25°C unless otherwise

IDSS IDSS IGSSF IGSSR VGS(th) VDS(on)	60 1.5 	10 100 100 100 100 4.5 4 0.08	Vdc μA nAdc nAdc
IDSS IGSSF IGSSR VGS(th) FDS(on)		100 100 100 4.5 4	μΑ nAde nAde
IGSSF IGSSR VGS(th)	1.5	100 100 100 4.5 4	nAdc nAdc
VGS(th) PDS(on) VDS(on)	1.5	100 4.5 4	nAdc Vdc
VGS(th) rDS(on) VDS(on)	1.5	4.5	Vdc
VGS(th) rDS(on) VDS(on)	1.5	4	
rDS(on) VDS(on)	1.5	4	
VDS(on)	*	0.08	Ohm
VDS(on)	N-TO-SOURCE V		
		2.4	Vdc
g _{FS}	6	regue 1,	mhos
WDSR	Ē	80 120 40	mJ
11 -00	i = Li	10	
Ciss		1600	pF
Coss		1000	إسبا
150		400	
- 11/1/			
td(on)	X	50	ns
	3/	450	
	-75A-	100	
		200	
	30 (Typ)	50	nC
-	15 (Typ)	_	1
	15 (Typ)	A 910515	
VSD	1.4 (Typ)	1.9	Vdc
		by stray inc	ductance
		_	ns
Ld	3.5 (Typ) 4.5 (Typ)		nH
L _S	7.5 (Typ)	-	
	Ciss Coss Crss td(on) tr td(off) tf Qg Qgs Qgd VSD ton trr Ld	Ciss — — — — — — — — — — — — — — — — — —	- 80 - 120 - 40 Ciss - 1600 Coss - 1000 Crss - 400 td(on) - 50 tr - 450 td(off) - 100 tf - 200 Qg 30 (Typ) 50 Qgs 15 (Typ) - Qgd 15 (Typ) - VSD 1.4 (Typ) 1.9 ton Limited by stray inc trr 300 (Typ) - Ld 3.5 (Typ) - Ld 3.5 (Typ) - Ls 7.5 (Typ) -

TYPICAL ELECTRICAL CHARACTERISTICS



1.1 VDS = VGS ID = 1 mA

VDS = VGS
ID = 1 mA

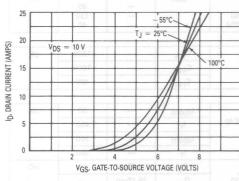
0.8 VDS = VGS
ID = 1 mA

1.1 VDS = VGS
ID = 1 mA

1.1 VDS = VGS
ID = 1 mA

Figure 1. On-Region Characteristics

Figure 2. Gate-Threshold Voltage Variation With Temperature



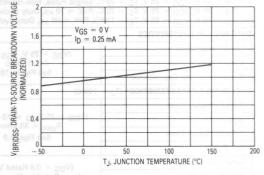
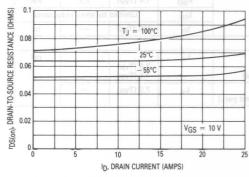


Figure 3. Transfer Characteristics

Figure 4. Breakdown Voltage Variation With Temperature



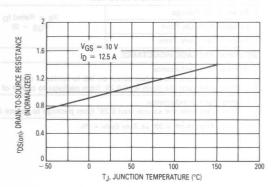


Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

80

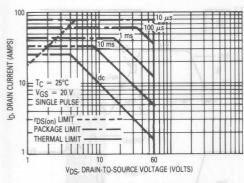


Figure 7. Maximum Rated Forward Biased Safe Operating Area

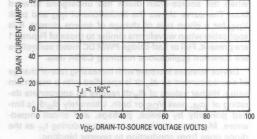


Figure 8. Maximum Rated Switching
Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

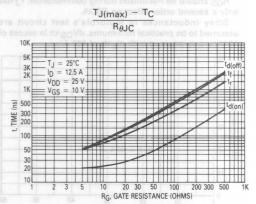


Figure 9. Resistive Switching Time Variation versus Gate Resistance

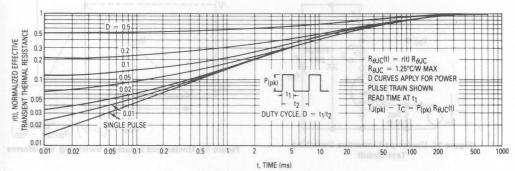


Figure 10. Thermal Response

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so $d_{\rm IS}/dt$ is specified with a maximum value. Higher values of $d_{\rm IS}/dt$ require an appropriate derating of $l_{\rm FM}$, peak $V_{\rm DS}$ or both. Ultimately $d_{\rm IS}/dt$ is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during $t_{\rm rr}$ as the diode goes from conduction to reverse blocking.

VDS(pk) is the peak drain-to-source voltage that the device must sustain during commutation; IFM is the maximum forward source-drain diode current just prior to the onset of commutation.

 V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as IS decays from I_{RM} to zero.

RGS should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_{S}/dt of 400 $A/\mu s$.

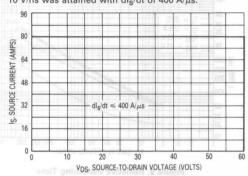


Figure 12. Commutating Safe Operating Area (CSOA)

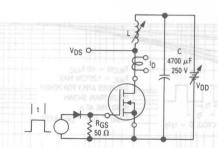


Figure 14. Unclamped Inductive Switching Test Circuit

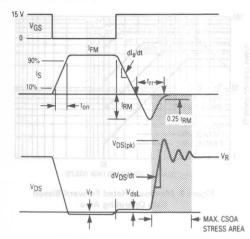


Figure 11. Commutating Waveforms

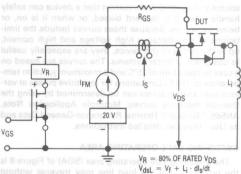


Figure 13. Commutating Safe Operating Area
Test Circuit

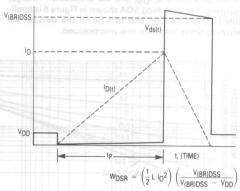
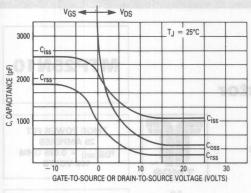


Figure 15. Unclamped Inductive Switching Waveforms



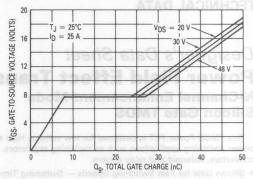
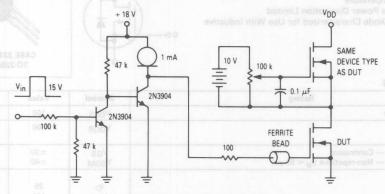


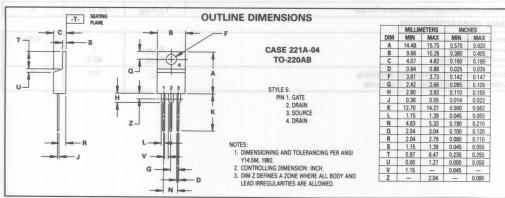
Figure 16. Capacitance Variation

Figure 17. Gate Charge versus Gate-to-Source Voltage



 $V_{in} = 15 V_{pk}$; PULSE WIDTH $\leq 100 \mu s$, DUTY CYCLE $\leq 10\%$

Figure 18. Gate Charge Test Circuit



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

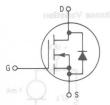
This TMOS Power FET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds Switching Times Specified at 100°C
- Designer's Data IDSS, VDS(on), VGS(th) and SOA Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FET

25 AMPERES rDS(on) = 0.085 OHM 100 VOLTS





CASE 221A-04 TO-220AB

MAXIMUM RATINGS

Daniel Intilitati					
Ratin	ng	2113904	Symbol	Value	Unit
Drain-Source Voltage			VDSS	100	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	FERRITE READ		VDGR	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive (t _p ≤	50 μs)		V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current Continuous Pulsed	a DUTY CYCLF ≈ 10%	 V _{Ab} . PULSE WIDTH ≈ 100 us	I _D	25 100	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	Feet Circuit	urs 18. Gate Charge	PD	125 1	Watts W/°C
Operating and Storage Temperature Range		CONTRACT WAS IN SAID	TJ, Tstg	-65 to 150	°C

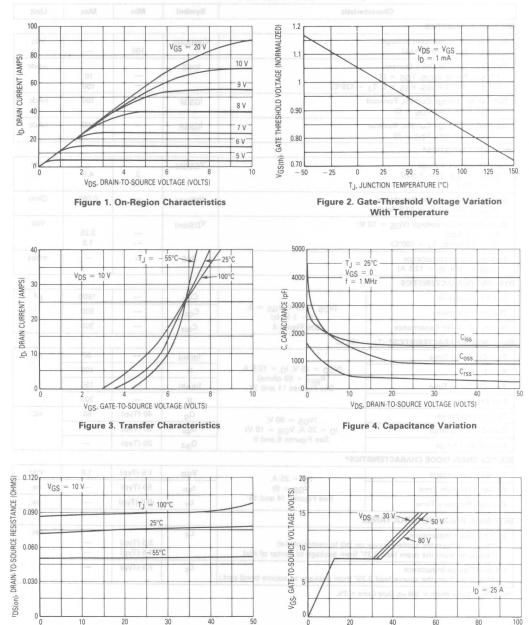
THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	CASE 221A-94 TO-229AB	R _θ JC R _θ JA	1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		A TL	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

	teristic	Symbol	Min	Max	Unit
FF CHARACTERISTICS	1 8 1				001
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)		V(BR)DSS	100	_	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ	= 125°C)	IDSS		10 100	μAdc
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	WI S VS	IGSSF		100	nAdc
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	7.7 = 0.80	IGSSR		100	nAdc
N CHARACTERISTICS*	5 5				
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C			2 1.5	4.5	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, I _D = 12.5 Adc)			On-Kagion (0.085	Ohm
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 25 \text{ Adc}$) ($I_D = 12.5 \text{ Adc}$, $T_J = 100^{\circ}\text{C}$)			Ξ	2.25 1.8	Vdc
Forward Transconductance (V _{DS} = 10 V, I _D = 12.5 A)			- 5	-	mhos
YNAMIC CHARACTERISTICS	M.1 = 1 000 0101	77/1		101 - 801	30
Input Capacitance		Ciss		1600	pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0, \\ f = 1 \text{ MHz})$	Coss		800	
Reverse Transfer Capacitance	See Figure 4	C _{rss}		300	05
WITCHING CHARACTERISTICS* (TJ	= 100°C)				
Turn-On Delay Time	/ copr	td(on)	1	60	ns
Rise Time	$(V_{DD} = 25 \text{ V}, I_{D} = 12.5 \text{ A},$	tr	AFF	450	
Turn-Off Delay Time	R _{gen} = 50 ohms) See Figures 11 and 12	td(off)	1535	150	
Fall Time TIOVI STATION STRUCK OT WARD	LanV	tf	W 300 U/33 OF 5	300	0
Total Gate Charge	(V _{DS} = 80 V,	Qg	40 (Typ)	60	nC
Gate-Source Charge	I _D = 25 A, V _{GS} = 10 V)	Qgs	20 (Typ)	Flaure 3	
Gate-Drain Charge	See Figures 6 and 9	Q_{gd}	20 (Typ)	_	
OURCE DRAIN DIODE CHARACTERIS	TICS*				
Forward On-Voltage	(Is = 25 A,	V _{SD}	1.5 (Typ)	1.8	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	50 (Typ)	_V(0) =	ggV ns
Reverse Recovery Time	See Figures 14 and 15	t _{rr}	450 (Typ)		ns
ITERNAL PACKAGE INDUCTANO	E Section 19		n/ac		000
Intérnal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		Ld	3.5 (Typ) 4.5 (Typ)		nH 080
Internal Source Inductance (Measured from the drain lead 0.25" from package to center of die)			L _s 7.5 (Typ)		



I_D, DRAIN CURRENT (AMPS)

Figure 5. On-Resistance versus Drain Current

Figure 6. Gate Charge versus Gate-To-Source Voltage

Q_q, TOTAL GATE CHARGE

SAFE OPERATING AREA INFORMATION

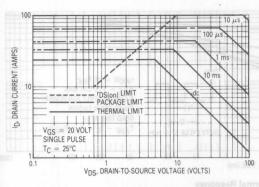


Figure 7. Maximum Rated Forward Biased Safe Operating Area

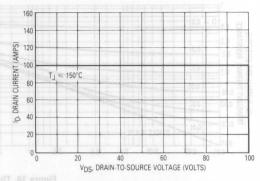


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

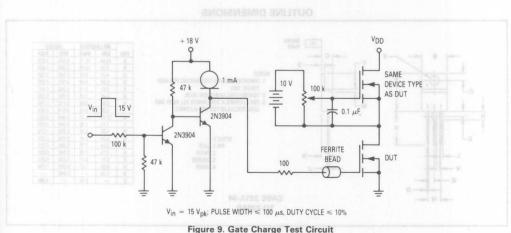
The FBSOA curves define the maximum drain-tosource voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$





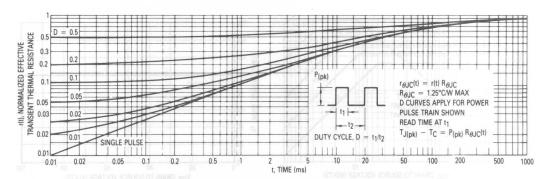


Figure 10. Thermal Response

RESISTIVE SWITCHING

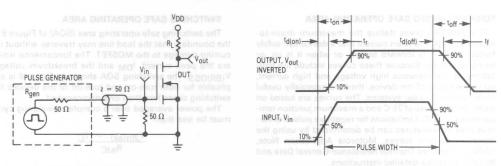
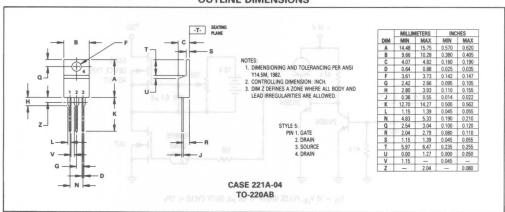


Figure 11. Switching Test Circuit

Figure 12. Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

TMOS IV Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate

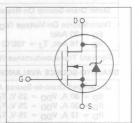
This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace
 External Zener Transient Suppressor Absorbs High
 Energy in the Avalanche Mode Unclamped
 Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- · Diode is Characterized for Use in Bridge Circuits
- Equivalent to IRFZ30



MTP30N05E

TMOS POWER FETS 30 AMPERES rDS(on) = 0.05 OHM 50 VOLTS





CASE 221A-04 TO-220AB

MAXIMUM RATINGS (T.) = 25°C unless otherwise noted)

	Rating	Type = 0.8 hated vpss.	Symbol	Value	Unit
Drain-Source Voltage	200	See Figures 17 and 18	V _{DSS}	50 STATE	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)			VDGR	MAHO 50 ON MA	Vdc
Gate-Source Voltage — Continuous — Non-repetitiv	$ve\ (t_p \le 50\ \mu s)$	(IS = 30 A	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	113	0 201	I _D	30 80	Adc
Total Power Dissipation @ T _C = 25°C	C bd		PD	75 0.6	Watts W/°C
Operating and Storage Temperature	Range	(eib to senter of die)	T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

HENWAL CHANACTERISTICS				
Thermal Resistance — Junction to Case	in package to source bond part.)	$R_{\theta JC}$	1.67	°C/W
 Junction to Ambient 		R _θ JA	62.5	Pulse Test: Pu
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		TL	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

OFF CHARACTERISTICS			-		
		V	FO		Vale
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)		V(BR)DSS	12 50 8 18	91'S D	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0,	T _J = 125°C)	IDSS	- N	10 100	μΑ
Gate-Body Leakage Current, Forwa	ard (VGSF = 20 Vdc, VDS = 0)	IGSSF	THE D	100	nAdc
Gate-Body Leakage Current, Rever	rse (V _{GSR} = 20 Vdc, V _{DS} = 0)	IGSSR	meens	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (VDS = VGS, ID = 250 μ A) TJ = 100°C	ETs is designed to withstand high. These new energy efficient devices y times. Designed for low voltage,	VGS(th)	20MT lo as limin 20 brid lim 1.5 oib	edo 4	Vdc
Static Drain-Source On-Resistance	(VGS = 10 Vdc, ID = 16 Adc)	rDS(on)	ni en <u>o</u> itsori	0.05	Ohm
Drain-Source On-Voltage (V _{GS} = (I _D = 30 Adc) (I _D = 16 Adc, T _J = 100°C)	V _{DS(on)}	ng a <u>re</u> a are ants_	1.65 1.4	Vdc	
Forward Transconductance (VDS	= 15 V, I _D = 16 A)	9 _{FS}	9	manu- <u>or</u> -una	mhos
DRAIN-TO-SOURCE AVALANCHE CH	The state of the s	heamsian! I -	ont Supprot	oslava sul	La series de la constante de l
Unclamped Drain-to-Source Avala (I _D = 80 A, V _{DD} = 25 V, T _C = 3 (I _D = 30 A, V _{DD} = 25 V, T _C = 3 (I _D = 12 A, V _{DD} = 25 V, T _C = 3	WDSR	UIS) Energy rating Area	90 180 -70	In Lmilive	
DYNAMIC CHARACTERISTICS	activity s of etc	me Comparat	Recovery Ti	. n Diode	dayl-rayio
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$	Ciss	y Di <u>ad</u> e	1600	pF
Output Capacitance	f = 1 MHz	Coss	3 HI 980 101	800	May sond
Reverse Transfer Capacitance	See Figure 16	C _{rss}	_	200	
SWITCHING CHARACTERISTICS* (T	J = 100°C)				
Turn-On Delay Time		t _{d(on)}	_	25	ns
Rise Time	$(V_{DD} = 25 \text{ V}, V_{GS} = 0,$ f = 1 MHz)	t _r	_	35	
Turn-Off Delay Time	See Figure 9	[†] d(off)	_	45	
Fall Time		tf	_	35	
Total Gate Charge	(VDS = 0.8 Rated VDSS,	Qg	26 (Typ)	30	nC
Gate-Source Charge	ID = Rated ID, VGS = 10 V)	Qgs	14 (Typ)	_	
Gate-Drain Charge	See Figures 17 and 18	Qgd	12 (Typ)	<u> 90</u> 0 m	i ilin estat
SOURCE DRAIN DIODE CHARACTER	RISTICS*		(103/11)	- 80 ⁶ 11.0	n 5% 25ml
Forward On-Voltage	(IS = 30 A	V _{SD}	a <u>na</u> unita	1.6	Vdc
Forward Turn-On Time	V _{GS} = 0)	ton	Limited	by stray inc	luctance
Reverse Recovery Time	MAG	t _{rr}	160 (Typ)	paging —	ns
NTERNAL PACKAGE INDUCTANCE	63		Tr = 25°C	ng) ng)antre	(I said la
Internal Drain Inductance (Measured from the contact scre (Measured from the drain lead (ew on tab to center of die) 0.25" from package to center of die)	Ld	3.5 (Typ) 4.5 (Typ)	over Jur <u>ig</u> e Tei	nH
Internal Source Inductance	,				AD JAMES

TENNAL PACKAGE INDUCTANCE				
Internal Drain Inductance	Ld		EGIS 4	nH
(Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	8	3.5 (Typ) 4.5 (Typ)	at agrant	
Internal Source Inductance	Ls	7.5 (Typ)	SINS LUANS	
(Measured from the source lead 0.25" from package to source bond pad.)		ction to Casi	mit — socut	

^{*}Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

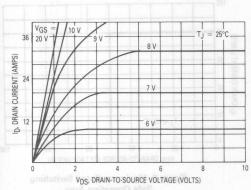


Figure 1. On-Region Characteristics

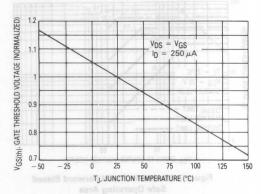


Figure 2. Gate-Threshold Voltage Variation With Temperature

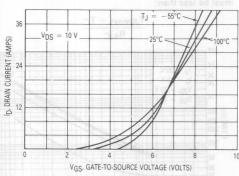


Figure 3. Transfer Characteristics

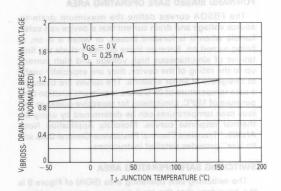


Figure 4. Breakdown Voltage Variation
With Temperature

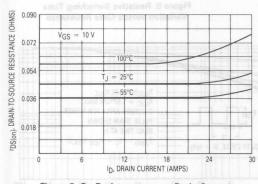


Figure 5. On-Resistance versus Drain Current

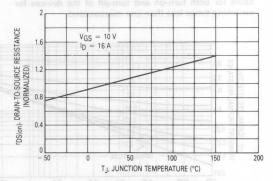


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

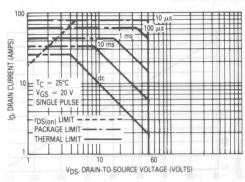


Figure 7. Maximum Rated Forward Biased Safe Operating Area

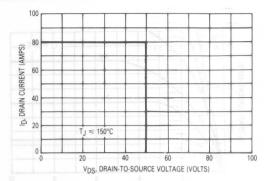


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V_{\mbox{\footnotesize (BR)DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

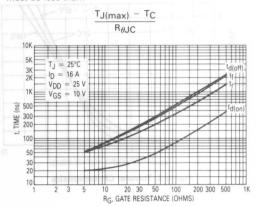


Figure 9. Resistive Switching Time Variation versus Gate Resistance

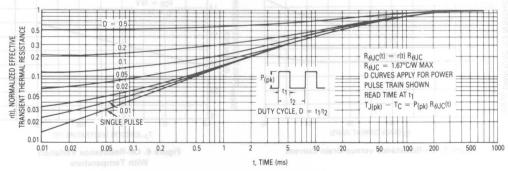


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of IFM and peak VDS for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dl_S/dt is specified with a maximum value. Higher values of dls/dt require an appropriate derating of IFM, peak VDS or both. Ultimately dls/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during trr as the diode goes from conduction to reverse blocking.

VDS(pk) is the peak drain-to-source voltage that the device must sustain during commutation; IFM is the maximum forward source-drain diode current just prior to the onset of commutation.

VR is specified at 80% of V(BR)DSS to ensure that the CSOA stress is maximized as IS decays from IRM to zero.

RGS should be minimized during commutation. TJ has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dVps/dt in excess of 10 V/ns was attained with dls/dt of 400 A/μs.

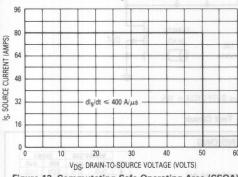


Figure 12. Commutating Safe Operating Area (CSOA)

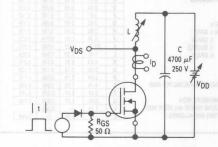


Figure 14. Unclamped Inductive Switching **Test Circuit**

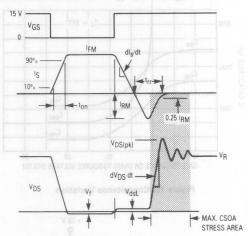


Figure 11. Commutating Waveforms

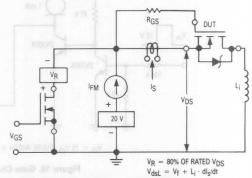


Figure 13. Commutating Safe Operating Area **Test Circuit**

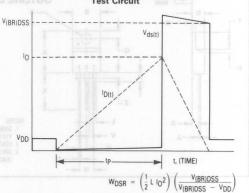


Figure 15. Unclamped Inductive Switching Waveforms

3

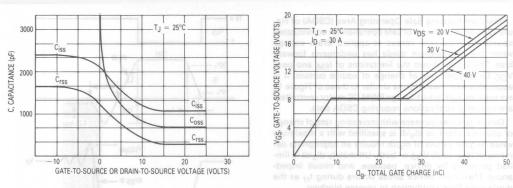


Figure 16. Capacitance Variation

Figure 17. Gate Charge versus Gate-to-Source Voltage

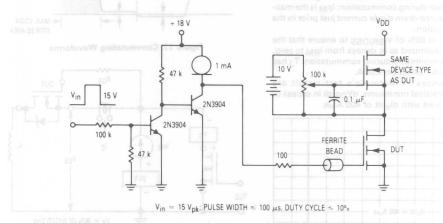
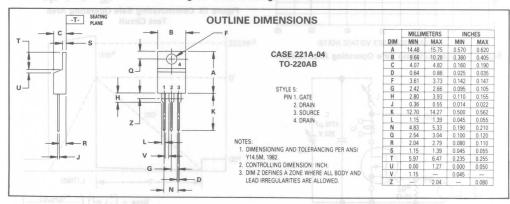


Figure 18. Gate Charge Test Circuit



gure 15. Unclamped inductive Switching Waveforms

Signia (4. Undemped Inductive switching

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

TMOS IV

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate

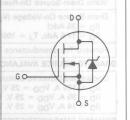
This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits





TMOS POWER FET 35 AMPERES rDS(on) = 0.055 OHM 60 VOLTS



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

	Rating	(no)b [†]	Symbol	Value	Unit
Drain-Source \	/oltage	n ³	V _{DSS}	60	Vdc
Drain-Gate Vo	tage (R _{GS} = 1 M Ω)	(No)b ¹	VDGR	60	Vdc
Gate-Source V	oltage — Continuous — Non-repetitive ($t_p \le 50 \ \mu s$	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
	— Continuous (T _C = 2 — Pulsed	25°C)	IDM	35 120	Adc
Total Power D Derate abov	issipation @ T _C = 25°C e 25°C	pôp	PD	125 1	Watts W/°C
Operating and	Storage Temperature Ra	nge	TJ, Tstg	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	R _θ JC	1	E (TO-220)
Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L (ed)	275	crew co-tab to c 0.25" from pact



CASE 221A-04 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Chai	racteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)			V(BR)DSS	60	O = Te	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, T_J = 125°C)				na - n	10 80	μΑ
Gate-Body Leakage Current, Forwa	rd (VGSF =	20 Vdc, V _{DS} = 0)	IGSSF	N 10 90000 (10 to 10	100	nAdc
Gate-Body Leakage Current, Revers	se (VGSR =	20 Vdc, V _{DS} = 0)	IGSSR	MERCATION	100	nAdc
N CHARACTERISTICS*	dold ba	etadiju ni bazniyah si aT	TRACES	POMET No. of	aleste III II	oures has
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C				2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	(VGS = 10)	/dc, I _D = 17.5 Adc)	rDS(on)	rticul a dy w	0.055	Ohm
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 35 Adc) (I _D = 17.5 Adc, T _J = 100°C)				ig area area ents.— Diode Des	2.3	Vdc
Forward Transconductance (VDS =	= 15 V, I _D =	17.5 A) dpiH s	d oed 9FS	estac142 the	enc T ransi	mhos
RAIN-TO-SOURCE AVALANCHE CH.	ARACTERIST	rics	Unclamped -	- ebolvi eri:	ne Avalant	Til Victor
Unclamped Inductive Switching Energy See Figures 14 and 15 (ID = 120 A, VDD = 25 V, TC = 25°C, Single Pulse, Non-repetitive) (ID = 35 A, VDD = 25 V, TC = 25°C, P.W. \leq 70 μ s, Duty Cycle \leq 1%) (ID = 14 A, VDD = 25 V, TC = 100°C, P.W. \leq 60 μ s, Duty Cycle \leq 1%)		W _{DSR}	rating Area	80 175 65	mJ	
YNAMIC CHARACTERISTICS	SERVICE SERVICE	8 0) 9	ildərsqmqQ ən	necovery the	rapalti nis	ICHBI-BOT
Input Capacitance	()	/ _{DS} = 25 V, V _{GS} = 0,	Ciss	or Use in B	3000	pF
Output Capacitance		f = 1 MHz	Coss	_	1500	
Reverse Transfer Capacitance		See Figure 16	C _{rss}	_	500	1
WITCHING CHARACTERISTICS* (TJ	100°C)	(b)	s otherwise note	- 25°C unless	(T) 80Mh.	AF MUM
Turn-On Delay Time	rield	euteV ladmyl	t _d (on)	- 8	60	ns
Rise Time	(V _{DD}	= 25 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms)	t _r	_	450	umpos ii
Turn-Off Delay Time	abV	See Figure 9	[†] d(off)	(t) M t i	2 150	pt sign-n
Fall Time	Vde	Vgs ±20	tf	ntinu gu s	300	า เทยอริษ
Total Gate Charge	XqV (V	DS = 0.8 Rated VDSS,	Ω_{g}	60 (Typ)	90	nC
Gate-Source Charge	ID =	= Rated ID, VGS = 10 V)	Qgs	33 (Typ)	- Co <u>nt</u> inuo	insticut ti
Gate-Drain Charge		See Figures 17 and 18	Qgd	35 (Typ)		
OURCE DRAIN DIODE CHARACTER	ISTICS*	1		3 0x 31	2 23 s	vedri stene
Forward On-Voltage	0	(I _S = 35 A	V _{DS}	1.7 (Typ)	2.5	Vdc
Forward Turn-On Time		$V_{GS} = 0$	ton	Limited	by stray ind	uctance
Reverse Recovery Time	Allego	$dl_S/dt = 100 A/\mu s$	t _{rr}	200 (Typ)		ns
NTERNAL PACKAGE INDUCTANCE	(TO-220)	Redic			aut.3	of null an
Internal Drain Inductance (Measured frrom the contact screw on tab to center of die)			L _d	3.5 (Typ) 4.5 (Typ)	ineid w	nH
	Measured from the contact screw on tab to center of die) Measured from the drain lead 0.25" from package to center of die) Pernal Source Inductance				9869 7777	I learnail

^{*}Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

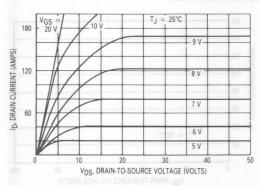


Figure 1. On-Region Characteristics

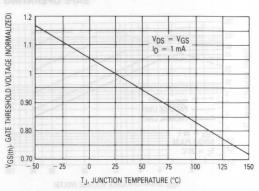


Figure 2. Gate-Threshold Voltage Variation
With Temperature

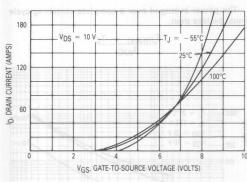


Figure 3. Transfer Characteristics

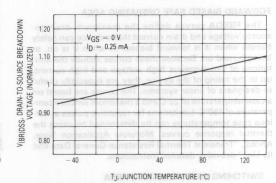


Figure 4. Breakdown Voltage Variation
With Temperature

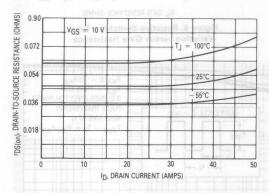


Figure 5. On-Resistance versus Drain Current

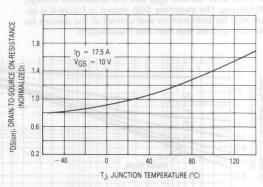


Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

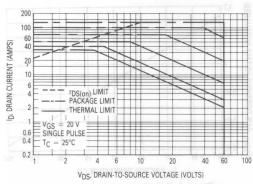


Figure 7. Maximum Rated Forward Biased
Safe Operating Area

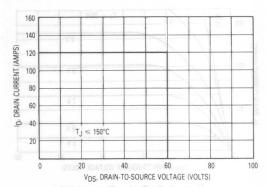


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{\mbox{\footnotesize DM}}$ and the breakdown voltage, $V(\mbox{\footnotesize BR})_{\mbox{\footnotesize DSS}}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

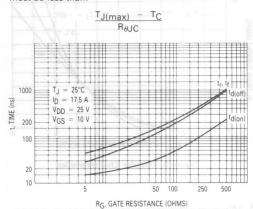


Figure 9. Resistive Switching Time Variation versus Gate Resistance

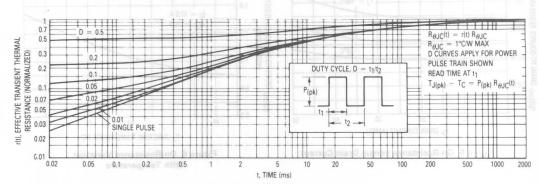


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of IFM and peak VDS for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so $dl_{\rm S}/dt$ is specified with a maximum value. Higher values of $dl_{\rm S}/dt$ require an appropriate derating of $l_{\rm FM}$, peak $V_{\rm DS}$ or both. Ultimately $dl_{\rm S}/dt$ is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during $t_{\rm rr}$ as the diode goes from conduction to reverse blocking.

 $V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; IFM is the maximum forward source-drain diode current just prior to the onset of commutation.

 $V_{\mbox{\scriptsize R}}$ is specified at 80% of $V_{\mbox{\scriptsize (BR)DSS}}$ to ensure that the CSOA stress is maximized as IS decays from IRM to zero.

RGS should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dl_{S}/dt of 400 A/ μ s.

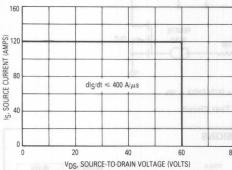


Figure 12. Commutating Safe Operating Area (CSOA)

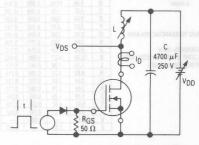


Figure 14. Unclamped Inductive Switching Test Circuit

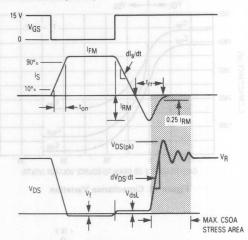


Figure 11. Commutating Waveforms

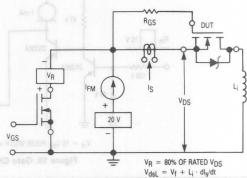


Figure 13. Commutating Safe Operating Area Test Circuit

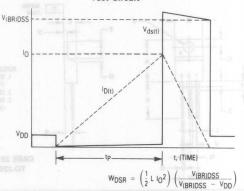


Figure 15. Unclamped Inductive Switching Waveforms

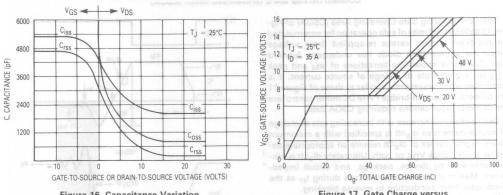


Figure 16. Capacitance Variation

Figure 17. Gate Charge versus Gate-to-Source Voltage

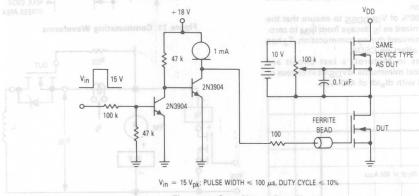
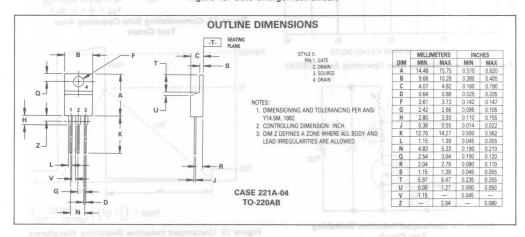


Figure 18. Gate Charge Test Circuit



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Advance Information

TMOS IV N-Channel Enhancement-Mode Power Field Effect Transistor

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits.
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode.
- Diode is Characterized for Use in Bridge Circuits.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	12	Symbol	MTP3055E	Unit
Drain-Source Voltage	(flo)b [†]	VDSS	60	Vdc
Drain-Gate Voltage (RGS = 1 M Ω)	48	VDGR	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive (tp	≦ 50 μs)	V _{GS} V _{GSM}	benefit ± 20 ag// ± 40 = =	Vdc Vpk
Drain Current — Continuous — Pulsed	bgO	I _D	12 26	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	osv	PD	40 0.32	Watts W/°C
Operating and Storage Temperature Range	e nol	T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	ReJC	3.12	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L _{slb 10}	275	°C

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA)	V(BR)DSS	60	_	Vdc
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = Rated VDSS, VGS = 0, TJ = 125°C)	IDSS	=	10 80	μΑ

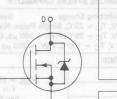
(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MTP3055E

TMOS POWER FET
12 AMPERES

rDS(on) = 0.15 OHM
60 VOLTS



TMOS





NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI '914-5M, 1982.

2. CONTROLLING DIMENSION: INCH.

3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALL DOWED.

	MILLIN	METERS	INC	HES
MIC	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
В	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
Н	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
0	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
٧	1.15	-	0.045	-
Z	-	2.04	-	0.080

CASE 221A-04 TO-220AB

ELECTRICAL CHARACTERISTICS — continued (T _C = 25°C unl	less otherwise noted)		
Characteristic	Symbol	Min	Max

Characteristic			Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued)					W # E	47. 82 B
Gate-Body Leakage Current, Forw	ard (Vo	GSF = 20 Vdc, V _{DS} = 0)	IGSSF	_	100	nAdc
Gate-Body Leakage Current, Reve	rse (Vo	SSR = 20 Vdc, VDS = 0)	IGSSR	ed-ni	100	nAdc
ON CHARACTERISTICS*			in an discount in the		337 6.1.	
Gate Threshold Voltage (VDS = VGS, ID = 1 mA) TJ = 100°C				2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance	(VGS	= 10 Vdc, I _D = 6 Adc)	rDS(on)	gnema -w ran s	0.15	Ohm
Drain-Source On-Voltage (VGS = (ID = 12 Adc) (ID = 6 Adc, TJ = 100°C)	10 V)	a- a- on-	VDS(on)	iodes with tigh <u>spe</u> ed s hver <u>te</u> rs and	1.5	Vdc
Forward Transconductance (VDS	Forward Transconductance ($V_{DS} = 15 \text{ V}, I_{D} = 6 \text{ A}$)			4	had snagd	mhos
PRAIN-TO-SOURCE AVALANCHE ST	RESS	CAPABILITY	nigram vastas l	fer additions	to bns (issue	Tho end ed
Unclamped Inductive Switching Energy See Figures 15 and 16 (ID = 26 A, VDD = 6 V, TC = 25°C, Single Pulse, Non-repetitive) (ID = 12 A, VDD = 6 V, TC = 25°C, P.W. \leq 200 μ s, Duty Cycle \leq 1%) (ID = 4.8 A, VDD = 6 V, TC = 100°C, P.W. \leq 200 μ s, Duty Cycle \leq 1%)			ned to Replace or Absorbs I	nt St up presix		mJ
YNAMIC CHARACTERISTICS	4			(S) Energy C		2 6/10/16
Input Capacitance	1	(V _{DS} = 25 V, V _{GS} = 0,	Ciss	l eest onite	500	pF
Output Capacitance	7	f = 1 MHz	Coss	idge C ircuits	300	(52) (m.). (52) (1-9)
Reverse Transfer Capacitance	3	See Figure 11	C _{rss}	scove <u>ry</u> Time	100	
WITCHING CHARACTERISTICS* (T	J = 10	00°C)	athieri'i ani	Diode.	nt hexiset for	to Visit al
Turn-On Delay Time			t _{d(on)}	25°C unless s	20	ns
Rise Time	Jink	$(V_{DD} = 25 \text{ V}, I_{D} = 0.5 \text{ Rated } I_{D})$	t _r	- 10	60	
Turn-Off Delay Time	16V	R _{gen} = 50 ohms) See Figure 18	td(off)	_	65	V sennag
Fall Time	ydy	Vones 60	tf	TD8/LT	65	PoV etai
Total Gate Charge	yov	(VDS = 0.8 Rated VDSS,	Qg	12 (Typ)	17	nC
Gate-Source Charge	JqV	I _D = Rated I _D , V _{GS} = 10 V)	Qgs	6.5 (Typ)	noV -	
Gate-Drain Charge	state.	See Figure 14	Q _{gd}	5.5 (Typ)	Continuous	TOWN THE
OURCE DRAIN DIODE CHARACTER	RISTICS	* MO			Pibiting	
Forward On-Voltage	2000	(IFM = 0.5 Rated ID,	V _{SD}	1.7 (Typ)	2	Vdc
Forward Turn-On Time	D#:	$dl_S/dt = 100 \text{ A/}\mu\text{s}, \text{ V}_{GS} = 0)$	ton	Limited	by stray ind	uctance
Reverse Recovery Time			t _{rr}	50 (Typ)	90	ns
NTERNAL PACKAGE INDUCTANCE	(TO-22	0)		and the state	in and	
Internal Drain Inductance (Measured from the contact scre			L _d	3.5 (Typ)	bnut — Junal Junalanut	nH

Internal Source Inductance

(Measured from the drain lead 0.25" from package to center of die)

(Measured from the source lead 0.25" from package to source bond pad.)

4.5 (Typ)

7.5 (Typ)

3

TYPICAL ELECTRICAL CHARACTERISTICS

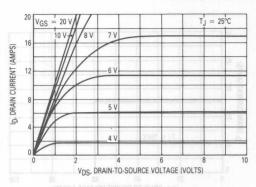


Figure 1. On-Region Characteristics

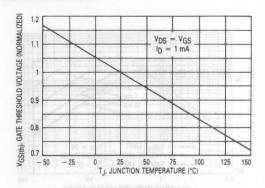


Figure 2. Gate-Threshold Voltage Variation
With Temperature

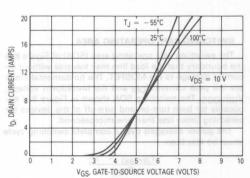


Figure 3. Transfer Characteristics

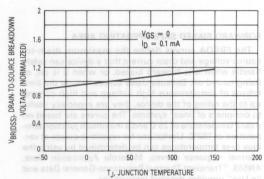


Figure 4. Breakdown Voltage Variation
With Temperature

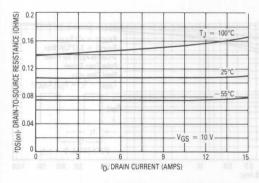


Figure 5. On-Resistance versus Drain Current

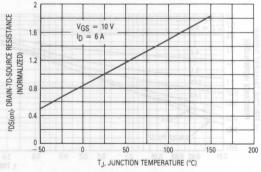


Figure 6. On-Resistance Variation
With Temperature

SAFE OPERATING AREA INFORMATION

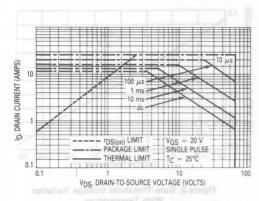


Figure 7. Maximum Rated Forward Biased Safe Operating Area

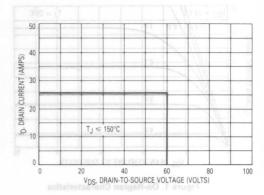


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

 $T_{J(max)} - T_{C}$

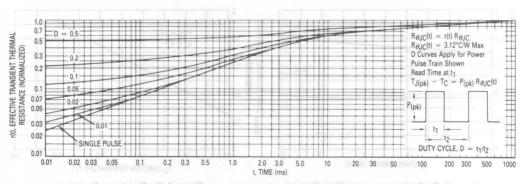


Figure 9. Thermal Response

3

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of IFM and peak VR for a given commutation speed. It is applicable when waveforms similar to those of Figure 10 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM} , peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

V_{DS(pk)} is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of V_{(BR)DSS} to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

RGS should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, $L_{\hat{i}}$ in Motorola's test circuit are assumed to be practical minimums.

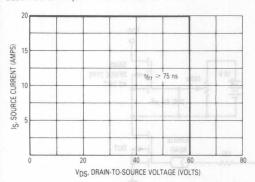


Figure 11. Commutating Safe Operating Area (CSOA)

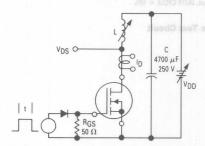


Figure 13. Unclamped Inductive Switching Test Circuit

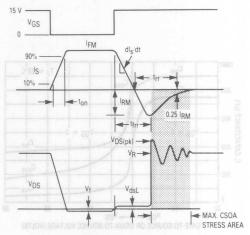


Figure 10. Commutating Waveforms

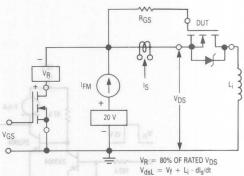


Figure 12. Commutating Safe Operating Area
Test Circuit

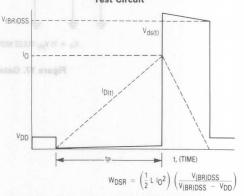


Figure 14. Unclamped Inductive Switching Waveforms

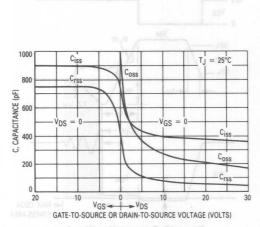


Figure 15. Capacitance Variation

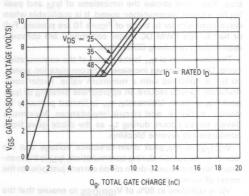


Figure 16. Gate Charge versus Gate-to-Source

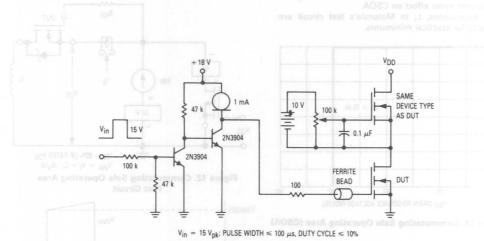


Figure 17. Gate Charge Test Circuit

13. Unclamped teductive Switching Year Circuit

MOTOROLA SEMICONDUCTOR **TECHNICAL DATA**

Advance Information

Power Field Effect Transistor

N-Channel Enhancement-Mode **Silicon Gate TMOS** with Current Sensing Capability

This TMOS Power FET with current sensing capability is designed for all power control applications where it is desirable to sense current such as in power supplies and motor controls. This device allows current sensing with a minimum of power loss.

DRAIN Q

TMOS

• "Lossless" Current Sensing for Maximum Efficiency - Sense Current is Reduced by a Factor of 950

- Ideal for Short Circuit/Overload Protection
- Simplifies Many Circuits When Used With Current Mode Integrated Circuits Such as the MC34129
- Kelvin Source Contact to Maximize Accuracy



required. MAXIMUM RATINGS (T_C = 25°C unless otherwise noted.)

to the Kelvin Terminal (K) when current sensing is not

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	60	Vdc
Drain-to-Gate Voltage (RGS = 1 MΩ)	VDGR	60	Vdc
Gate-to-Source Voltage — Continuous — Non-repetitive (t _p ≤ 50 μs)	V _{GS} V _{GSM}	20 ± 40	Vdc Vpk
Drain-to-Mirror Voltage	V _{DMS}	60	Vdc
Gate-to-Mirror Voltage	VGM	20	Vdc
Drain Current — Continuous — Pulsed	I _D	40 120	Amps
Sense Current — Continuous — Pulsed	IMM	45 130	mA
Total Power Dissipation @ T _C = 25°C Derate above 25°C	o PD	125 A 08 =1 0 V S	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

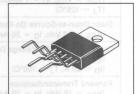
THERMAL CHARACTERISTICS

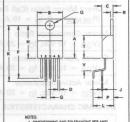
Thermal Resistance, Junction-to-Case		$R_{\theta JC}$	1	°C/W
Junction-to-Ambient	260	$R_{\theta JA}$	62.5	11
Maximum Lead Temperatu 1/8" from case for 5 seco		₁₃ F T _L	275	°C

This is advance information on a new introduction and specifications are subject to change without notice.

MTP40N06M

TMOS SENSEFET **40 AMPERES** rDS(on) = 0.04 OHM 60 VOLTS





PIN 1. GATE 2. MIRROR 4. KELVIN 3. DRAIN 5. SOURCE

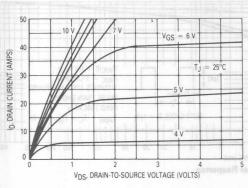
	MILLIN	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX		
A	15.49	15.88	0.610	0.625		
В	9.91	10.41	0.390	0.410		
C	4.32	4.57	0.170	0.180		
D	0.71	0.81	0.028	0.032		
F	20.83	21.59	0.820	0.850		
G	1.45	1.96	0.057	0.077		
Н	12.70	13.69	0.500	0.539		
J	0.38	0.64	0.015	0.025		
K	21.46	23.50	0.845	0.925		
L	8.00	8.38	0.315	0.330		
P	4.32	4.70	0.170	0.185		
Q	3.53	3.73	0.139	0.147		
R	0.89	1.40	0.035	0.055		
T	9.02	9.40	0.355	0.370		
٧	4.70	5.46	0.185	0.215		

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{MK} = 0 unless otherwise noted.)

LECTRICAL CHARACTERIS	1100 (1C - 25 C, VMK - 0 dil	ileaa ottiei vviae ii			1 1 1 1 1 1 1 1 1	100000
Charac	teristics	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown V (V _{GS} = 0, I _D = 0.25 mA)	/oltage	V(BR)DSS	60	ites over	a Inte	Vdc
Zero Gate Voltage Drain Curr (VDS = 60 V, VGS = 0) (VDS = 60 V, VGS = 0, TJ		IDSS	[h王 b	10 100	μAdc
Gate-Body Leakage Current – (VGSF = 20 Vdc, VDS = 0)		IGSSF	oM-Mo	ancemi ans	100	nAdc
Gate-Body Leakage Current – (VGSR = 20 Vdc, VDS = 0		IGSSR	Capab	ausing	100	nAdc
N CHARACTERISTICS*	ned for all power	sbility is design				
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = 1 \text{ mAdd})$ $(T_J = 125^{\circ}\text{C})$	to muminim a ri	VGS(th)	2 1.5	2.5	4 3.5	Vdc
Static Drain-to-Source On-Res (VGS = 10 Vdc, I _D = 20 A		rDS(on)	Cimu <u>m</u> Effici Factor of 9	0.03	0.04	Ohms
Drain-to-Source On-Voltage (VGS = 10 Vdc) (ID = 40 A) (ID = 20 A, T_J = 100°C)		V _{DS(on)}	d With Curt	1.2	1.8 1.8	Vdc
Forward Transconductance (V _{DS} = 15 Vdc, I _D = 20 A	dc)	9fs	12	r Disarpatio	OA is Powe 0.04 Gh	mhos
URRENT SENSING CHARACT	ERISTICS	n possina			1	
Current Mirror Ratio (Cell Rat (RSENSE = 0, ID = 10 A, V		ntvusx	900	tels tesisge for	960	porq p <u>elibre</u> ti al egne los kit seu to co
Mirror Compliance Ratio (VGS = 10 Vdc, ID = 20 A		suga K _{mc}	M) be shorted ting is not	0.67	sed that the e erminal (K) wit	to Kelvin I
Source Active Resistance (VGS = 10 Vdc, ID = 20 A	dc, R _S = 10 megohm)	ra(on)	a selvandro	17 telnu 0/85 =	OT) SOUTH	mΩ
Mirror Active Resistance (VGS = 10 Vdc, ID = 20 A	dc) say 68	rm(on)	-	16	apatloV s	Ohms
YNAMIC CHARACTERISTICS	09 V 08	andV I			Voltage	stap-of-ni
Input Capacitance		Ciss	_	_	1800	pF
Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0$ f = 1 MHz	20V Coss		Continuous	900	9-100-Sould
Transfer Capacitance	NOV 1 - 1 WIIIZ	C _{rss}	EN US - G// 1	seminoper mar	400	
WITCHING CHARACTERISTICS	S*	Sheri V			938910 Y	d novinos m
Turn-On Delay Time	004 08	td(on)		20	40	ns
Rise Time	V _{DD} = 25 V, I _D = 20 A	tr tr		20	40	in Current
Turn-Off Delay Time	R _{gen} = 50 Ohms	td(off)	_	60	100	nemub es
Fall Time	130	MMI tf	_	30	60	
Total Gate Charge	125 Worts	₫ ⁹ Qg	_	62	® no75	nC
Gate-Source Charge	V _{DS} = 48 V, I _D = 40 A	Qgs		27	0.07.0	Ode alste
Gate-Drain Charge	V _{GS} = 10 V	Q _{gd}	- DBI	35	leT egistoric	ins gnits:
OURCE-DRAIN DIODE CHARA	CTERISTICS*			8011	GIRZ CART	MO-SPOO
Forward On-Voltage	1910	V _{SD}	_	1.1	1.5	Vdc
Forward Turn-On Time	IS = 80 A	ton	_	260	treidm#	ns
Reverse Recovery Time	278 °C	JT trr	ng P ur goses	200	derecent b	red mamis

^{*}Indicates Pulse Test: Pulse Width = 300 µs max, Duty Cycle = 2%.

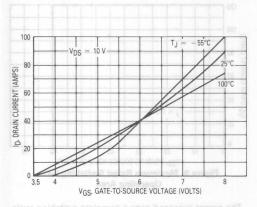
TYPICAL CHARACTERISTICS



1.2 VDS = VGS ID = 1 mA

Figure 1. On-Region Characteristics

Figure 2. Gate Threshold Voltage Variation with Temperature



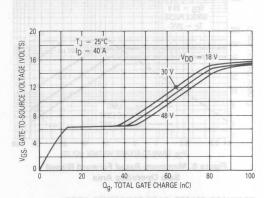
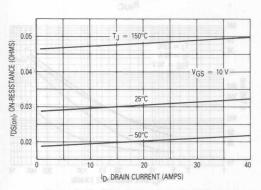


Figure 3. Transfer Characteristics

Figure 4. Stored Charge Variation



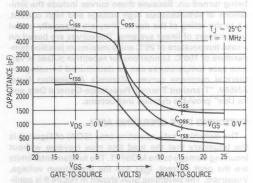


Figure 5. On-Resistance versus Drain Current

Figure 6. Capacitance Variation



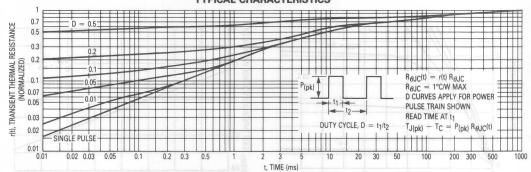
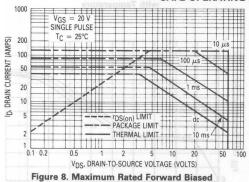


Figure 7. Thermal Response

SAFE OPERATING AREA INFORMATION



Safe Operating Area

100 DRAIN CURRENT (AMPS) 80 60 40 lDS, [i ≤ 150°C 20 VDS, DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 9. Maximum Rated Switching Safe **Operating Area**

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-tosource voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_{C}}{R_{\theta JC}}$$

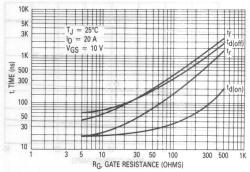


Figure 10. Resistive Switching Time Variation with Gate Resistance

SAFE OPERATING AREA INFORMATION

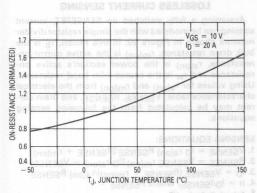


Figure 11. On-Resistance Variation with Temperature

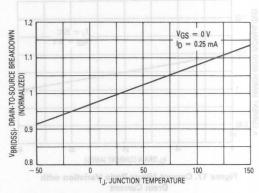


Figure 12. Breakdown Variation with Temperature

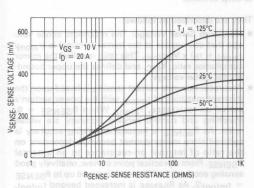


Figure 13. Sense Voltage Variation with Sense Resistance

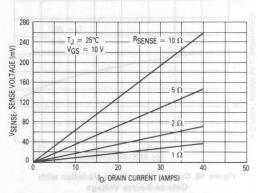


Figure 14. Sense Voltage Variation with Drain Current

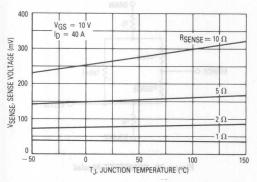


Figure 15. Sense Voltage Variation with Temperature

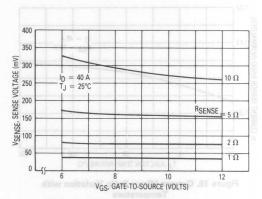


Figure 16. Sense Voltage Variation with Gate-to-Source Voltage

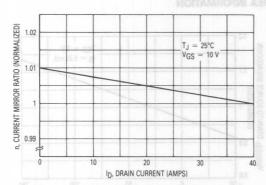


Figure 17. Current Mirror Ratio Variation with Drain Current

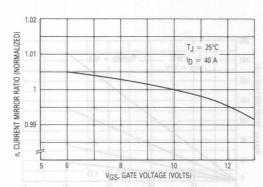


Figure 18. Current Mirror Ratio Variation with Gate-to-Source Voltage

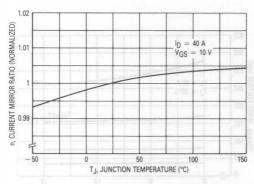


Figure 19. Current Mirror Ratio Variation with Temperature

LOSSLESS CURRENT SENSING

Assuming a fully switched on SENSEFET, current sensing can be modeled with the simple resistor divider network shown in Figure 20. In this model, r_b is the bulk drain resistance, $r_{m(on)}$ is the active mirror on-resistance, $r_{a(on)}$ is the power section's active on-resistance and r_w is the source wire bond resistance. Using values for $r_{a(on)}$ and $r_{m(on)}$ from the electrical characteristics table; VSENSE, RSENSE, and drain current may be calculated from the following sensing equations

SENSING EQUATIONS:

- 1. VSENSE = ID ra(on) RSENSE/[RSENSE + rm(on)]
- 2. RSENSE = VSENSE rm(on)/[ID ra(on) VSENSE]
- 3. ID = VSENSE (RSENSE + rm(on))/ra(on) RSENSE
- 4. n = ID/ISENSE; where RSENSE = 0
- 5. $r_{a(on)} = r_{m(on)}/n$

When using these equations there are several factors to keep in mind.

They are described as follows:

- Maximum Sense Voltage: The maximum sense voltage that can appear at the mirror terminal is (r_a(on)/r_a(on) + r_b) x V_{DS}(on). This ratio is called the mirror compliance ratio, K_{MC}, and defines the upper boundary for sense voltage.
- Accuracy: Accurate current sensing is based upon the inherent matching of $r_{m(on)}$ with the power section's active on-resistance, $r_{a(on)}$. When RSENSE = 0, matching and current sensing accuracy are within \pm 3%. As RSENSE is increased, sensing accuracy is reduced since mirror current becomes dependent on the ratio of internal on-resistance to an external RSENSE. From a practical point of view, relatively good sensing accuracy (\pm 10%) is maintained up to RSENSE = $r_{m(on)}/2$. As RSENSE is increased beyond $r_{m(on)}/2$ sensing accuracy decreases rapidly.

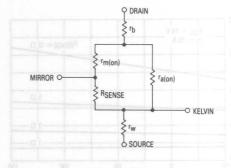


Figure 20. SENSEFET Model

- Ground Loop Errors: Lossless current sensing is a technique that looks for 100 mV signals in a loop that may carry tens or even hundreds of amps. The potential for ground loop errors in this kind of an application is a first order design consideration. Internal wire bond resistance, contact resistance, and external wiring resistance are all significant. Therefore, it is important to reference sense voltage measurement circuitry to the Kelvin pin rather than power ground. In addition, referencing gate drive to the Kelvin pin rather than power ground will provide faster switching speeds.
- Noise Suppression: Switching noise is also a first order design issue. Layout, therefore, is critical. In addition, a single pole RC filter between RSENSE and the current sensing circuitry's input terminals is often desirable. A 1 µsec time constant is generally long enough to provide adequate noise suppression and short enough to provide adequate protection during overloads. An illustration is provided in Figure 21.
- Double Pulse Suppression: In PWM circuits it is critically important to include double pulse suppression in the control circuit topology. If the current limit loop is

- allowed to oscillate at its natural frequency, failure of the SENSEFET is likely due to excessive power dissipation. By syncing current limiting to the clock with a latch, double pulse suppression architectures solve this problem, and provide effective protection from overload stress.
- Parasitic Diode: In addition to the power section's usual source-drain diode, there is a mirror-drain diode in the sense cells. Like the source-drain diode, the mirror-drain diode conducts during the reversemode operation, however, current sense characteristics are defined only in the forward-mode operation.
- Reverse Recovery: In bridge circuits, when a SENSE-FET's source-drain diode is commutated a voltage spike is produced at the mirror. This spike is short since it lasts only for the drain-source diode's reverse recovery time. However, its amplitude can be an order of magnitude larger than normal sense voltages and produce unwanted overcurrent trips. Blanking, filtering, or other suppression techniques may be required in some applications.

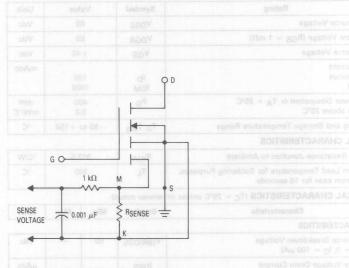


Figure 21. SENSEFET with Noise Suppression

MOTOROLA ■ SEMICONDUCTOR **TECHNICAL DATA**

Small-Signal Field Effect Transistor

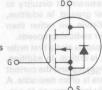
N-Channel Enhancement-Mode Silicon Gate TMOS

... are designed for high voltage, high speed applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Lamp Relay Driver or Buffer him add a besubong at saliga
- Analog Signal Switching
- duce unwanted overcurrent trips. Blanking, htering, or other suppression techniques may be required in some



VN0610LL



N-CHANNEL **SMALL-SIGNAL TMOS FET** rDS(on) = 5 OHMS 60 VOLTS



CASE 29-04 TO-226AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	60	Vdc
Drain-Gate Voltage (RGS = 1 m Ω)	VDGR	60	Vdc
Gate-Source Voltage	VGS	± 40	Vdc
Drain Current Continuous Pulsed	I _D	190 1000	mAdc
Total Power Dissipation (a, T _A = 25°C Derate above 25°C	PD	400 3.2	mW mW/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

1				
	Thermal Resistance Junction to Ambient	$R_{\theta JA}$	312.5	°C/W
	Maximum Lead Temperature for Soldering Purposes,	TL	300	°C

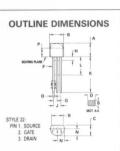
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				SURCION
Drain-Source Breakdown Voltage (VGS = 0, ID = 100 μ A)	V(BR)DSS	60	-	Vdc
Zero Gate Voltage Drain Current (VDS = 48 V, VGS = 0) (VDS = 48 V, VGS = 0, $T_J = 125$ °C)	IDSS	W TERES	10 500	μAdo
Gate-Body Leakage Current, Forward (VGSF = 30 Vdc, VDS = 0)	IGSSF	-	- 100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_{D} = 1$ mA)	V _{GS(th)}	0.8	2.5	Vdc
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 500 mA) (VGS = 10 Vdc, ID = 500 mA, TC = 125°C)	rDS(on)	=	5 9	Ohm

^{*}Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



NOTES:

1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED

2. DIM "F" APPLES BETWEEN "H" AND "L". DIM "D" & "S" APPLES BETWEEN "L" & 12/0mm (IOS 1) FROM SEATING PLANE LEAD DIM IS UNCONTROLLED IN "I" & BETWOOD 12/0mm (IOS 1) FROM SEATING PLANE

3. CONTROLLING DIM "MCM.

	MILLIN	METERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
A	4.32	5.33	0.170	0.210	
В	4.45	5.20	0.175	0.205	
C	3.18	4.19	0.125	0.165	
D	0.41	0.55	0.016	0.022	
F	0.41	0.48	0.016	0.019	
G	1.15	1.39	0.045	0.055	
H	-	2.54	_	0.100	
J	2.42	2.66	0.095	0.105	
K	12.70	-	0.500	-	
L	6.35	-	0.250	-	
N	2.04	2.66	0.080	0.105	
P	2.93	-	0.115	-	
R	3.43	_	0.135	_	
S	0.39	0.50	0.015	0.020	

CASE 29-04 TO-226AA

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ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted) Min Max Unit Characteristic Symbol ON CHARACTERISTICS* (continued) V_{DS}(on) Drain-Source On-Voltage Vdc $(V_{GS} = 5 \text{ V}, I_{D} = 200 \text{ mA})$ $(V_{GS} = 10 \text{ V}, I_{D} = 500 \text{ mA})$ 1.5 2.5 750 On-State Drain Current ($V_{GS} = 10 \text{ V}, V_{DS} \ge 2 \text{ V}_{DS(on)}$) mA ID(on) Forward Transconductance (V_{DS} ≥ 2 V_{DS(on)}, I_D = 500 mA) 100 μmhos 9fs **DYNAMIC CHARACTERISTICS** Input Capacitance Ciss 60 pF $V_{DS} = 15 \text{ V}, V_{GS} = 0,$ Output Capacitance 25 Coss f = 1 MHz Reverse Transfer Capacitance 5 Crss **SWITCHING CHARACTERISTICS*** Turn-On Delay Time 10 ns $V_{DD} = 15 \text{ V, } I_D = 600 \text{ mA}$ ton Rgen = 25 ohms, RL = 23 ohms Turn-Off Delay Time 10 toff *Pulse Test Pulse Width \leq 300 μ s, Duty Cycle \leq 2% = 25°0 $V_{DS} = 10 V$ 550 1.6 0.8 VGS = 10 V V CURRENT (AMPS) 1.4 CURRENT (AMPS) 9 V-8 V 7 V DRAIN 0.6 DRAIN 6 V-0.4 ف 5 V. 0.2 ف 4 V_ 0.2 - 3 V-0 VGS, GATE SOURCE VOLTAGE (VOLTS) VDS, DRAIN SOURCE VOLTAGE (VOLTS) Figure 1. Ohmic Region Figure 2. Transfer Characteristics ON-RESISTANCE 2.4 1.2 (NORMALIZED) 2.2 1.15 V_{GS} = 10 V $V_{DS} = V_{GS}$ $I_{D} = 1 \text{ mA}$ 1.1 2 $I_D = 200 \text{ mA}$ 1.8 1.05 DRAIN-SOURCE O (NORMALIZED) AGE 0.95 THRESHOLD 0.9 STATIC [0.85 0.8 0.8 rDS(on). \(\hat{q}\) 0.75 \\ 0.75 \\ 0.7 0.6 0.4 0.7 - 20 + 100 +140+20+60 +100+140T, TEMPERATURE (°C) T, TEMPERATURE (°C) Figure 3. Temperature versus Static Drain-Source Figure 4. Temperature versus Gate Threshold Voltage **On-Resistance**

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Small-Signal Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

... are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and GO relay drivers.



- Telecommunication Switch
- Lamp Relay Driver or Buffer
- Analog Signal Switching
- · Available in Radial Tape and Reel
- Available in Amo Pack

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	60	Vdc
Drain-Gate Voltage (R _{GS} = 1 mΩ)	VDGR	60	Vdc
Gate-Source Voltage	VGS	± 40	Vdc
Drain Current Continuous Pulsed	I _D	150 1000	mAdc
Total Power Dissipation (a T _A = 25°C Derate above 25°C	PD	400 3.2	mW/°C
Operating and Storage Temperature Range	TJ, Tstg	-55 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Ambient	$R_{\theta JA}$	312.5	°C/W
Maximum Lead Temperature for Soldering Purposes,	TL	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	-1en B			
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 100 μA)	V _{(BR)DSS}	60		Vdc
Zero Gate Voltage Drain Current (VDS = 48 V, VGS = 0)	IDSS		10	μAdc
$(V_{DS} = 48 \text{ V}, V_{GS} = 0, T_{J} = 125^{\circ}\text{C})$	05-	hf +	500	-08-4
Gate-Body Leakage Current, Forward (VGSF = 30 Vdc, VDS = 0)	IGSSF	80%	- 100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA)	V _{GS(th)}	0.6	2.5	Vdc
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 0.5 Adc) (V _{GS} = 10 Vdc, I _D = 0.5 V, T _C = 125°C)	rDS(on)	-	7.5 13.5	Ohm

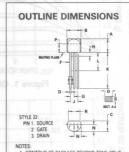
^{*}Pulse Test Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

(continued)



N-CHANNEL **SMALL-SIGNAL TMOS FET** rDS(on) = 7.5 OHMS 60 VOLTS





1. CUMTOUN OF PACAGE BETOND ZONE "P IS UNCONTROLLED.

2. DIM "F" APPLIES BETWEEN "L" & 12.70mm "D" 8"" "S PPLIES BETWEEN "L" & 12.70mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "I" & BEYOND 12.70mm (0.5") FROM SEATING PLANE.

3. CONTROLLING DIM: INCH.

	MILLIN	METERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
A	4.32	5.33	0.170	0.210	
В	4.45	5.20	0.175	0.205	
C	3.18	4.19	0.125	0.165	
D	0.41	0.55	0.016	0.022	
F	0.41	0.48	0.016	0.019	
G	1.15	1.39	0.045	0.055	
Н		2.54	_	0.100	
J	2.42	2.66	0.095	0.105	
K	12.70	-	0.500	_	
L	6.35	1-1	0.250		
N	2.04	2.66	0.080	0.105	
P	2.93	-	0.115	-	
R	3.43	-	0.135	-	
S	0.39	0.50	0.015	0.020	

CASE 29-04 TO-226AA

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Max	Unit
CHARACTERISTICS* (continu	ed)						
Orain-Source On-Voltage (VGS = 5 V, I _D = 200 mA) (VGS = 10 V, I _D = 500 mA)				V _{DS} (on)		1.5 3.75	Vdc
On-State Drain Current (VGS = 10 Vdc, V _{DS} ≥ 2 V _D	S(on))			ID(on)	750	_	mA
Forward Transconductance (V _{DS} = 10 V, I _D = 500 mA)				9fs	100	_	μmhos
NAMIC CHARACTERISTICS							
nput Capacitance				Ciss	_	60	pF
Output Capacitance	V _{DS} = 15 \ f = 1	$V_{\rm NHz} = 0$		Coss	_	25	
Reverse Transfer Capacitance		1011 12		C _{rss}	_	5	
/ITCHING CHARACTERISTICS*							
urn-On Delay Time	V _{DD} = 15 V,	In = 600 mA		ton	_	10	ns
urn-Off Delay Time	R _{gen} = 25 ohms		ns	toff	_	10	
lse Test Pulse Width ≤ 300 μs, Du	ity Cycle ≤ 2%.			OII		1	
2			1			1 1 1/	/25°C/
1.8 T _A = 25°C						1 /	1234
1.6		/ _{GS} = 10 V	0.8	$V_{DS} = 10$) V	-55°C//	//
\$ 1.4		9 4	S			1//	/125°C
W 1.2		34	A 0.6			1//	
E I		8 V	EN			1//	
8.0 GB		7 V	Š 04				
NE 0.6		6 V	AN AN				
1.4 DBAIN CURBENT AMPRS)		5 V.	D, DRAIN CURRENT (AMPS)				
0.2		4 V	_ 0.2				
0.2		3 V			//		
Figure 1.	5 6 7 8 URCE VOLTAGE (VOLTS) Ohmic Region	9 10	0	Fig		5 6 7 CE VOLTAGE (VOLT er Characteri	
2.2		6	1.2				
V _{GS} = 10 V		N IZ	1.15	1			$V_{DS} = V_{GS}$
2 ID = 200 mA		J. Wall	1.1	1			ID = 1 mA
1.8		N. II	1.05				
1.6 1.6 1.4 1.4 1.4 1.4 1.4 1.4 1.4 1.4 1.4 1.4		TAG	1				
1.4 AAA		\$	0.95				
≥ 1.2			0.9			++>	1
1		TS TS	0.85				1
2.4 2.2 VGS = 10 V 1 _D = 200 mA 1.8 1.6 1.6 1.6 0.8		Vecent THRESHOLD VOLTAGE INORMALIZED	0.8				+++
0.6		4	0.75				
0.4	+60 +10		0.7	60 - 20	0 +20	+ 60	100

+ 20 + 60 T, TEMPERATURE (°C) Figure 3. Temperature versus Static Drain-Source On-Resistance

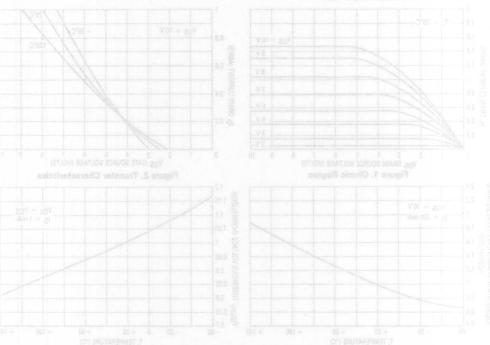
+ 100

VGS(th), THRESHO 0.82 0.72 0.72 0.7 + 140 - 60 0 + 20 T, TEMPERATURE (°C)

Figure 4. Temperature versus Gate Threshold Voltage

ELECTRICAL CHARACTERISTICS - continued ITc = 28°C unless otherwise noted

"Puls - Trace Pulse Width & 300 ws. Daty Oxelo < 2%



Rgure 3. Temparature versus Static Drain-Source
On-Resistance

TMOS INDEX CROSS-REFERENCE

MTMSN40 - MTM4N45 - MTP3N40	



H ogg9	Melocols Direct Replacement	

Ind	ex and (Cross Re	ference
3-227 3-27 3-27 3-482 3-482 3-32 3-32 3-32 3-467 3-467 3-467	MTM15N35 2N6768JTX MTM15N65 2N677GJTX	ZN6786 ZN6766JTX ZN6766 ZN6768 ZN676JTX ZN6760 ZN6770	2N6765 2N6765 2N6765/TX 2N6767 2N6768 2N6768AAN 2N6768JTX 2N6768JTXV 2N6768
3-37 3-42 3-42 3-44 			

TMOS INDEX CROSS-REFERENCE

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #	Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2N6659 2N6660 2N6660/750 2N6661/750 2N6755 2N6755 2N6756 2N6756JTX 2N6756JTXV 2N6757	2N6659 2N6660 2N6660/750 2N6661 2N6661/750 2N6756 2N6756JTX 2N6756JTXV	2N6756 2N6758		2N6801 2N6802 2N6823 2N6826 2N7000 2N7002 2N7008 2SK294 2SK295 2SK296	2N6823 2N6826 2N7000 2N7002 2N7008	MTP8N08 MTP8N10 MTP3N45	
2N6758 2N6758JTX 2N6758JTXV 2N6759 2N6760 2N6760JAN 2N6760JTX 2N6760JTXV 2N6761 2N6762	2N6758 2N6758JTX 2N6758JTXV 2N6759 2N6760 2N6760JTX 2N6760JTXV 2N6762	2N6760JTX MTM4N45	3-10 3-10 3-10 3-14 3-14 3-14 3-14 3-385 3-18	2SK298 2SK299 2SK310 2SK311 2SK312 2SK313 2SK319 2SK320 BS107 BS107A	BS107 BS107A	MTM5N40 MTM4N45 MTP3N40 MTP2N45 MTM8N40 MTM7N45 MTP5N40 MTP4N45	3-390 3-385 3-549 3-350 3-263 3-258 3-390 3-385
2N6762JAN 2N6762JTX 2N6762JTXV 2N6763 2N6764 2N6764JTX 2N6764JTXV 2N6765 2N6766 2N6766JTX	2N6762JTX 2N6762JTXV 2N6764 2N6764JTX 2N6764JTXV 2N6766 2N6766	2N6762JTX MTM35N06E MTM20N15	3-18 3-18 3-18 3-323 3-22 3-22 3-22 3-293 3-27 3-27	BS170 BSS89 BSS91 BSS93 BSS95 BSS97 BSS123 BUZ10 BUZ10A BUZ111	BSS89 BSS123 BUZ10A BUZ11	MFE9200 MFE9200 BS107 BS107 MTP25N05E	3-64 — 3-163 3-163 — 3-67 3-682 — 3-69
2N6766JTXV 2N6767 2N6768 2N6768JAN 2N6768JTX 2N6768JTXV 2N6769 2N6770 2N6770JAN 2N6770JAN	2N6766JTXV 2N6768 2N6768JTX 2N6768JTXV 2N6770 2N6770JTX	MTM15N35 2N6768JTX MTM15N45 2N6770JTX	3-27 3-462 3-32 3-32 3-32 3-32 3-467 3-37 3-37 3-37	BUZ11A BUZ14 BUZ15 BUZ17 BUZ18 BUZ20 BUZ21 BUZ23 BUZ23 BUZ24 BUZ25	BUZ11A	MTM35N05 MTP12N10 MTP20N10 MTM12N10 MTM25N10 MTM25N10	3-69 3-318 — — 3-441 3-472 3-444 3-303 3-303
2N6770JTXV 2N6781 2N6782 2N6783 2N6784 2N6784 2N6786 2N6786 2N6787 2N6788 2N6788	2N6770JTXV 2N6782 2N6784 2N6788		3-37 3-42 3-44 3-46 	BUZ27 BUZ28 BUZ31 BUZ32 BUZ33 BUZ34 BUZ35 BUZ36 BUZ37 BUZ38		MTP8N20 MTM7N20 MTM15N20 MTM8N20 MTM15N20	3-405
2N6790 2N6791 2N6792 2N6793 2N6794 2N6795 2N6796 2N6797 2N6798 2N6800				BUZ40 BUZ41A BUZ42 BUZ43 BUZ44A BUZ45 BUZ45A BUZ45A BUZ45B BUZ46 BUZ48		MTP2N50 MTP4N50 MTP4N50 MTM2N50 MTM4N50 MTM7N50 MTM7N50 MTM15N50 MTM4N50	3-350 3-385 3-385 3-350 3-385 3-258 3-258 3-283 3-385

TMOS INDEX CROSS-REFERENCE (Continued) (boundlood) 32M3R3333380R3 X3DM1 20MT

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #	Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
BUZ48A BUZ50 BUZ50A BUZ50B BUZ53A BUZ53A BUZ54A BUZ54A BUZ57A BUZ57A	0810781 0810781 18F0820	MTP1N100 MTP1N100 MTP1N100 MTM5N100	3-345 3-345 3-345 3-243 — —	IRF243 IRF250 IRF251 IRF252 IRF253 IRF320 IRF321 IRF322 IRF323	IRF243 IRF250 IRF251 IRF252 IRF253	MTM5N40 MTM5N40 MTM5N40 MTM5N35	3-91 3-93 3-93 3-93 3-390 3-390 3-390 3-390
BUZ58A BUZ60 BUZ60B BUZ63 BUZ63B BUZ64 BUZ64 BUZ71 BUZ71A BUZ71A BUZ72A BUZ73	BUZ71 BUZ71A BUZ73	MTP5N40 MTP5N40 MTM5N40 MTM5N40 MTM15N40	3-390 3-390 3-390 3-390 3-462 	IRF330 IRF331 IRF332 IRF333 IRF340 IRF341 IRF342 IRF343 IRF350 IRF351 IRF352	IRF330 IRF331 IRF333 IRF340 IRF350 IRF351	MTM5N40 MTM8N40 MTM8N40 MTM8N40	3-95 3-95 3-95 3-97 3-263 3-263 3-263 3-99 3-99 3-462
BUZ73A BUZ74 BUZ74A BUZ76 BUZ76A BUZ80 BUZ80A BUZ83 BUZ83A BUZ83A	BUZ84	MTP7N20 MTP2N50 MTP2N50 IRF732 IRF732 MTM4N85 MTM6N85	3-599 3-350 3-350 3-125 3-125 	IRF353 IRF420 IRF421 IRF422 IRF423 IRF430 IRF431 IRF431 IRF432 IRF433 IRF440	03469TM	MTM15N35 MTM2N50 MTM2N50 MTM2N50 MTM2N50 MTM4N50 MTM4N45 MTM4N45 MTM4N45	3-462 3-350 3-350 3-350 3-385 3-385 3-385 3-385 3-101
BUZ84A BUZ88 BUZ88A IRF120 IRF121 IRF123 IRF133 IRF130 IRF131 IRF132	BUZ84A	MTM12N10 MTM15N06E MTM12N10 MTM15N06E MTM12N10 MTM12N10	3-81 — 3-441 3-456 3-441 3-456 3-83 3-441 3-441	IRF441 IRF442 IRF443 IRF450 IRF451 IRF452 IRF453 IRF510 IRF511 IRF512	IRF450 IRF451 IRF452 IRF510 IRF511 IRF512	MTM7N50 MTM7N45 MTM15N50	3-101 3-258 3-258 3-103 3-103 3-103 3-467 3-105 3-105
IRF133 IRF140 IRF141 IRF142 IRF143 IRF150 IRF151 IRF152 IRF153 IRF220	IRF140 IRF141 IRF142 IRF150 IRF151 IRF152	MTM12N10 IRF141 MTM35N06E MTM8N20	0.05	IRF513 IRF520 IRF521 IRF522 IRF523 IRF530 IRF531 IRF532 IRF533 IRF540	IRF513 IRF520 IRF521 IRF522 IRF523 IRF530 IRF531 IRF532 IRF533 IRF540	18F6420	3-105 3-107 3-107 3-107 3-109 3-109 3-109 3-111
IRF221 IRF222 IRF223 IRF230 IRF231 IRF232 IRF233 IRF240 IRF241 IRF241	IRF230 IRF240 IRF241	IRF621 MTM8N20 IRF631 MTM8N20 IRF631 MTM15N20	3-89 3-117 3-405 3-117	IRF541 IRF542 IRF543 IRF610 IRF611 IRF612 IRF613 IRF620 IRF621 IRF622	IRF541 IRF542 IRF610 IRF612 IRF620 IRF621	MTP25N06 IRF621 MTP5N20 MTP5N20	3-111 3-111 3-477 3-113 3-115 3-113 3-584 3-115 3-115 3-584

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IRF623 IRF630 IRF631 IRF632 IRF633 IRF640 IRF641 IRF642 IRF643 IRF710	IRF630 IRF631 IRF632 IRF640 IRF641 IRF642 IRF643 IRF710	IRF621 IRF631	3-115 3-117 3-117 3-117 3-117 3-119 3-119 3-119 3-119 3-121
IRF711 IRF712 IRF713 IRF720 IRF721 IRF722 IRF723 IRF730 IRF731 IRF732	IRF720 IRF722 IRF730 IRF731 IRF732	IRF710 MTP2N40 MTP2N35 IRF720 IRF722	3-121 3-534 3-534 3-123 3-123 3-123 3-125 3-125 3-125
IRF733 IRF740 IRF741 IRF742 IRF743 IRF820 IRF821 IRF822 IRF823 IRF830	IRF733 IRF740 IRF741 IRF820 IRF821 IRF823 IRF830	MTP10N40 MTP10N35 MTP3N50	3-125 3-127 3-127 3-652 3-652 3-129 3-129 3-154 3-129 3-131
IRF831 IRF832 IRF833 IRF840 IRF841 IRF842 IRF9430 IRF9131 IRF9132	IRF831 IRF832 IRF833 IRF840 IRF841 IRF842 IRF843	MTM12P10 MTM12P06 MTM8P10	3-131 3-131 3-131 3-133 3-133 3-133 3-133 3-446 3-446 3-410
IRF9133 IRF9520 IRF9521 IRF9522 IRF9523 IRF9530 IRF9531 IRF9532 IRF9533 IRFD1Z0	IRFD1Z0	MTM8P08 MTP8P10 MTP8P08 MTP8P10 MTP8P08 MTP12P10 MTP12P06 MTP8P10 MTP8P08	3-410 3-410 3-410 3-410 3-410 3-446 3-446 3-410 3-135
IRFD1Z3 IRFD110 IRFD111 IRFD112 IRFD113 IRFD120 IRFD121 IRFD122 IRFD123 IRFD123	IRFD1Z3 IRFD110 IRFD113 IRFD120 IRFD123 IRFD210	IRFD110 IRFD110 IRFD120	3-135 3-137 3-137 3-137 3-137 3-139 3-139 3-139 3-141

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IRFD211 IRFD212 IRFD213 IRFD220 IRFD221	IRFD213 IRFD220	IRFD120	3-139 3-141 3-143
IRFD221 IRFD222 IRFD223 IRFD9110 IRFD9112 IRFD9120	IRFD223 IRFD9110 IRFD9120	IRFD220 IRFD9110	3-143 3-143
IRFD9123 IRFF110 IRFF111 IRFF112 IRFF113 IRFF120 IRFF121 IRFF122 IRFF123 IRFF220	IRFD9123 IRFF110 IRFF113 IRFF120 IRFF123 IRFF220	817274A 817274A	3-145
IRFF221 IRFF222 IRFF223 IRFZ20 IRFZ22 IRFZ30 IRFZ30 IRFZ40 IRFZ42 IVN5000AND	IRFF222 IRFF223 IRFZ20 IRFZ22 IRFZ30 IRFZ32 IRFZ40 IRFZ42	MPF910	3-149 3-151 3-151 3-153 3-153 3-155 3-155 3-155
IVN5000SNE IVN5000SNF IVN5000SNH IVN5000TND IVN5000TNE	D VISTMTM B WEET TO THE B WEET	MPF910 MPF990 MPF990 MFE960 MFE990 MFE960	3-157 3-157 3-178
IVN5001AND IVN5001AND IVN5001ANF IVN5001ANH IVN5001SND IVN5001SNE IVN5001SNF	MTM3SND IRFIAT MTM3SND MTMBNS1	MFE990 MPF910 MPF910 MPF990 MPF990 MPF990	3-160 3-157 3-157 3-178 3-178
IVN5001TNE IVN5001TNF IVN5001TNH IVN5200CND IVN5200HND IVN5200HNE IVN5200HNF IVN5200HNH IVN5200KND IVN5200KND	IRF621 MTM8NI20 IRF631 MTM8NI20 IRF631 MTM75NI20	MFE990 MFE990 MTP10N05 MTP10N10 MTM12N10 MTM12N10	3-160 3-160 3-160 3-625 — — 3-441 3-441

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Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #	Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement
IVN5200KNF IVN5200KNH IVN5200TND IVN5200TNE IVN5200TNF IVN5200TNH IVN5201CND IVN5201CND IVN5201CNE IVN5201CNF IVN5201CNF		MTM12N10 MTM12N10 MTP10N06 MTP8N08 MTP8N10	3-441 3-441 — 3-625 3-609 3-609 — — —	IVN6300SNM IVN6300SNP IVN6300SNS IVN6300SNU IVN6300SNU IXTH5N90 IXTH5N90A IXTH5N100 IXTH5N100A IXTH6N70	MTPRIM TO MERCAN	MTH5N90 MTH5N100
IVN5201KND IVN5201KNE IVN5201KNF IVN5201KNH IVN5201TND IVN5201TNE IVN5201TNF IVN5201TNH IVN5000CNS IVN6000CNT		MTM12N10 MTM12N10 MTM12N10 MTM12N10 MTM12N10	3-441 3-441 3-441 3-441 — — — 3-549 3-350	IXTH6N70A IXTH6N80 IXTH6N80A IXTH12N45 IXTH12N45A IXTH12N50 IXTH12N50A IXTM3N70 IXTM3N70A IXTM3N80	MTPBN45 MTPBN45 MTPBN45 MTPBN45 6	-0001110M
IVN6000CNU IVN6000KNR IVN6000KNS IVN6000KNT IVN6000KNU IVN6100TNS IVN6100TNU IVN6100TNU IVN6200CND IVN6200CNE	acиosнтМ	MTP2N50 MTM5N35 MTM5N40 MTM2N50 MTM2N50 MTP10N05 MTP10N06	3-350 3-390 3-390 3-350 3-350 — — 3-625 3-625	IXTM3N80A IXTM3N90 IXTM3N90A IXTM3N100 IXTM3N100A IXTM4N45 IXTM4N45A IXTM4N50 IXTM4N50A IXTM4N70	() () ()	
IVN6200CNF IVN6200CNH IVN6200CNM IVN6200CNP IVN6200CNR IVN6200CNS IVN6200CNT IVN6200CNU IVN6200CNW IVN6200CNW	Эниаснтм .	MTP12N08 MTP12N10 MTP8N20 MTP5N35 MTP5N40 MTP4N45 MTP4N50 MTP2N85 MTP2N85	3-441 3-441 3-405 — 3-390 3-390 3-385 3-385 3-385 3-355	IXTM4N70A IXTM4N80 IXTM4N90 IXTM4N90A IXTM4N90A IXTM4N100 IXTM4N100A IXTM5N900 IXTM5N900 IXTM5N900 IXTM5N100	8	
IVN6200KND IVN6200KNE IVN6200KNF IVN6200KNH IVN6200KNM IVN6200KNP IVN6200KNS IVN6200KNS IVN6200KNU IVN6300ANE	AGUSWTM GBUCWTM JOHEMTM	MTM12N05 MTM12N10 MTM12N10 MTM12N10 MTM8N20 MTM5N40 MTM4N45 MTM4N50 MPF910	3-436 3-441 3-441 3-441 3-405 	IXTM5N100A IXTM6N70 IXTM6N70A IXTM6N80 IXTM6N80A IXTM7N45 IXTM7N45A IXTM7N50 IXTM7N50A IXTM7N50A IXTM12N45	обиватм	BUZ84A BUZ84A BUZ84A BUZ84A MTM8N45 MTM8N50 MTM8N50 MTM15N45
IVN6300ANF IVN6300ANH IVN6300ANM IVN6300ANP IVN6300ANS IVN6300ANT IVN6300ANU IVN6300SNE IVN6300SNF IVN6300SNH	MINSUS MINSUS MINSUS MINSUS MINSUS MINSUS	MPF990	3-178	IXTM12N45A IXTM12N50 IXTM12N50A IXTP3P70 IXTP3P70A IXTP3N80 IXTP3N80A IXTP3N90	ar watow s MTD sows	MTM15N45 MTM15N50 MTM15N50 MTP3N75 MTP3N80 MTP2N90 MTP2N90 MTP2N90 MTP3N100

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #	Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacemen
IXTP3N100A IXTP4N45A IXTP4N45A IXTP4N50 IXTP4N50A IXTP4N70A IXTP4N70A IXTP4N80A IXTP4N80A IXTP4N90	MIHSWIN	MTP3N100 MTP4N45 MTP4N45 MTP4N50 MTP4N50	3-559 3-385 3-385 3-385 3-385 ————————————————————————————————————	MTD3055E MTH5N95 MTH5N100 MTH6N55 MTH6N60 MTH6N85 MTH6N90 MTH7N45 MTH7N50 MTH8N35	IVIIDOUGGE	
IXTP4N90A IXTP4N100 IXTP4N100A IXTP7N45 IXTP7N45A IXTP7N50 IXTP7N50A MCR1000-6 MCR1000-6	MCR1000-4 MCR1000-6	MTP8N45 MTP8N45 MTP8N50 MTP8N50	3-620 3-620 3-620 3-620 3-620	MTH8N40 MTH8N55 MTH8N60 MTH8P18 MTH8P20 MTH13N45 MTH15N20 MTH15N20 MTH15N35	MTH8N55 MTH8N60	
MCR1000-8 MFE910 MFE930 MFE960 MFE990 MFE9200 MGM5N45 MGM5N50 MGM20N45 MGM20N50	MFE9200 MGM5N45 MGM5N50 MGM20N45 MGM20N50	A 6 A0 A	3-157 — 3-163 3-166 3-166 3-170 3-170	MTH25N08 MTH25N10 MTH25P05 MTH25P06 MTH30N18	MTH15N40 MTH20N15 MTH20P08 MTH20P10 MTH25N08 MTH25N10 MTH25P05 MTH25P06	MTH20N15
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